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InRel-NPower - Innovative Reliable Nitride based **Power Devices and Applications**



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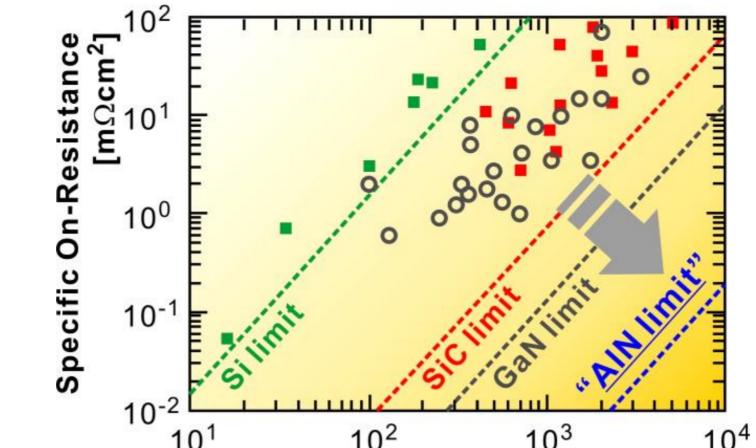
Overview and Introduction

Electric Energy: a major challenge

The way in wich energy is used has great impact on the economy, the environment and society. Currently, 40% of the energy used in the world is electricity, and it is expected to reach 60% by 2014.

However, a major part of the produced electricity is lost in electric power conversion.

Nitride-based semiconductors Si MOSFET 4H-SiC MOSFET O GaN HEMT



Ambition of the *InRel-NPower* project

The InRel-NPower project researches GaN and AIN-based transistor devices for application in power electronics. These material have performances 10 to 100 times higher than silicon currently being used - which could result in conversion systems achieving a 99% conversion efficiency!

We aim to mature the technology: by focusing on the raw material, on the packaging and by demonstrating its potential in a final device.

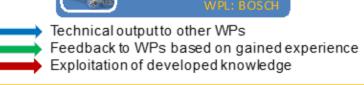




To reduce such losses we must create electronic devices that use new materials with higher efficiency.



Blocking Voltage [V] On-resistance as a function of blocking voltage for Si, SiC, GaN and AIN semiconductor materials. Nitrides outperform all others.



Material/Epitaxy and Device Processing

Material and Epitaxy

III-nitride material is the core enabler of superior switching devices: ≻GaN-on-Si

The project's baseline technology, with an emphasis on improving reliability by using different epitaxial buffer structures

► AIN-based electronics

Explorative investigation of the epitaxy of Ultra-Wide Bandgap layer structures grown on AIN templates (obtained by HVPE or 3SG)or bulk substrates (grown by PVT).

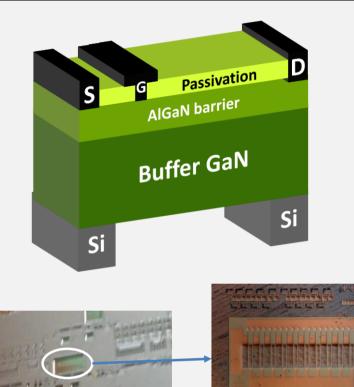
Advanced Material Characterisation

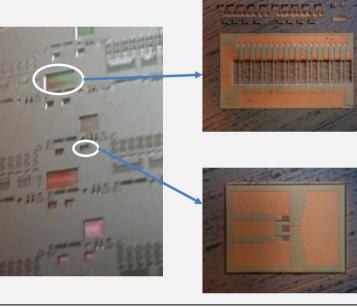
A major objective is to determine the correlation between material properties and device performance through XRD, AFM, SEM, TEM, CL, PL, EBSD, ...



Device Processing

- Optimization of power device processing on 6-inch GaN-on-Si wafers in ON-Semi's pilot line
 - Improvement of specific process modules for highly reliable and stable devices targeting on-resistance < 20mΩ, 650V
- Development of higher voltage GaN-on-Si power devices beyond 2 kVolts
- Optimization of substrate removal and subsequent replacement of the substrate by AIN material
- Development of new types of power devices based on AIN bulk substrate to enhance the breakdown voltage while delivering higher thermal dissipation.

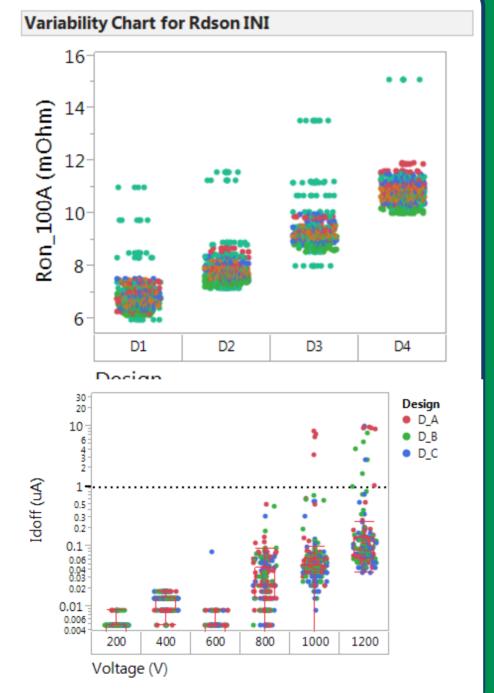




Characterization and Reliability

Characterization

- Statistical data collection of prime transistor
- parameters. Up to 100A, up to 1.2kV.
- ► Wafer level Pulsed I-V for dyn Ron characterization on >100 devices per wafer
- Substrate ramp measurements to investigate the effect of buffer traps
- ➤Wafer level reliability e.g. HTRB, HTGB, at various voltage levels, including short circuit testing
- Device screening, binning strategy
- \succ Measurement on devices with Si substrate removed, and on GaN-on-AIN devices. Up to 3kV.
- ➤Catholuminescence and electroluminescence



Reliability

- GaN power devices with proven reliability, beyond JEDEC
 - standardization of the requirements and protocols for the DGD analysis of the stability of HEMTs for high-voltage operation = -0.4 μs
- > Understanding of GaN HEMT transistor failure mechanisms to DGD = -0.75 μs enable life time prediction for use conditions
 - Analyze and modeling of the failure mechanisms of high voltage/power HEMTs operated under realistic use conditions
 - correlate the parametric degradation processes during accelerated stress to GaN material parameters
 - define stress and failure analysis protocols

Extraction of acceleration models (field, temperature, current,...) to build mission profiles

DGD = 0.4 μs DGD = -0.4 μs	Drain Cate
DGD	Drain
= -0.75 μs	Gote
DGD = -0.85 μs S	Drain Gote
DGD	Drain
= -0.9 μs	Gute
DGD	Drain
= -0.95 μs	Goire
DGD	Drain
= -1 μs	Gote

Packaging and Demonstration

Advanced low inductance packaging for power devices

► Low inductance packaging

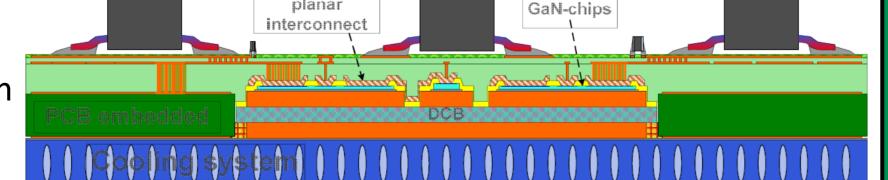
Advanced double-sided ceramics module design

Low inductance packaging

- Flexible planar interconnection
- Reduced electrical noise from smaller system
- Higher frequency drive operation
- Compact packaging
 - Higher reliability, robustness and reduction of system size
 - Includes embedded active and passive components/ sensors

and cooling

- Demonstrator (objectives):
 - Motor drives inverter with 60 % less power losses, more than 30 % reduction in volume and 50% higher power density
 - DC2AC converter: 2KW@30V at 50°C, peak efficiency up to 99% and expected life of 10⁶ hours at 30°C



- Double-sided ceramics design
- Usage of AMB-base power substrate and LTCC-base logic counter-substrate
- Compact packaging
 - Higher power densities by integration of further active and passive components / sensors on LTCC-substrate
- High effective and efficient AMB-backside cooling
- ► Robustness characteristics
- Built-up using robust double-sided Ag-sintering joining technology with potential up to 200°C junction temp.
- Validation of design's robustness characteristics including new GaN-devices especially by power cycle tests

