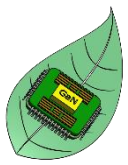
GaNonCMOS

GaNonCMOS (Power Conversion Applications)
Program Overview and
focus on 12/24/48V to 1V Voltage regulators

Séamus O'Driscoll

GaNonCMOS Program Introduction



www.ganoncmos.eu

Market Demand Partners

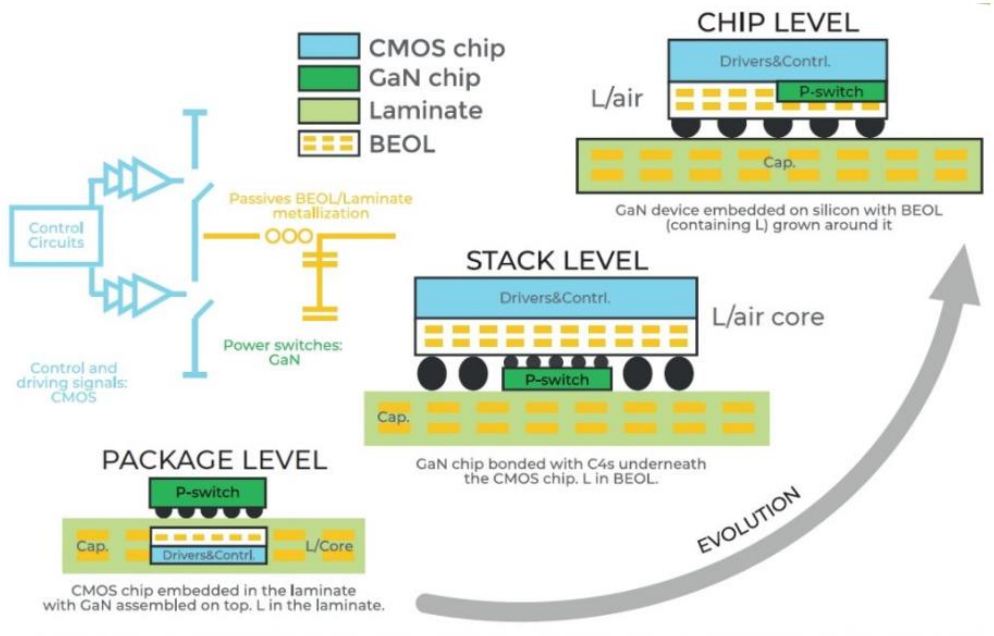
HPC: Server VR, Multi-Node

IBM

Merchant POL, Aerospace,

Automotive:

RECOM



Program Scope: GaN in Integration Power Systems

Today's 12V to 1V8 Server/PC VRM

Efficient, Dense, Low Cost

Flexible for Multi-Node, Multi Core, Lower Voltages, SoC Power, Nano-Grid Power

Compatible Input Power and Output Power

Systems & Demonstrators

Hardware Design Partners

Wafer: EpiGaN

GaN Switch: Fraunhofer IAF

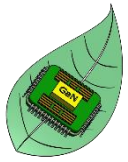
CMOS Control/Driver: ihp

Fouad Benkhelifa, Richard Reiner,
Norbert Fiebig, Marco Lisker
Gerald Weidinger, Gerald Weis
Stanislav suchovski
Thomas Brunschwiler, Cezar Zota

Embedded Substrate Technology: (Magnetic Devices and Semiconductors) AT&S

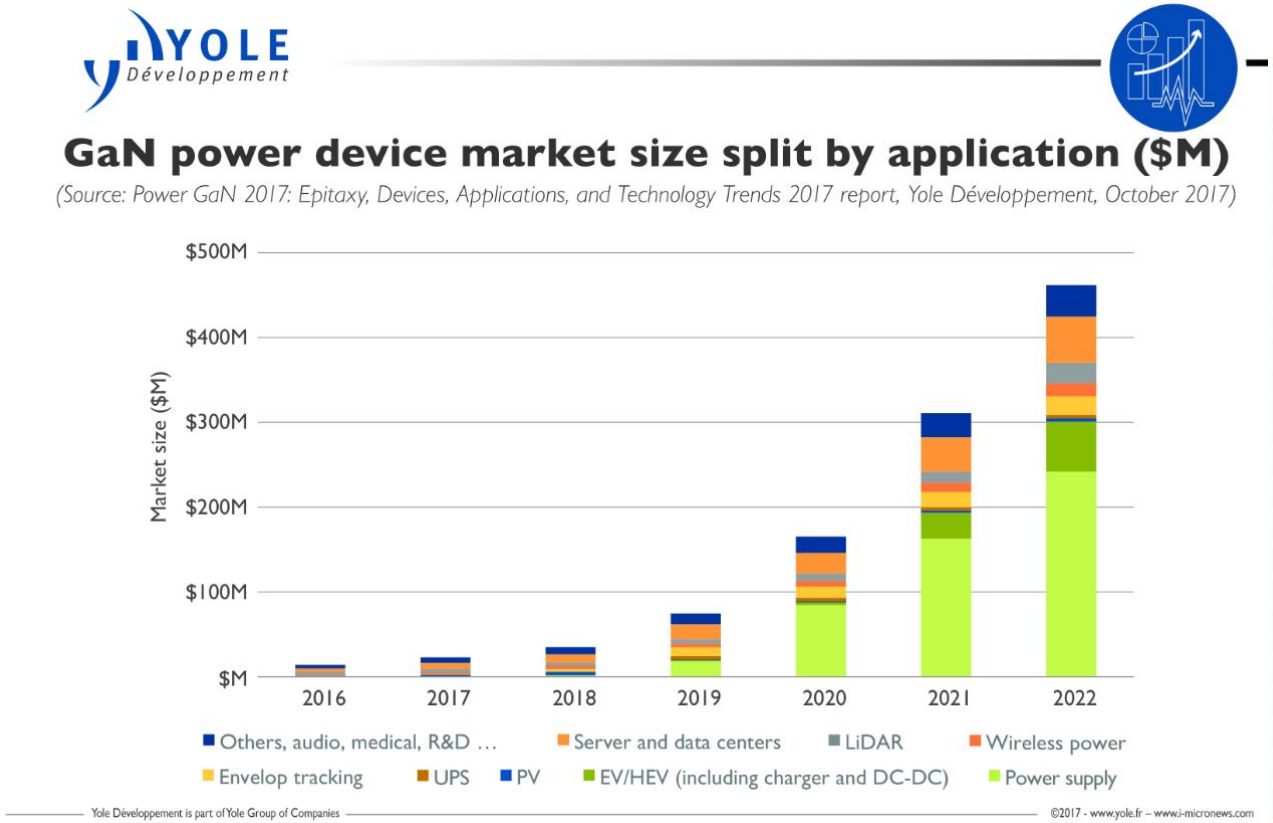
Voltage Regulator Designs and Advanced Integrated Magnetic Materials/Devices Tyndall National Institute

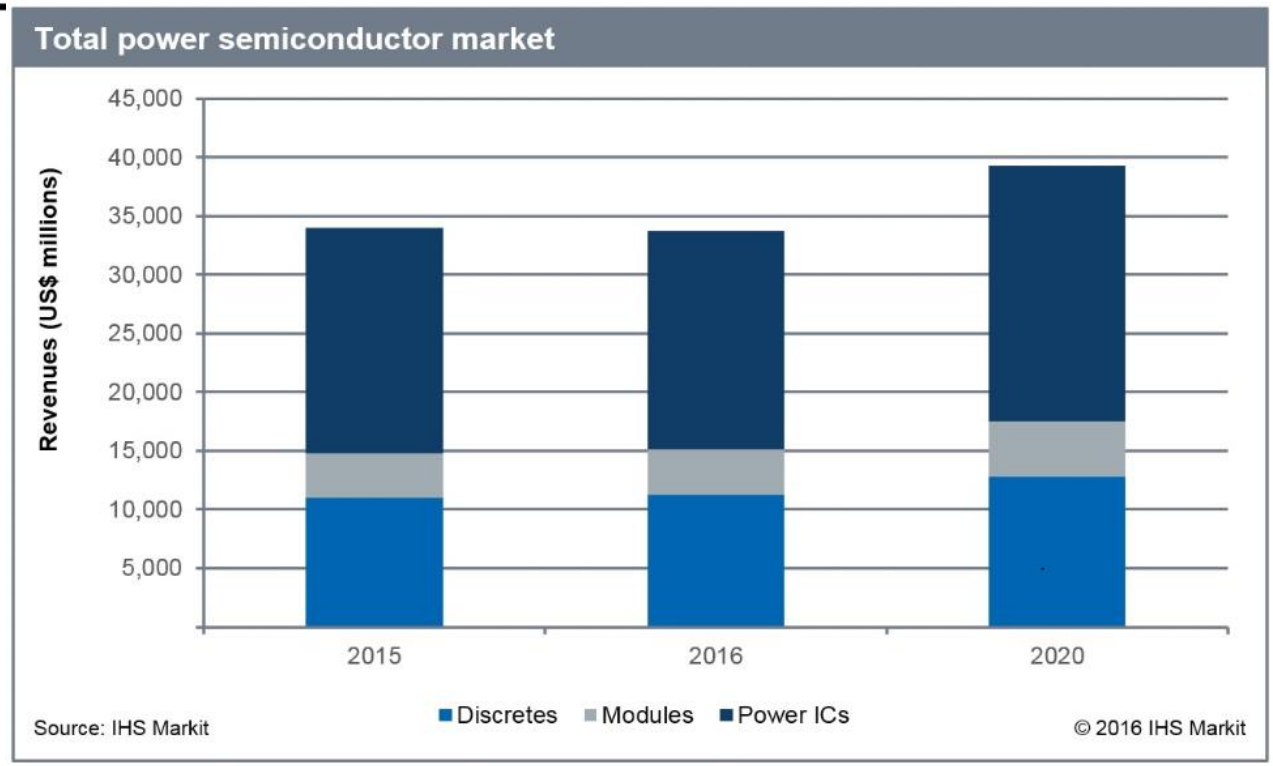
Reliability & Power System Manufacturing RECOM



GaN Switches in Power Conversion

- CAGR 50-70%, Still low percentage of overall market,…

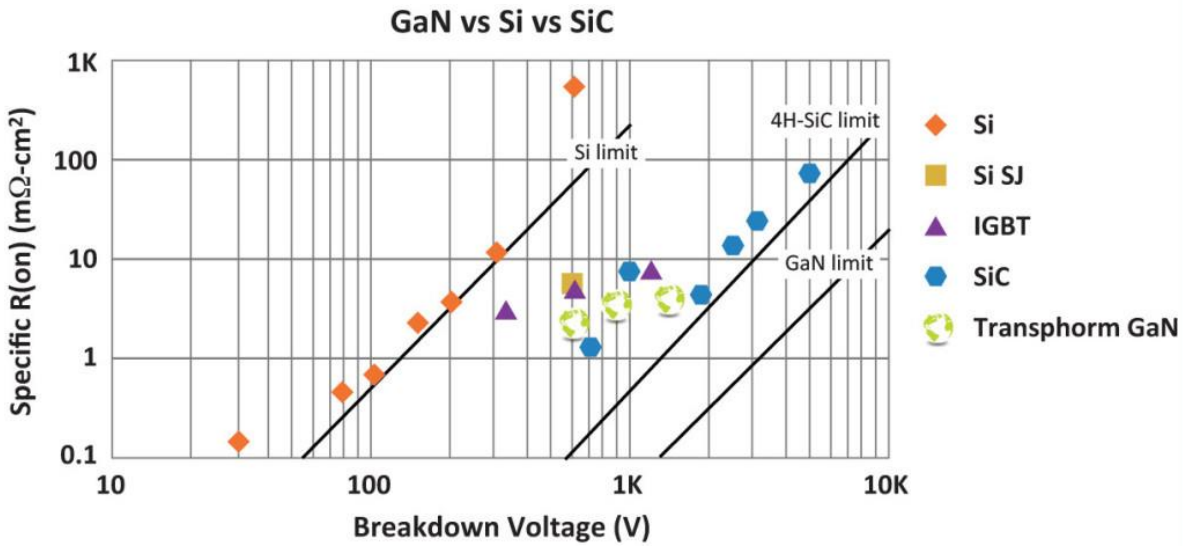




GaNonCMOS will apply to all of these segments

GaNonCMOS encompasses Discretes (Smart Drivers), Modules & Power ICs

GaN Application Advantage - Density



https://www.transphormusa.com/en/

Note the lower x-axis limit is usually shown as 50V!

600V Rated Application may employ 100V to 600 V switches depending on topology level count.

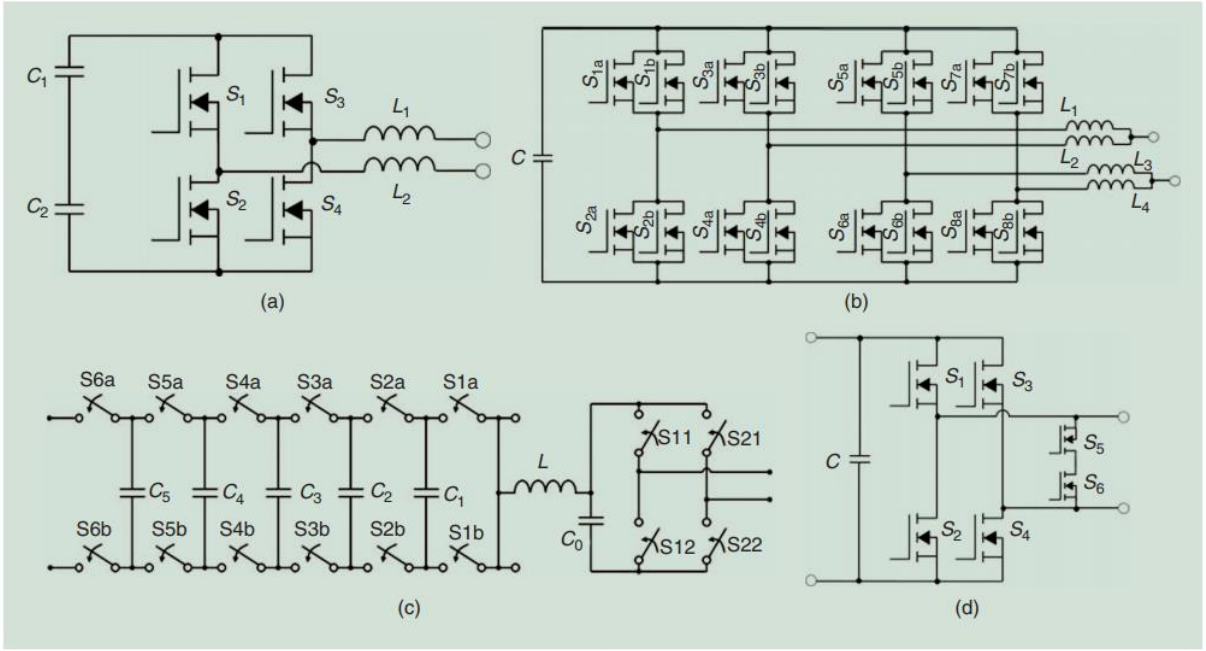


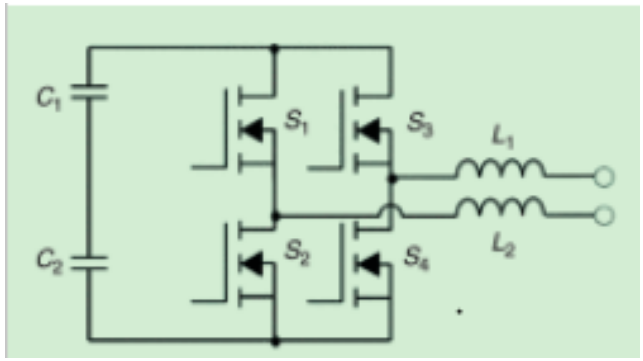
FIG 2 The inverter topologies used by LBC finalists. (a) Basic full-bridge inverter topology, as in TT, Texas A&M, Schneider, and UT; (b) parallel full-bridge inverter topology, as in ETH Zurich and CE+T; (c) seven-level flying capacitor inverter topology, as in UIUC; and (d) HERIC inverter topology, as in VT.

2014-2015 Little Box Challenge (LBC) by Google & IEEE

- > 215-W/in^3 power densities in 1kVA DC-AC inverter
- most of the top 16 entries used GaN

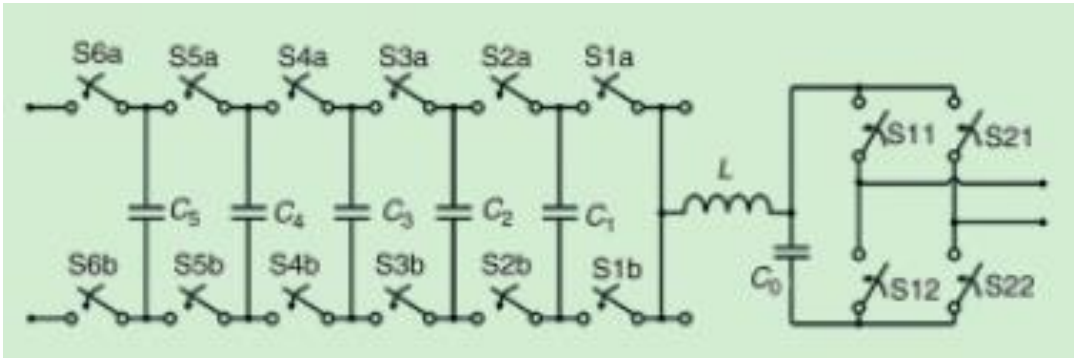
1. C. W. Halsted and M. D. Manjrekar, "A Critique of Little Box Challenge Inverter Designs: Breaking from Traditional Design Tradeoffs," in *IEEE Power Electronics Magazine*, vol. 5, no. 4, pp. 52-60, Dec. 2018. doi: 10.1109/MPEL.2018.2873992
2. https://pilawa.ece.illinois.edu/files/2016/05/Pilawa_PELS_webinar_may_25_2016_FINAL.pdf

Littlebox Finalist Solutions Illustrate Switch Voltage Rating Options for 1kVA DC-AC Inverter



Taiwan Tech (TT) Basic Full Bridge
- this will require >**600V** rated GaN switches > DC Link Voltage

600V GaN competes with 100V GaN!

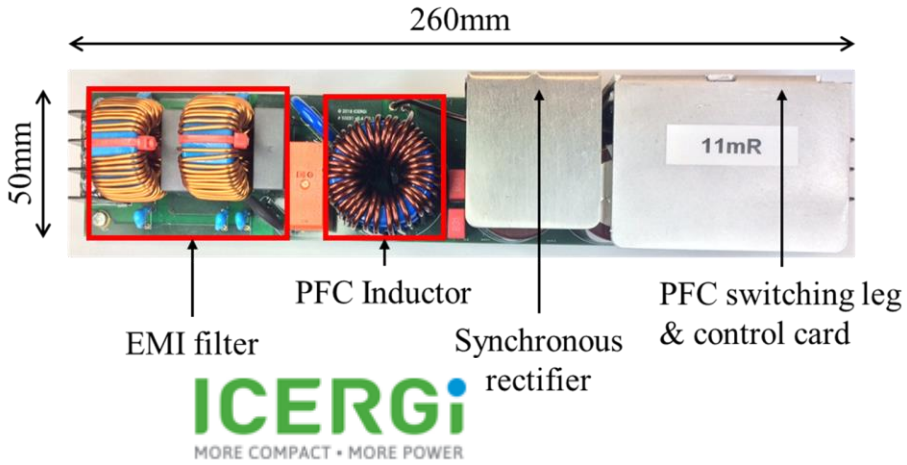


7-Level Flying Capacitor (FCML) Inverter with Output "unfolder" used **100V** EPC eHEMT devices

- DC Link Voltage is evenly divided across capacitors. Capacitors "break" the switching voltage.

- Effective per-switch frequency is reduced or Inductor V.s reduced

Commercial 3kW PFC Prototype (Titanium+ 85-264V_{RMS})

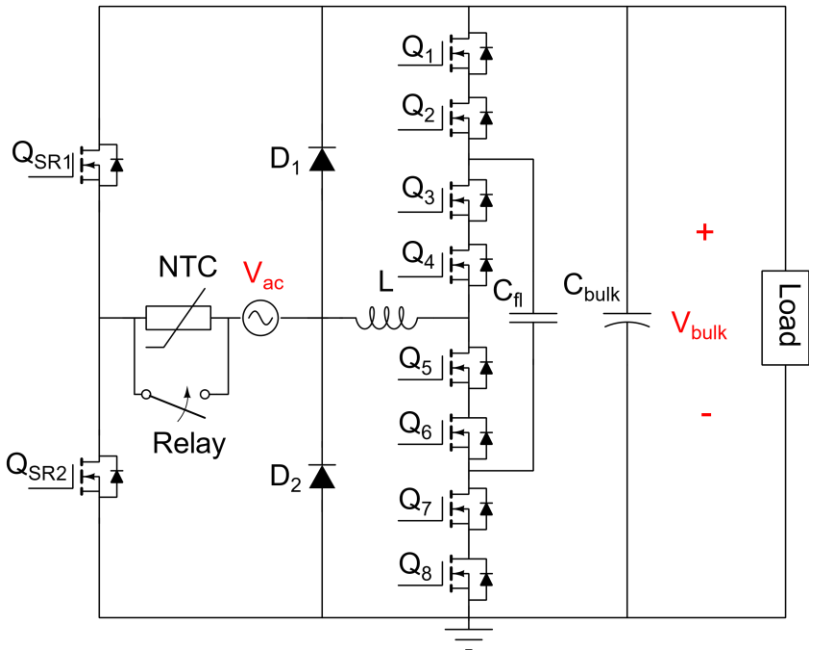


PFC PERFORMANCE BENCHMARK

Design/Efficiencies	115Vac	230Vac
ICERGi High Performance with SR	98.1%	99.1%
ICERGi Industrial with Diodes	97.5%	98.8%
Today's Industry "up-market"	95.0%	97.5%

- *Stacked Switches* reduces Conduction & Switching Losses Significantly
- GaN in similar ML design would increase efficiency from 98.1 to ~98.5%?

3-Level PFC Implementation using 150V Silicon MOSFETs



Diodes are to bypass inrush surge to C_{Bulk}

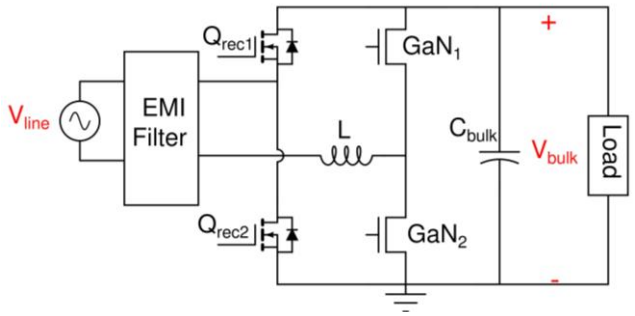
Low Voltage Silicon Switch Stacks and Multi-Level competing with GaN

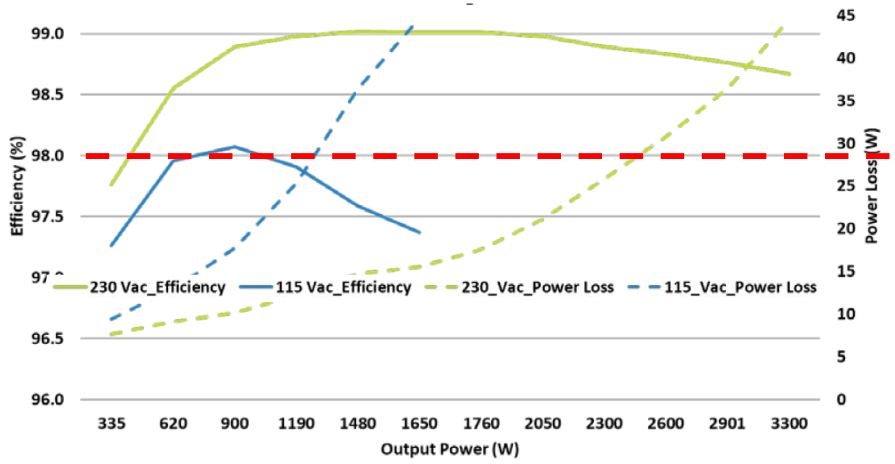
COMPARISON BETWEEN 300V AND 150V MOSFETs

	300V SuperSO8 BSC13DN30NS	**150V** SuperSO8 BSC110N15NS5	**2 x 150V** SuperSO8 BSC110N15NS5
On-state resistance R_{dson}	130mR	11mR	22mR
Reverse recovery time t_{rr}	111ns	45ns	45ns
Reverse recovery charge Q_{rr}	249nC	46nC	46nC
Output charge Q_{oss}	48nC	78nC	166nC
Gate charge Q_g	23nC	28nC	56nC
Wide selection of R_{dson}	×	✓	
Great switching characteristics	×	✓	

Optimised Silicon vs GaN Implementation for 3kW PFC

Transphorm GaN 3.3kW PFC: 50kHz Bridgeless 2-Level



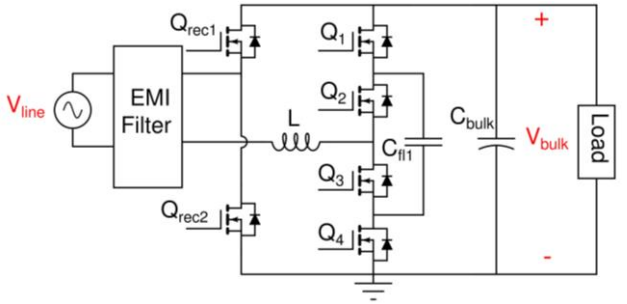


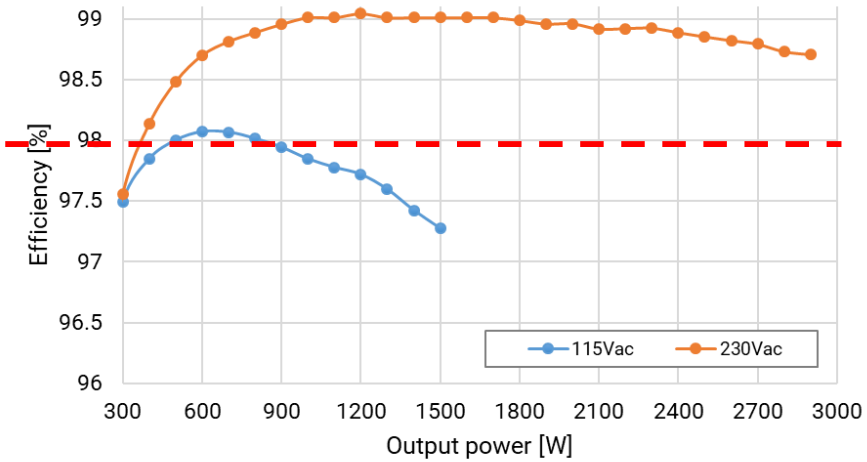
- Switching leg: **2 x 600V 35mR GaN Transphorm**
- Synchronous rectifier: **2 x 14mR 650V SJ MOSFETs**
- PFC Inductor volume: 142cm

ICERGi 3kW PFC: 70kHz Bridgeless 3-Level

ICERGi MORE COMPACT • MORE POWER

www.icergi.com





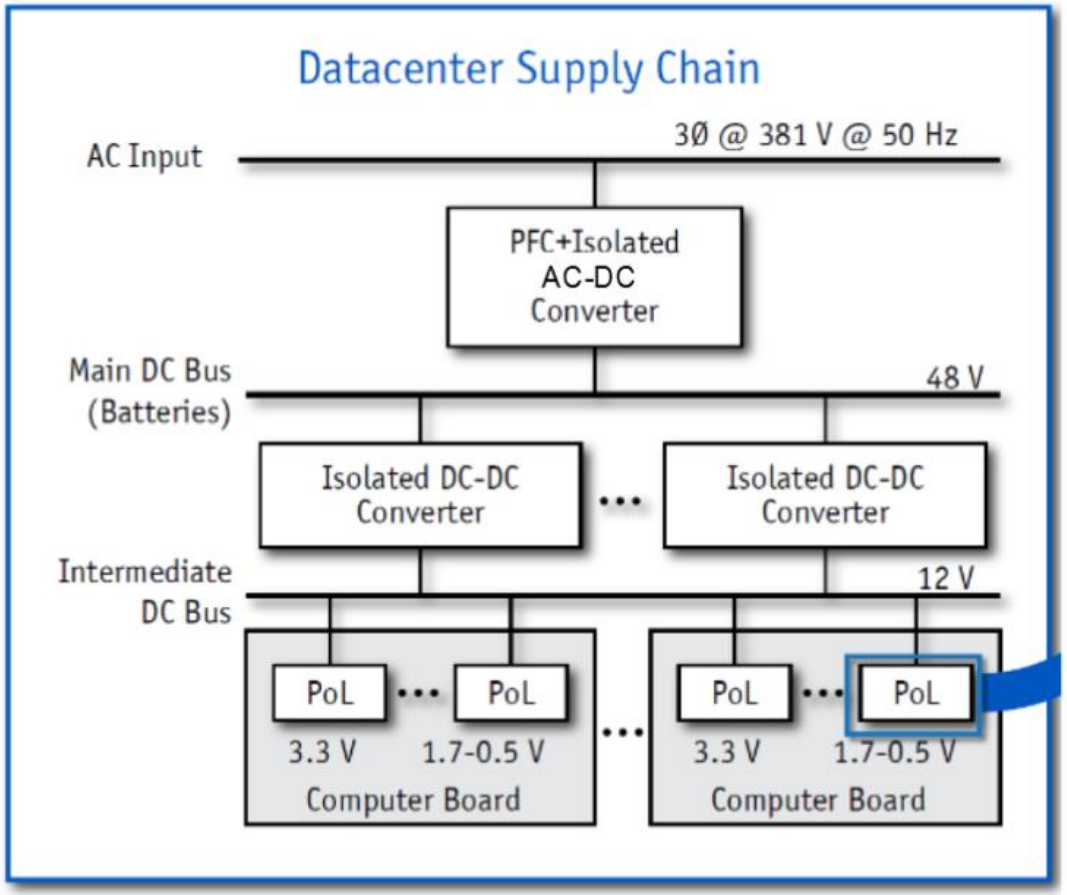
- Switching leg: **8 x 150V 11mR 150V OptiMOS Infineon**
- Synchronous rectifier: **2 x 19mR 650V SJ MOSFETs**
- Inductor volume: 35.2cm^3 (**~ 4 x reduction**)

Note what 3-L does o Inductor Volume

Low Voltage DC-DC POL Focus

Functional Electronic Packaging

Data Center Voltage Conversion … point of load converters



Courtesy P. Martinez Bezerra

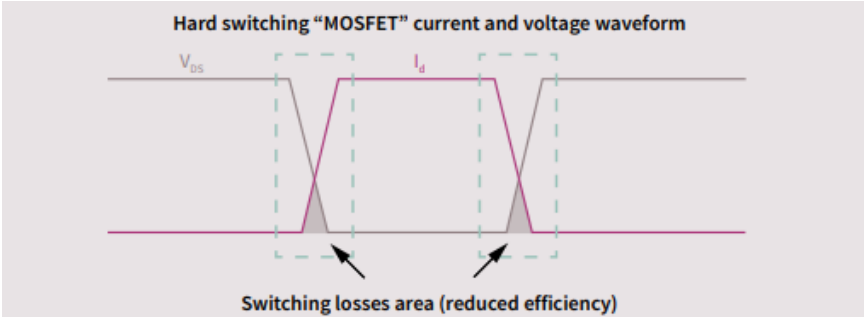
- *GaNonCMOS Program is concentrating on 12V/24V/48V to low output voltage*
- *Conversion for GP POL, and VRM for HPC.*
- *HPC may use direct conversion from 48V (Lower DC Distribution Loss)*
- *Aerospace (24V)*
- *Automotive (-> 48V)*

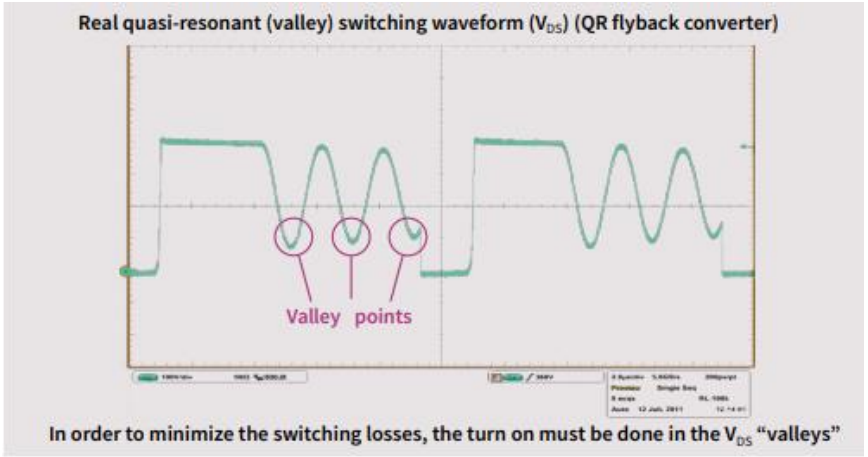
Some Switch-Mode Converter Operating Concepts and Loss Mechanisms

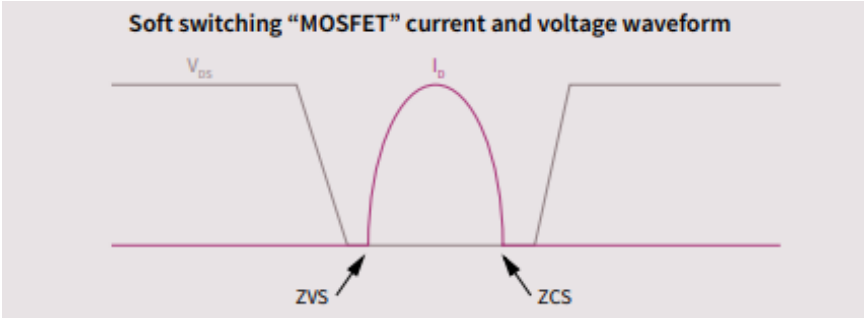
Basic Switching Loss Concepts

- Hard Switching
  - **Coss**, 3rd Quadrant Conduction **Recovery**, **Egt** (gate total energy) and **VI overlap** feature.
  - Resonant Valley – Coss (Vds), Egt

- Soft Switching
  - ZVS – turn on at zero voltage
  - ZCS – turn off at zero current

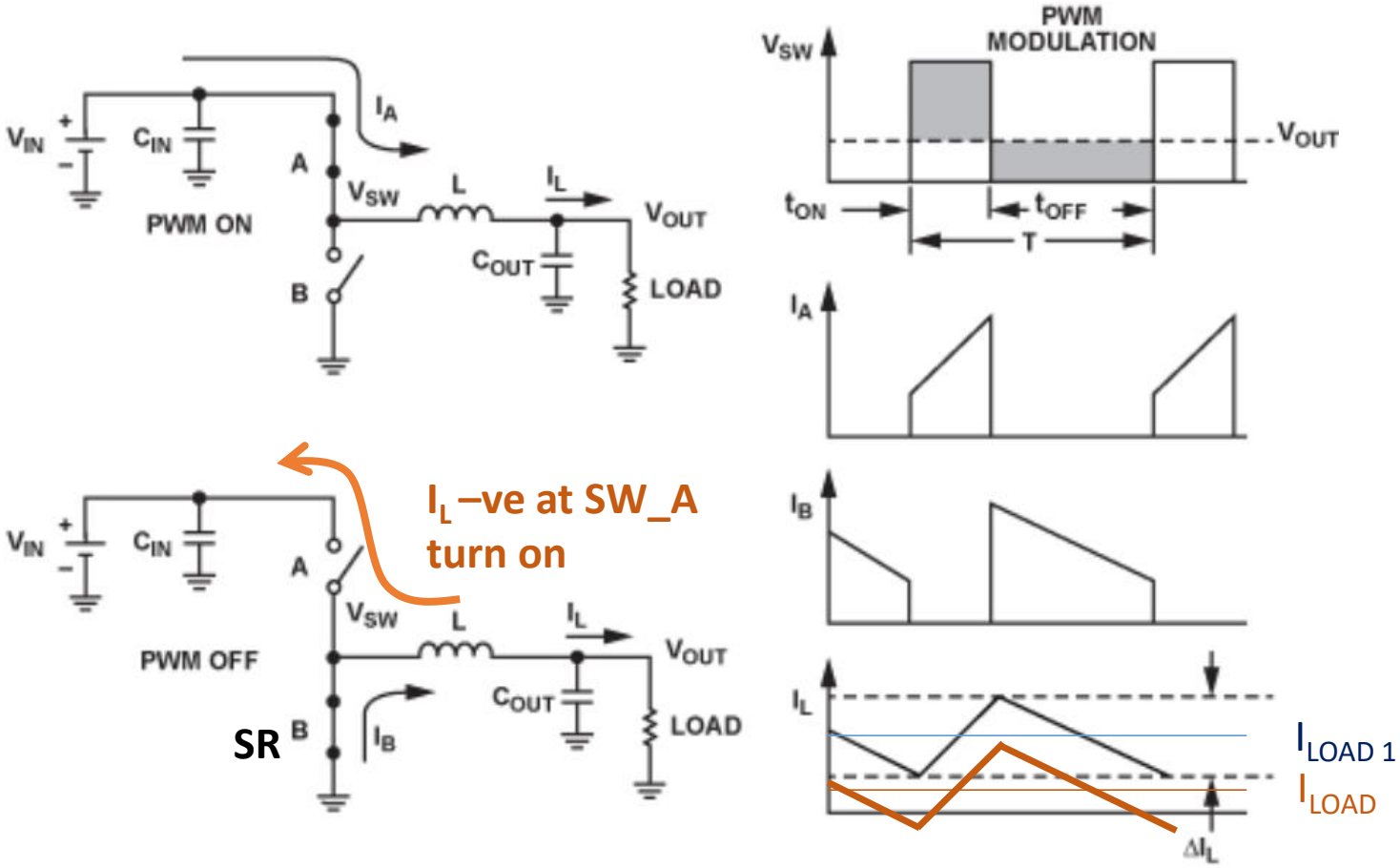






Continuous Conduction Mode (CCM)
Basic Buck Converter – some basic switching features

- Converter may achieve ZVS on Synchronous Rectifier (SR) with correct SR turn-on dead-time control (and positive I_L at the end of the switching cycle)
- With +ve I_L , SW_A may hard switch at turn on. It will discharge its own Coss, charge SR Coss and may recover SR
- If I_L negative at end SR on time; SW_A may also turn on with ZVS (if the inductor energy can drive Coss X 2)
- **3rd Quadrant Conduction functionality is important**
- Inrush surge current, with the application of input supply voltage requires <u>normally-off</u> device



Flying Capacitor Multi-Level Converter (3-L)

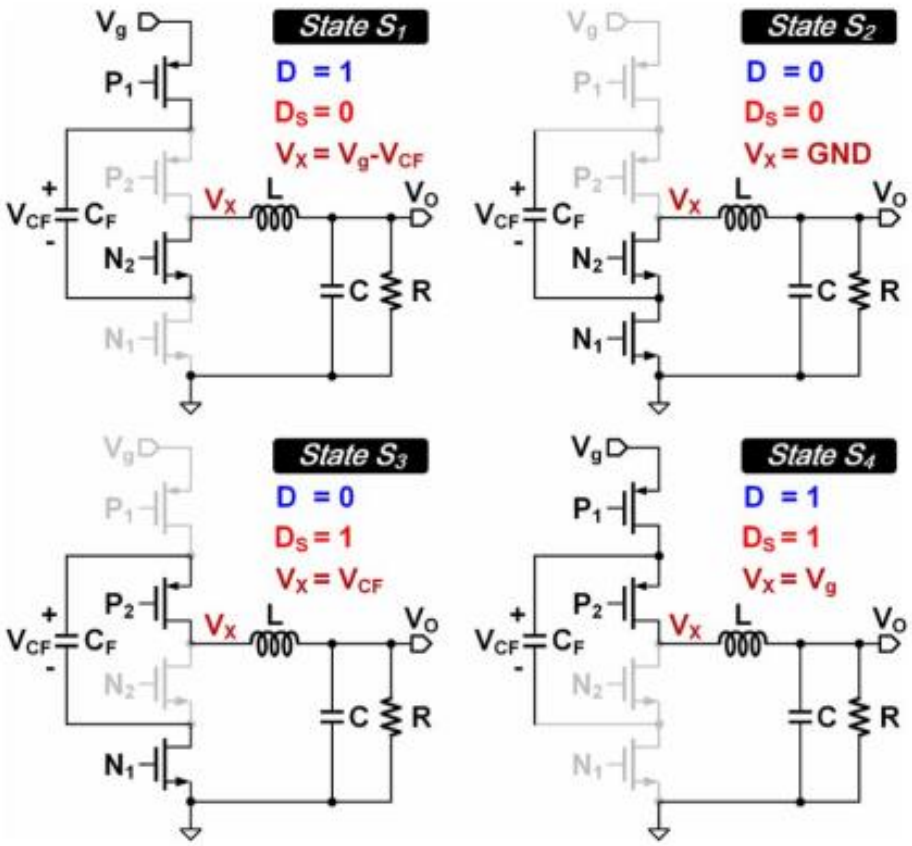
- Many conduction modes but the basic idea is that a charged flying capacitor will be in series with supply voltage to reduce the blocking voltage (BV) for all switches.
  - Also effective output switching frequency doubled (or per switch ***fs*** halved)
  - Average Switching Stage Output Voltage may be halved (or doubled)
  - Inductor Voltage-Second requirement may be reduced 4X (4X magnetic core size reduction)

V.dt = L.di

  - Duty Cycle Extension useful for High Step Down Ratio
  - Duty Cycle Extension useful to allow Multi-Phase with Achievable Inductor Coupling Factors

- Remove the flying cap => Stacked Switch solution

- These system integration possibilities are being explored holistically across GaNonCMOS



Four operation states of a 3-level buck converter S_1, S_2, S_3, and S_4.

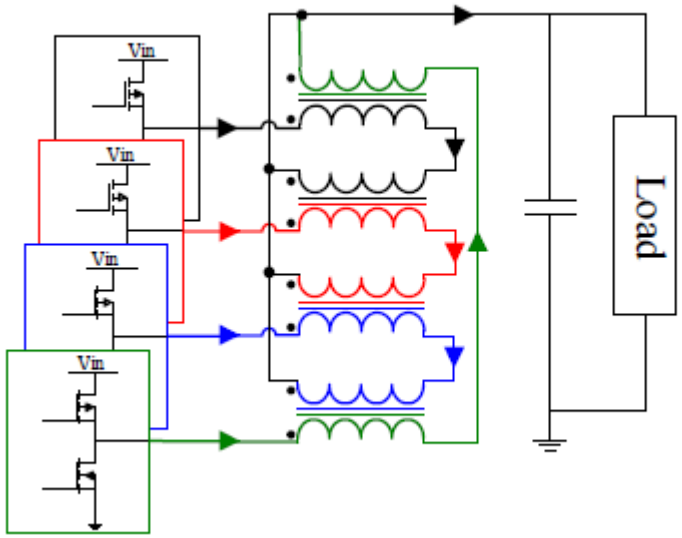
X. Liu, P. K. T. Mok, J. Jiang and W. Ki, "Analysis and Design Considerations of Integrated 3-Level Buck Converters," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 5, pp. 671-682, May 2016.

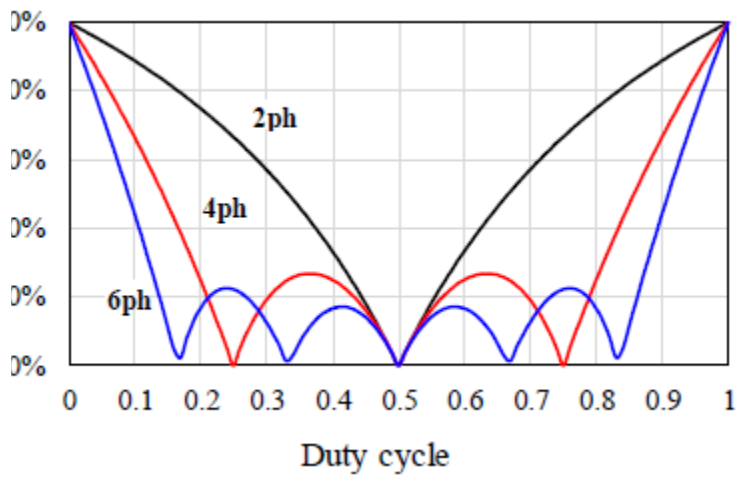
Multi-Phase Motivation -

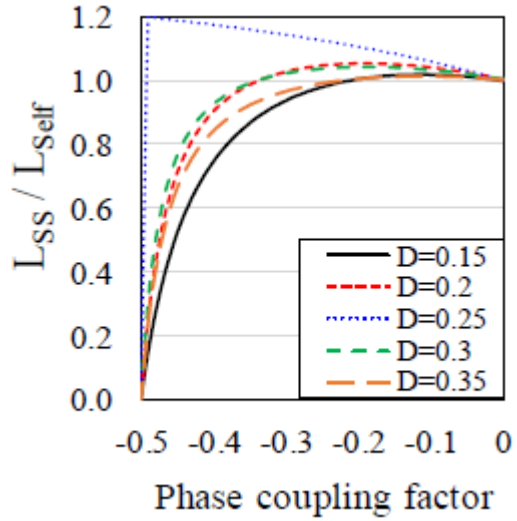
Interleaved Output Ripple reduction for Capacitor Advantage

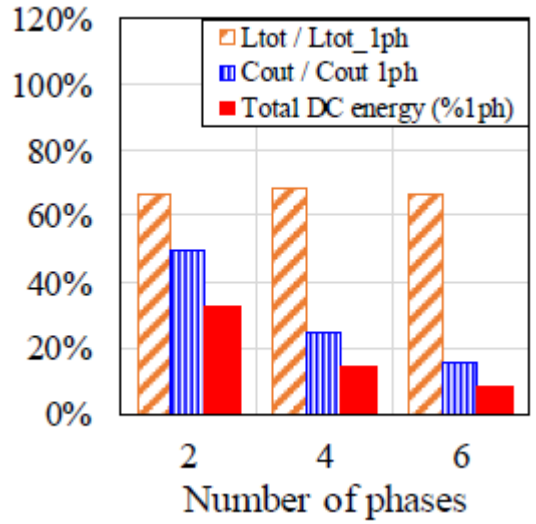
Inverse Coupled Inductors to cancel DC field and reduce ripple by increasing effective per phase steady-state inductance

Multi-Phase and Granular Power motivate us to consider smaller (1-4A) integrated POL stage



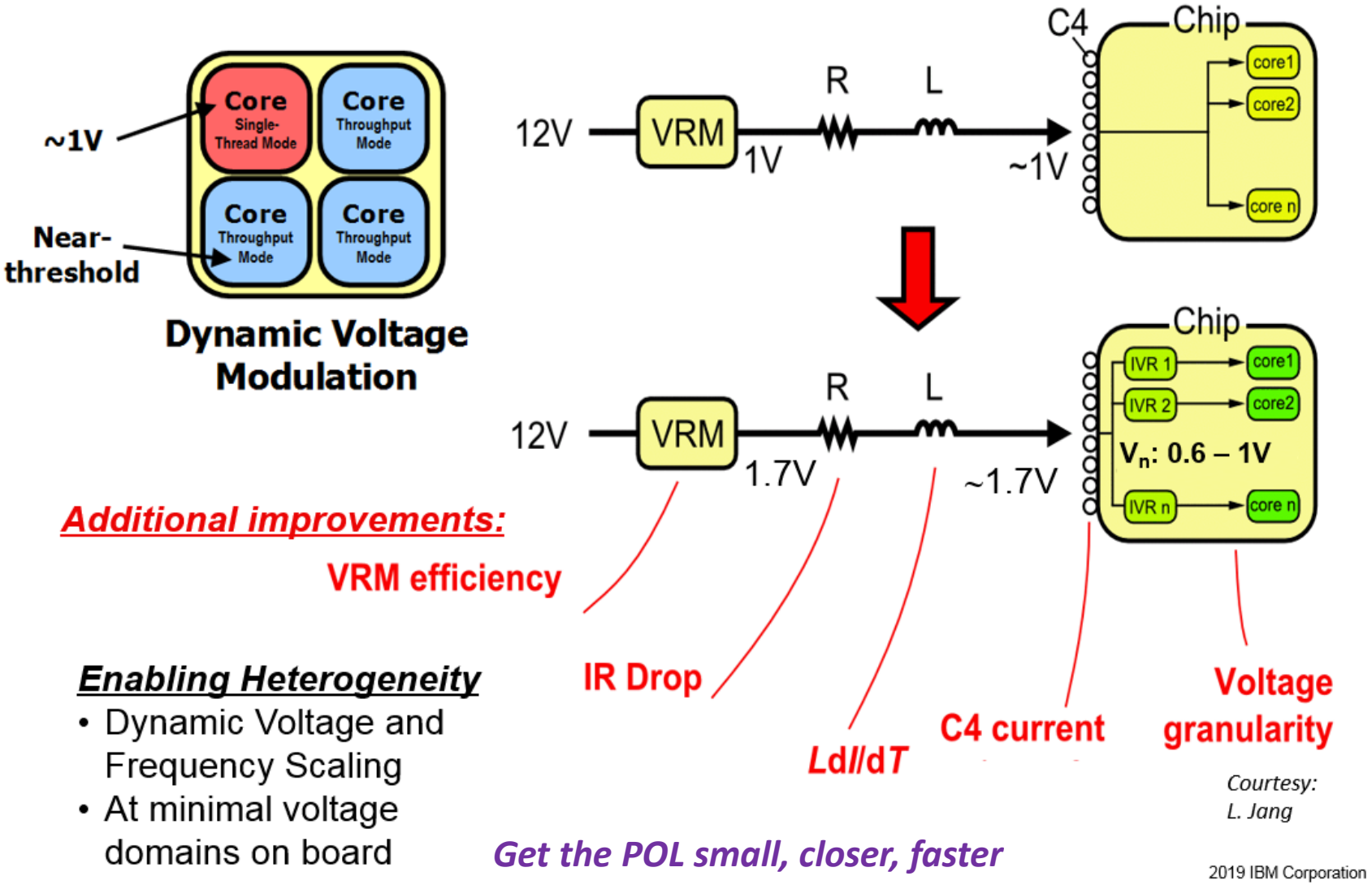






Y. Kandeel and M. Duffy, "Comparison of Coupled vs. Non-Coupled Microfabricated Inductors in 2W 20MHz Interleaved Buck Converter," *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA, 2019, pp. 2638-2645.

On-Chip Voltage Regulation … granular DC-DC conversion



Enabling Heterogeneity

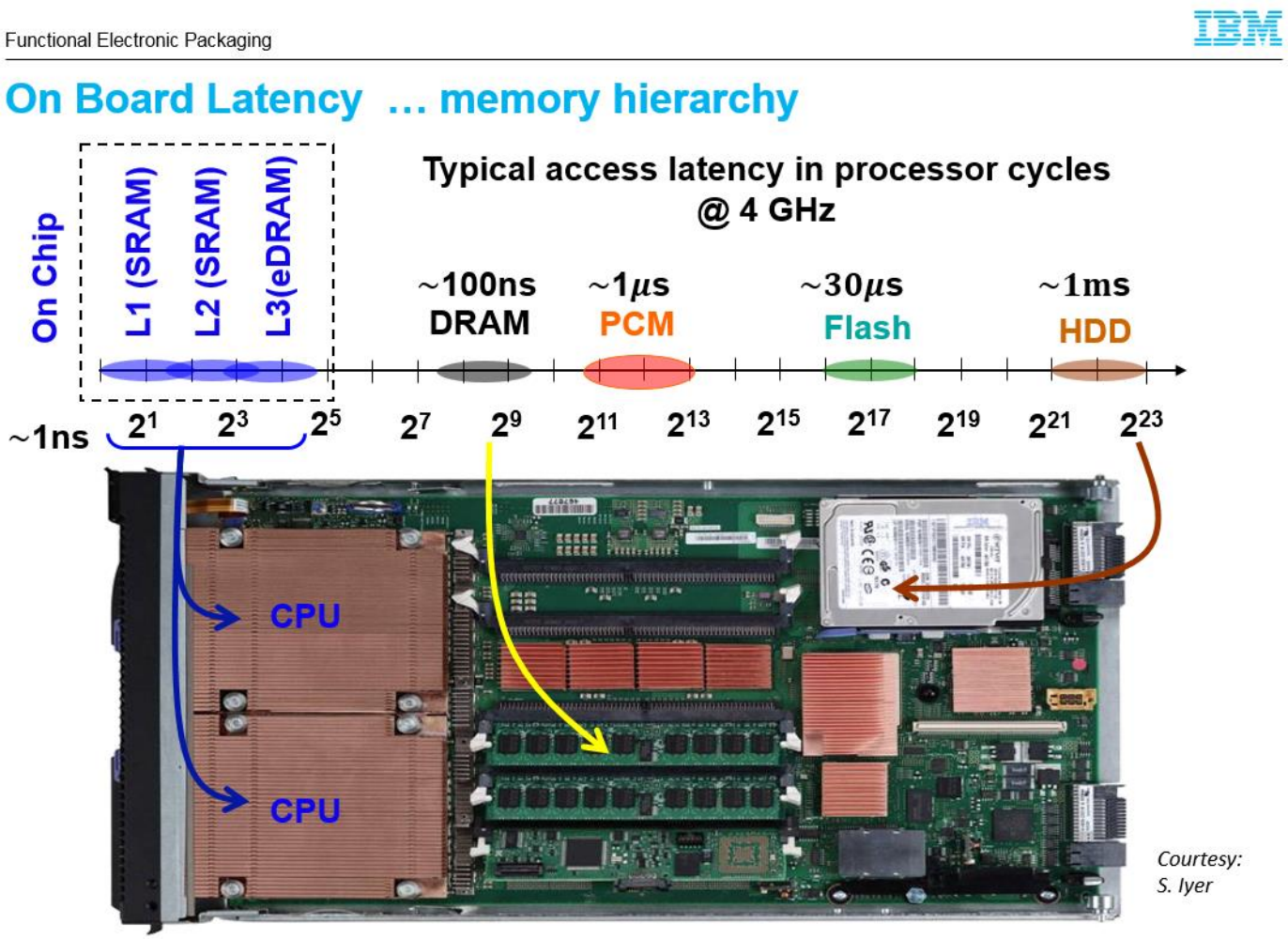
- Dynamic Voltage and Frequency Scaling
- At minimal voltage domains on board

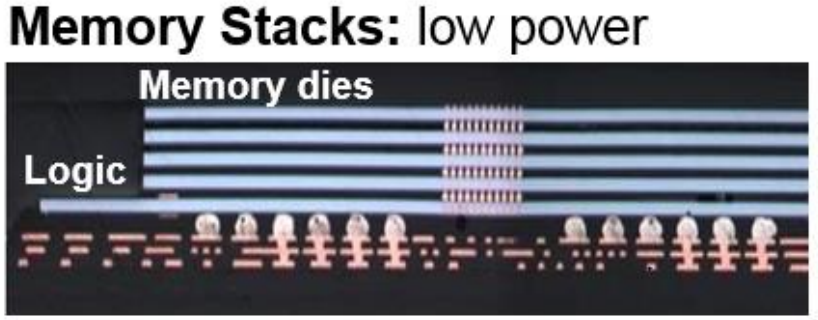
Get the POL small, closer, faster

Mobile SoCs tend to have 20 to 40 Voltage Rails/Domains for battery life extension

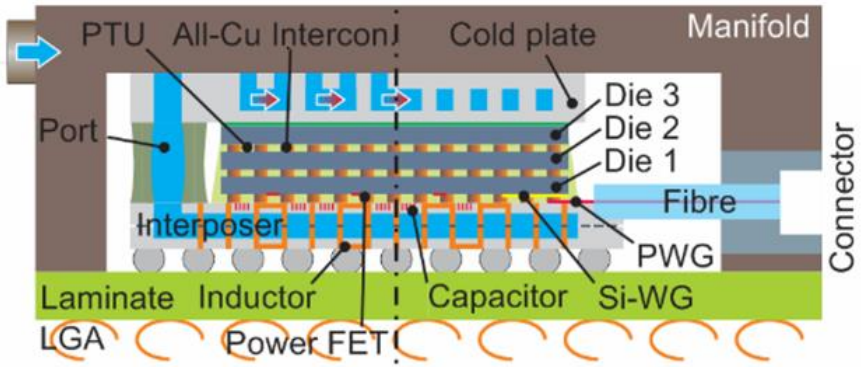
HPC SoCs can have up to 400 Voltage Rails for Power and On-Die thermal gradient management

Motivation for Granular Power at VRM/POL level





Source: Micron-IBM HMC development



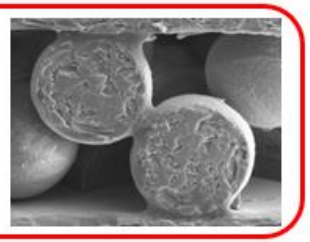
IBM HPC: 3-D Packaging Concepts

Array of Smaller Highly Integrated CPU Nodes

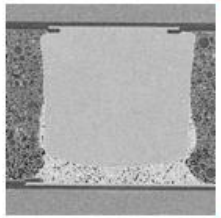
Scalable Packaging Platform

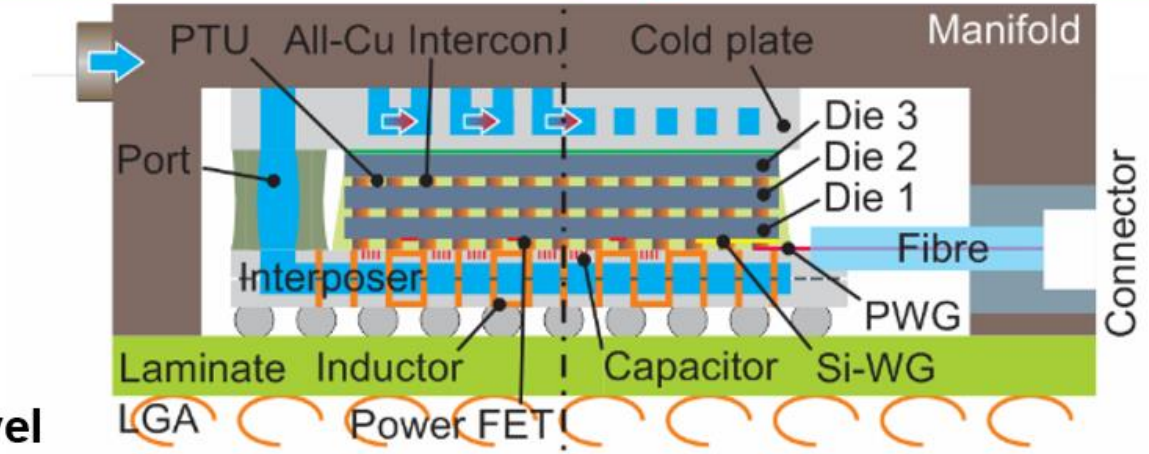
Chip Stack Level

Thermal Underfill
Percolating thermal underfill



Electrical Interconnects
All-copper interconnects



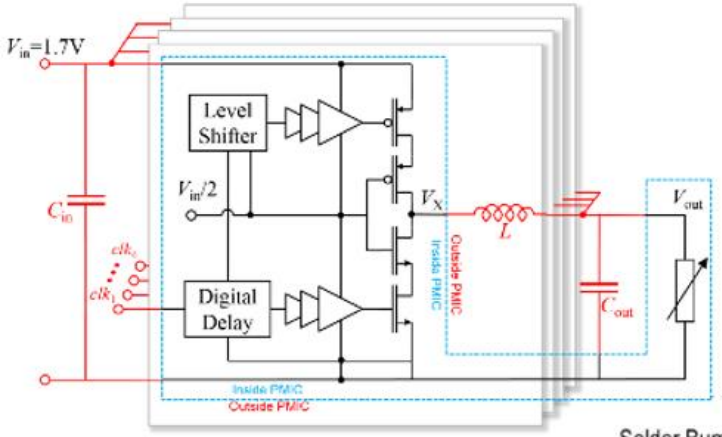


Interposer Level

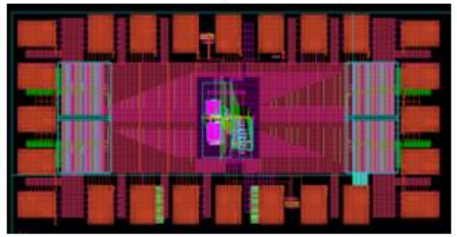
GaNonCMOS broad and holistic program focus on Switch Technology, Driver & Controller Circuits, Converter Topology, Packaging Technology, Integrated Magnetics and Embedded Substrates

Fully-Integrated Buck-Converter

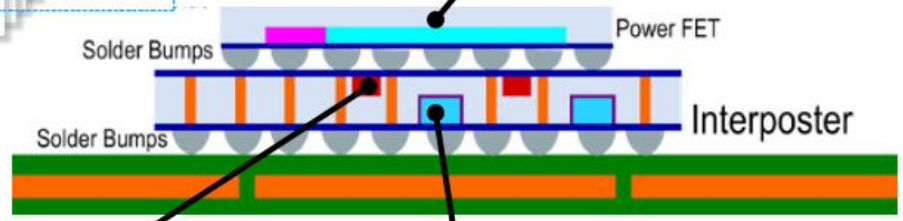
Buck-Converter Schematic



Power Management IC
14nm Globalfoundary Bulk
Power-FETs, control, load

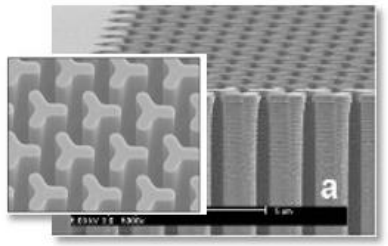


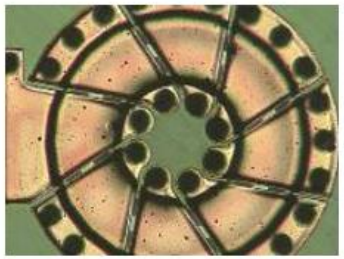
IBM



ipdia

Deep Trench Capacitors
MIMIM (250nF/mm^2)





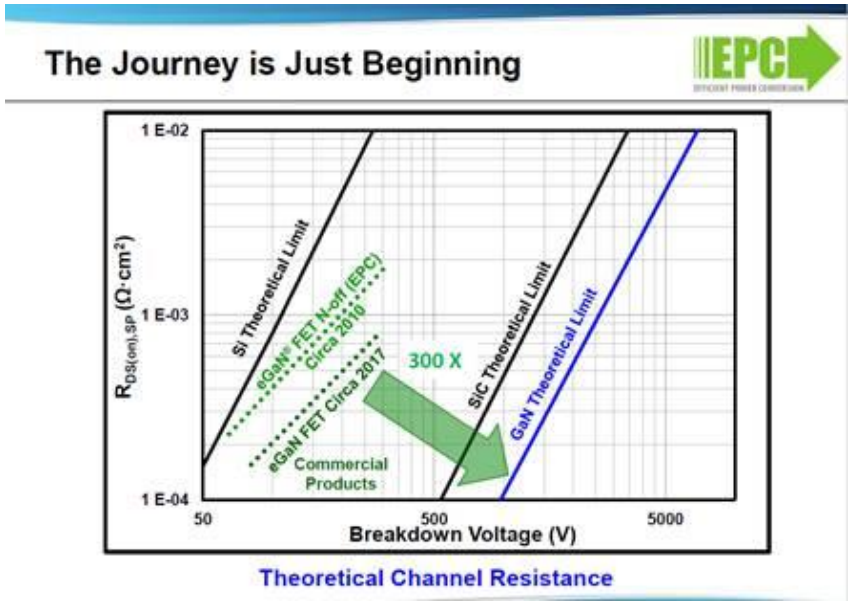
Inductors
TSV Inductors with magnetic core material

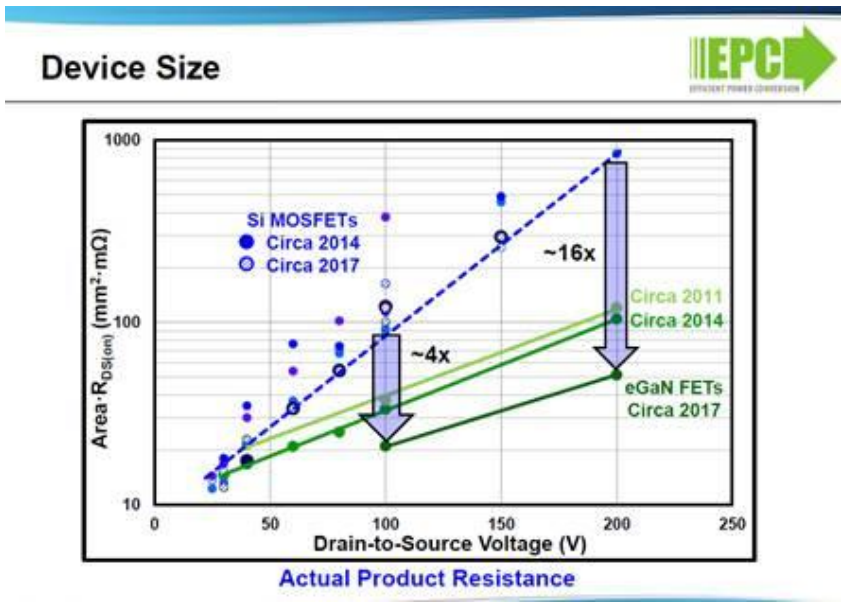
Tyndall National Institute

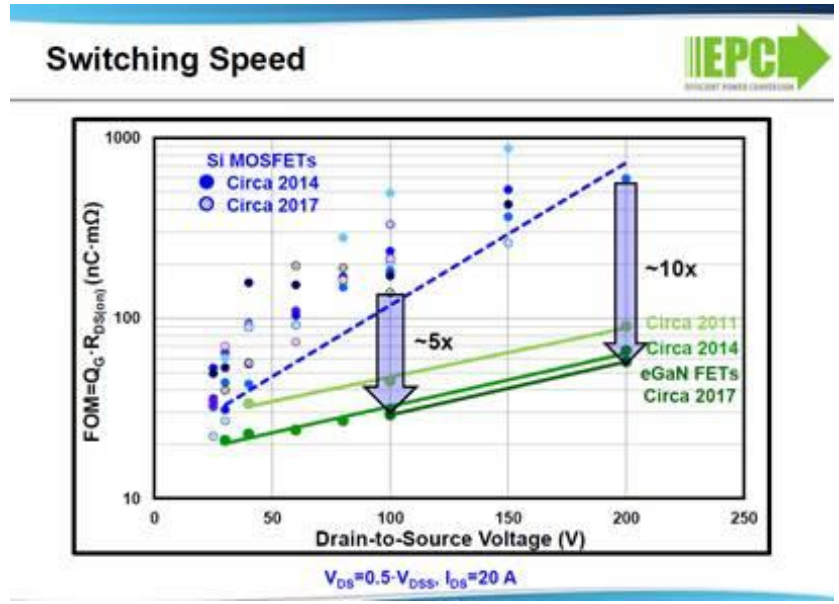
Initial research idea was to replicate the integration of the complete converter (as with earlier IBM 14nm PwrSoC) at 12V using the higher voltage and frequency capabilities of GaN.

This would require ~30X improvement in GaN switching FOM (Rdson.Egt from ~60 to ~2 mΩ.nJ) and hence proved not currently feasible

GaN Switch Performance vs Voltage Rating







Benchmark slides of EPC vs. Si presented by Alex. Lidow at the _Anwenderforum Leistungshalbleiter 2018 Munich

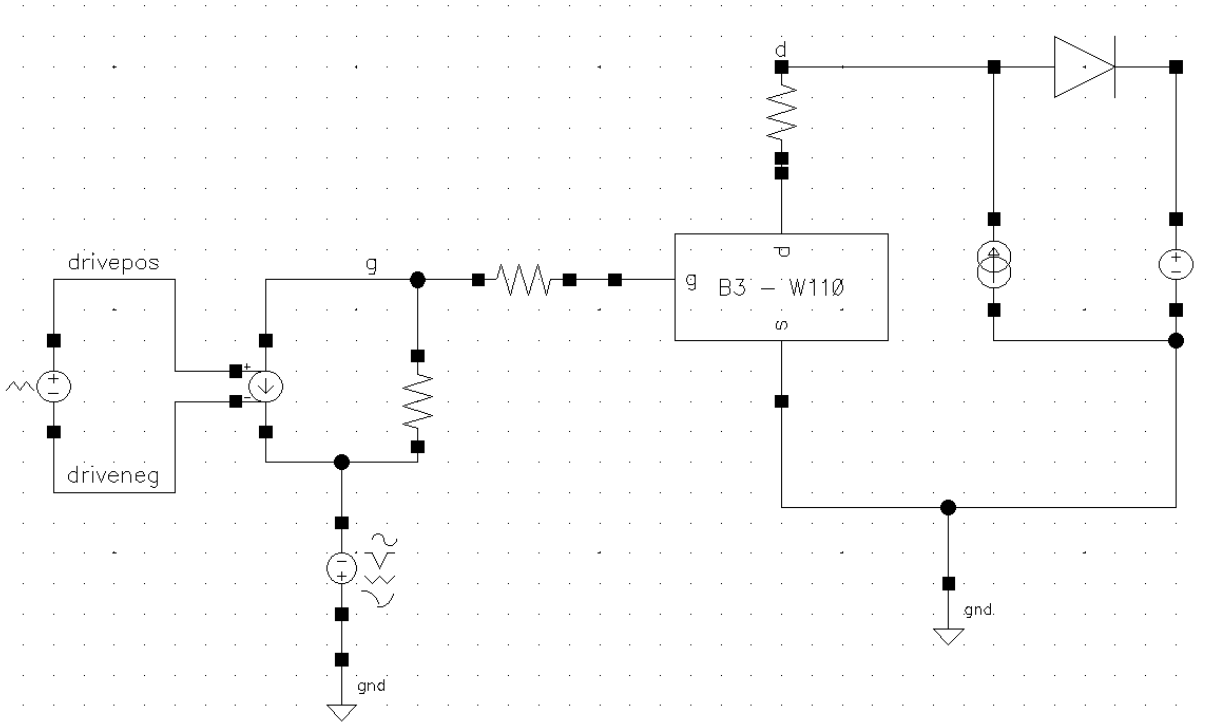
- GaNonCMOS Program explores < 25V switch rated applications
- Established commercial player – EPC
- IAF fabricating 100V and 25V devices for GaNonCMOS Program

Generally at higher voltages – GaN has very good advantage in Ciss, very low Qrr (particulary vs Super Junction) and reasonably good Coss

Tyndall Evaluation of IAF d-HEMT

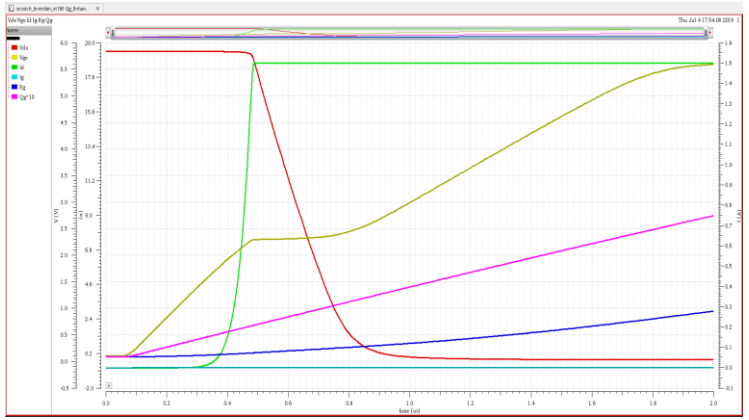
IAF Switch Performance vs COTS

- Simulated IAF supplied model for 25V B3, Adjusted W to 110mm to match R_{ON}
- Driving I_G ~490uA
- IAF d-HEMT from -4.4 to -0.45V
- EPC e-HEMT from 0 to 3.95V

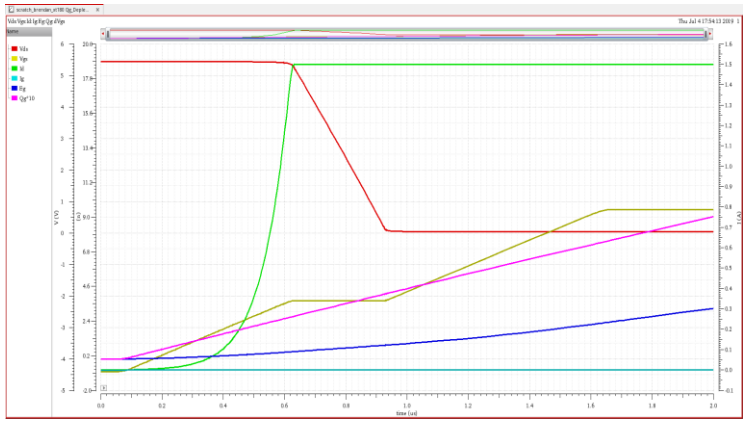


IAF Switching FOM Performance vs COTS EPC Device

- 25V IAF $R_{ON}.Q_{Gt}$ = 20 mΩ.nC
- 15V EPC2040 $R_{ON}.Q_{Gt}$ = 18 mΩ.nC



EPC20140
Ig = 490 uA
for 2us
VDS 6-0 V



IAF B3 W=110
Ig = 490 uA for
2us
VDS 6-0 V

IAF_B3_W110 (25V d-HEMT)	Qg to Miller Plateau Start	Qg to Miller Plateau End	Qg to Driver Voltage	R_{DS_on} (mΩ)	Ron.Qgt (mΩ.nC)
Simulation time (ns)	585	920	1375	@ -0.45V	
Qg (pC)	273	433	626	31.39	20
Egt (pJ)	475.3	934	1640		
EPC2040 (15V e-HEMT)	**Qg to Miller Plateau Start**	**Qg to Miller End**	**Qg to Driver Voltage**	**R_{DS_on} (mΩ)**	**Ron.Qgt (mΩ.nC)**
Simulation time (ns)	440	706	1250	@ 3.95V	
Qg (pC)	202	328	585	30.22	18
Egt (pJ)	256	550	1340		

Simulations Brendan O'Sullivan (PhD Student Tyndall)

Lateral MOSFET, Trench MOSFET and GaN HEMT are all currently similar @ 15-25V

Comment	Switch Part Number	Switch Reference	Switch Technology	Steady State Switch Voltage Rating [V]	Sp.RDSon Specific ON-resistance Die Only [mΩ.mm2]	QG.RDS FOM [mΩ.nC]
	EPC2023	http://epc-co.com/e	eGaN	30	13.915	20.00
	EPC2100	http://epc-co.com/e	eGaN	30	19.829	22.50
NEXFET - Lateral Channel (Low Qg, Qgd)	CSD16327q3	http://www.ti.com/l	TI NEXFET DISCRETE	25	20.625	20.46
NEXTPOWERS3	PSMN3R5-25MLD	http://assets.nexper	TRENCH.	25	18.800	32.71
XFAB 180nm xp018 process	23/25 nLDMOS			23	39.000	
	EPC2040	http://epc-co.com/e	E-HEMT	15	24.480	18.82
	BSZ0589NS	http://www.infineor	OptiMOS 5	30	22.902	22.88
	BSC0500NSI	http://www.infineor	OptiMOS 5	30	21.792	25.20
	BSC009NE2LS5I	http://www.infineor	OptiMOS 5	25	16.344	17.85
	CSD13202Q2	http://www.ti.com/l	TI NEXFET	12	12.188	38.25
	CSD13383F4	http://www.ti.com/l	TI FemtoFET	12	21.090	74.00
	CSD13380F3			12	23.814	57.33
Fraunhofer (Tyndall Simulation)	IAF (C4)		dHEMT	25	25.000	20.00

Lateral (LDMOS),
Trench MOSFET (VDMOS),
GaN HEMT

All currently offer somewhat similar performances at 25V.

Lateral MOSFET and GaN HEMT do have lower Q_G and Q_{GD} and allow 50% - 100% higher switching frequency

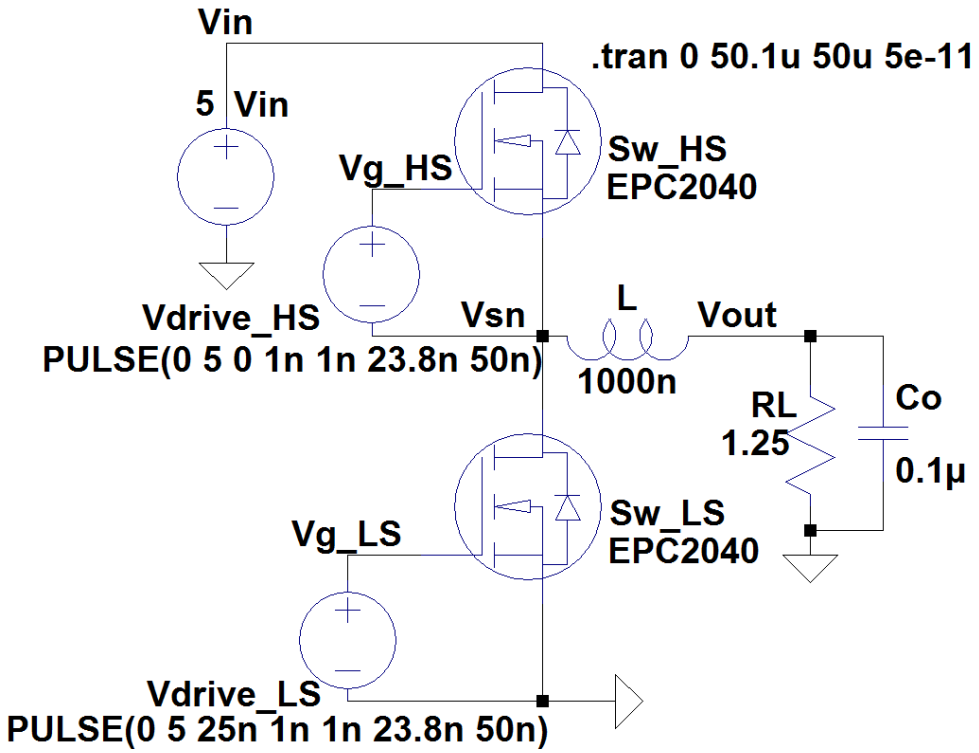
GaN HEMT has extremely low Reverse Recovery Charge

But silicon is very mature and GaN is only beginning its journey in improvement - ohmic-contact, sheet resistance, ohm-length, depletion length.

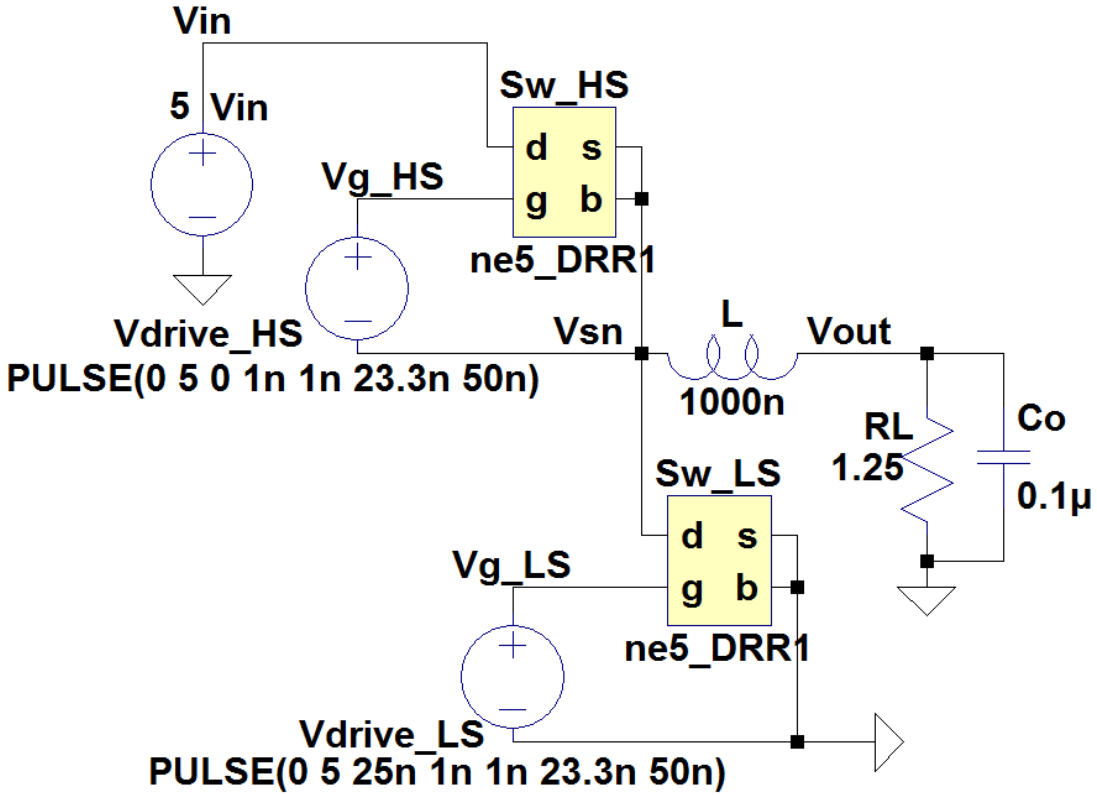
Evaluation of 15V EPC for 5V POL Application (versus 180nm CMOS)

EPC2040 (15V eHEMT) vs 180nm 5V CMOS (=R_{ON})

Both EPC2040 & 180nm 5V CMOS set for equal RON ~ 24mΩ.
W/L ratio of 80e-3/0.5e-6 for ne5

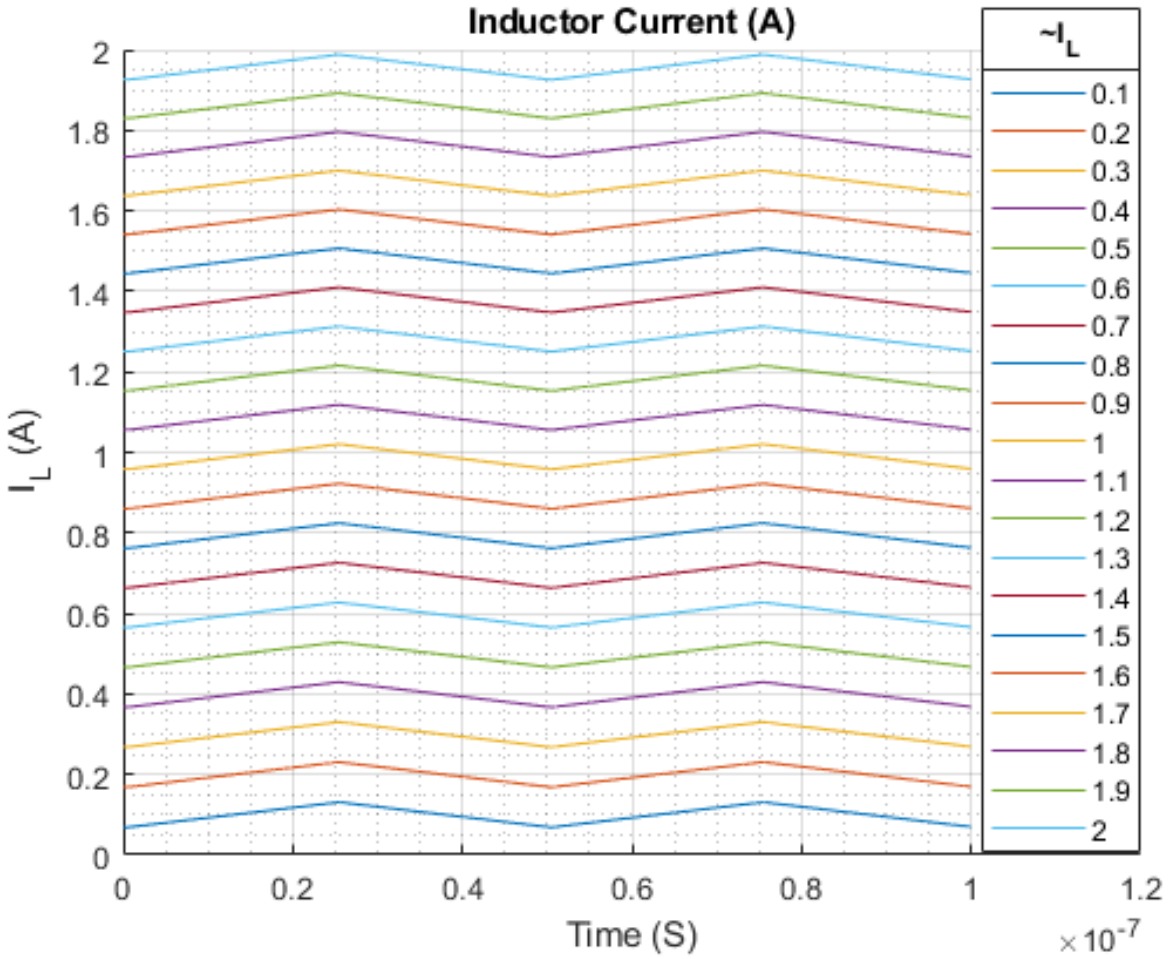


EPC



5V 180nm CMOS

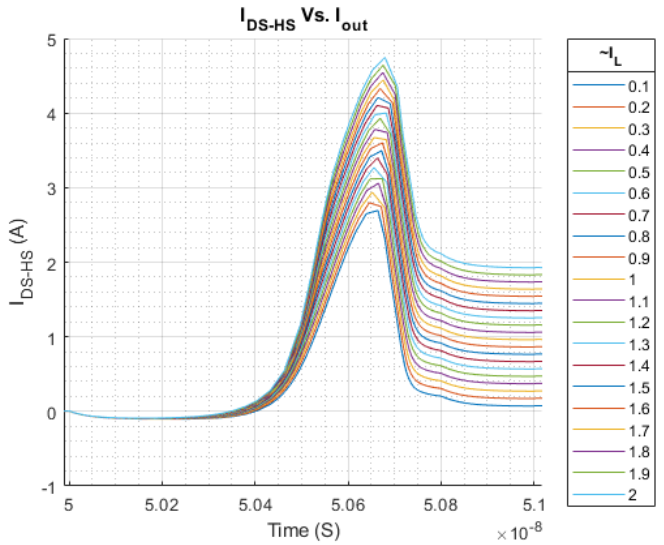
EPC2040 vs 180nm 5V CMOS (=R_{ON})

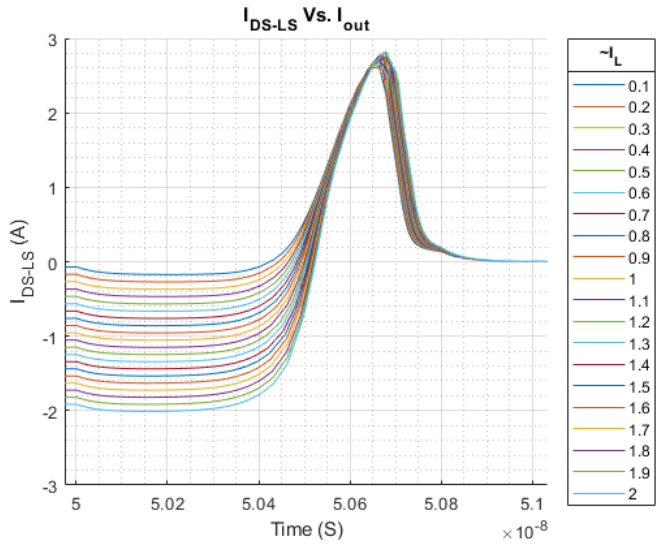


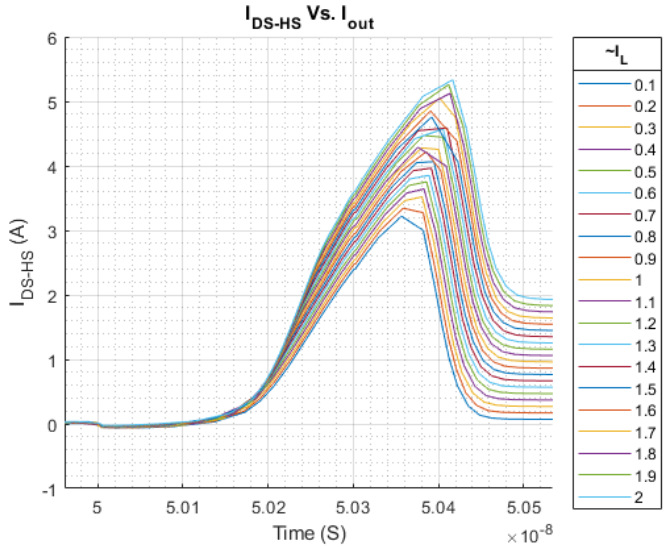
Sweeping Load Current
(Ripple Current ~0.0622A)

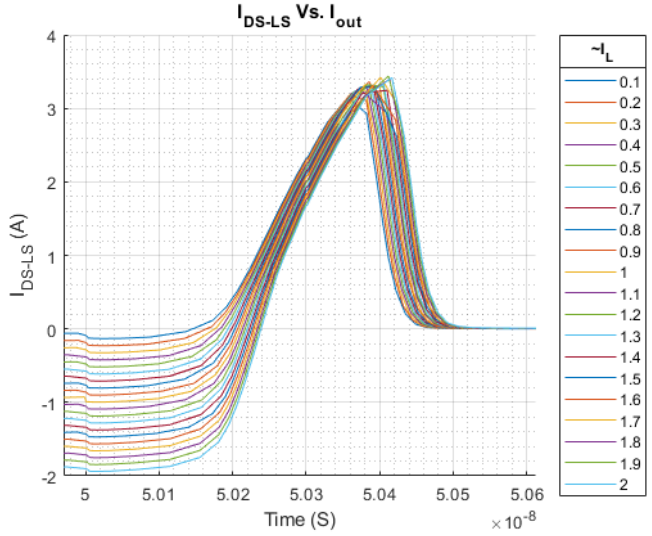
-to effectively sweep I_F for the body diode or 3rd quadrant conduction mechanism

EPC2040 vs 180nm 5V CMOS (=R_{ON})









15V eHEMT EPC2040

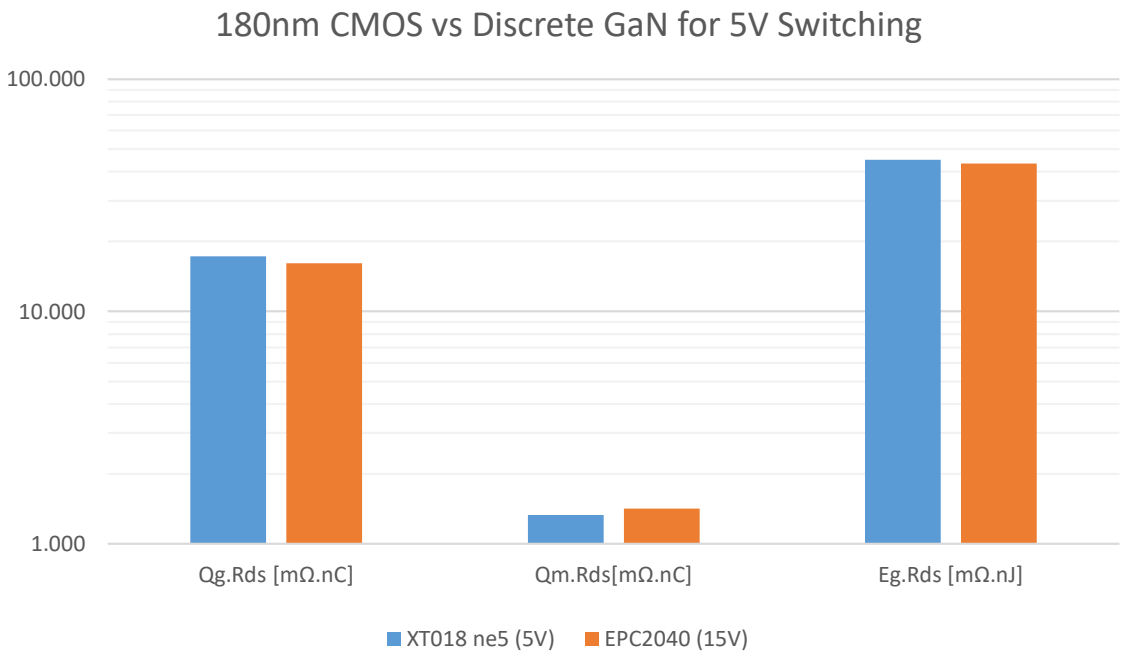
Comparable Coss – 15V GaN slightly better than 5V CMOS

180nm 5V CMOS

No significant Body Diode Reverse Recovery Issue for 5V Converter with ordinary bulk CMOS

Simulations Eoin Walsh (MSc.Eng. Tyndall)

Cadence Based Test Benches to Characterise Models for 5V CMOS vs 15V GaN eHEMT



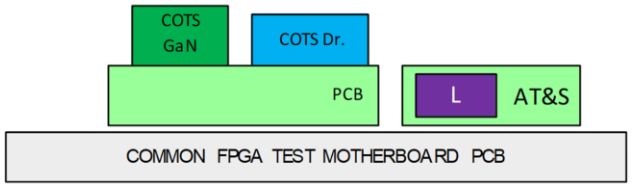
Values for 5V CMOS are for post layout parasitic extract (PEX)

- Simulations by Odhran Reidy, Tyndall

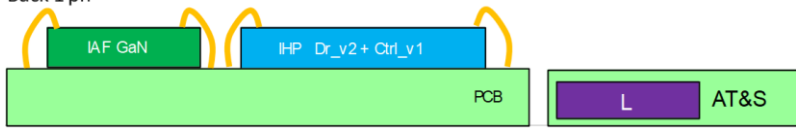
POL/VR Demonstrators

Open Loop POL PCB Level DEMONSTRATORS

12V to LV @2A
Buck 1 ph

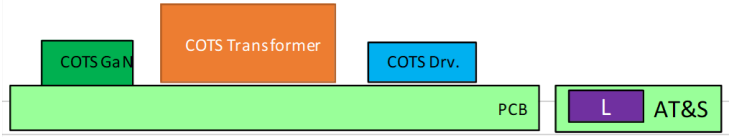


12V to LV @2A
Buck 1 ph

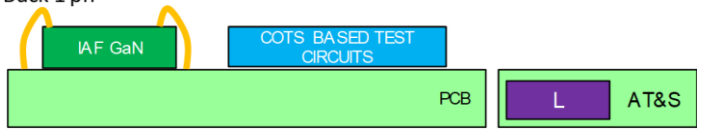


12V to LV @2A
Buck 1 ph

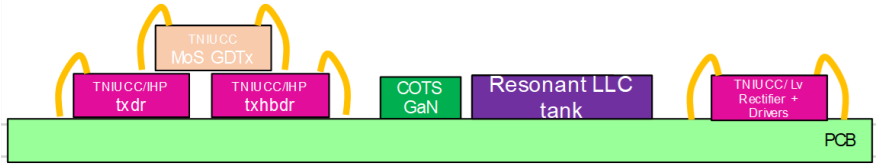
12V to LV @5A , 25V to 5V @ 5A
3-**L** (FCML) Buck 2 ph (5A)
Single and Coupled-L versions



12V to LV @2A
Buck 1 ph



12v to 1V5
10MHz LLC Converter

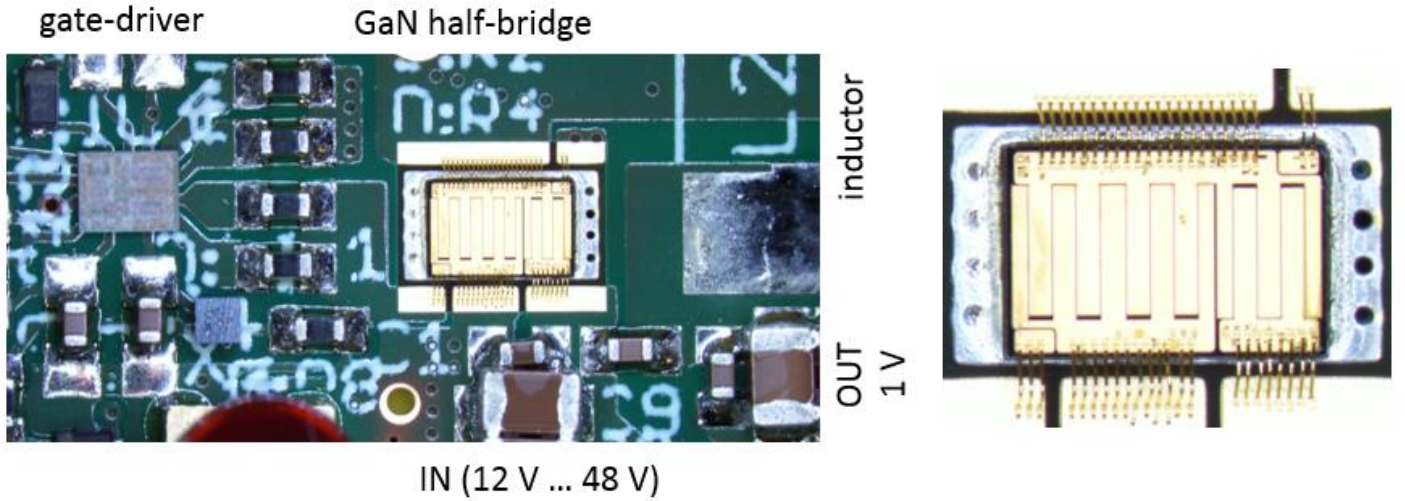


- POL to baseline with best COTS (EPC and Peregrine Driver)
- 3-L POL to further develop 4X reduction in Inductor and coupled-L
- Evaluate IAF 25V d-HEMT
- Evaluate IHP 25 MHz Controller/Driver Combo
- Prototype 10 MHz Resonant Converter

Monolithic Asymmetric Half Bridge

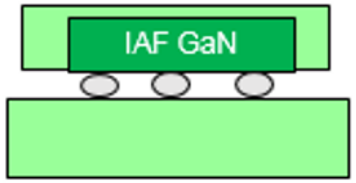
- 1 MHz
- IAF Asymmetric Half Bridge d-HEMT
- Inductor will degrade efficiency by further 5%
- Require > ~88% to have a viable solution
- Note capacitive couplings between phases for monolithic

24 – 1V POL results from ongoing Master's thesis Alexander Beeren

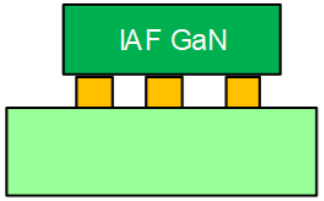


Stack Level Designs to be Evaluated

48V to 12V @4A
Buck 1 ph



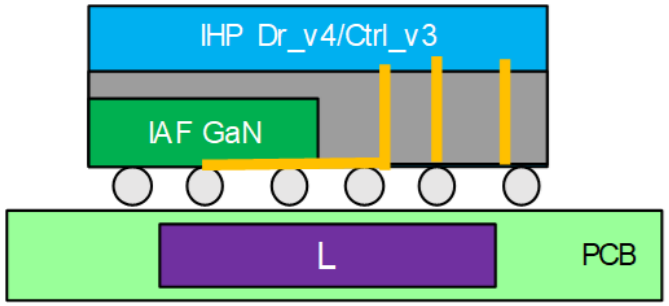
48V to 12V @4A
Buck 1 ph



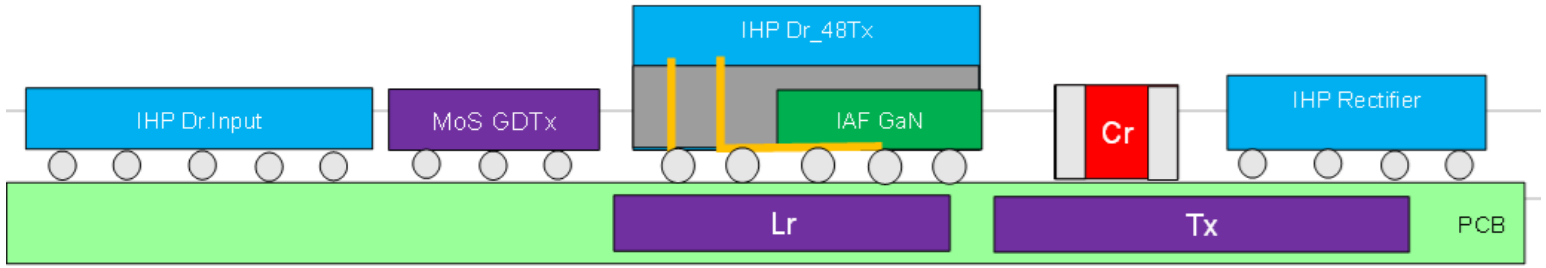
- **100V IAF switches with copper (125um thick) contacts and switch copper pattern design for compatibility with PCB embedding manufacturing process.**
- **Separate test board planned for design and build to cycle large embedded switch power dissipations and perform reliability trials**
- **Trial IBM Copper Pillar interconnect technology on discrete IAF switch, ahead of GaNonCMOS top level interconnect.**

Chip Scale Demonstrator Designs

12V to LV @2A
Buck 1 ph



48V to LV @4A
LLC 1 ph with MoS Tx Isolated GD CMOS (TNIUCC)

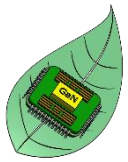


12V to 1V is the first target Chip Scale Demonstrator

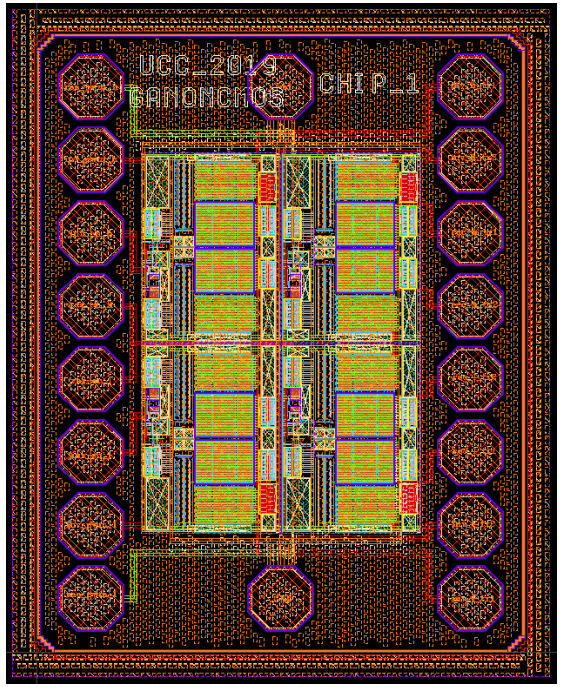
Resonant LLC Converter is a stretch goal and will probably only get to Design drawing stage. The idea is to push our GaN switching frequency to 10MHz and achieve greater than 90%. Also doing a PCB based version.

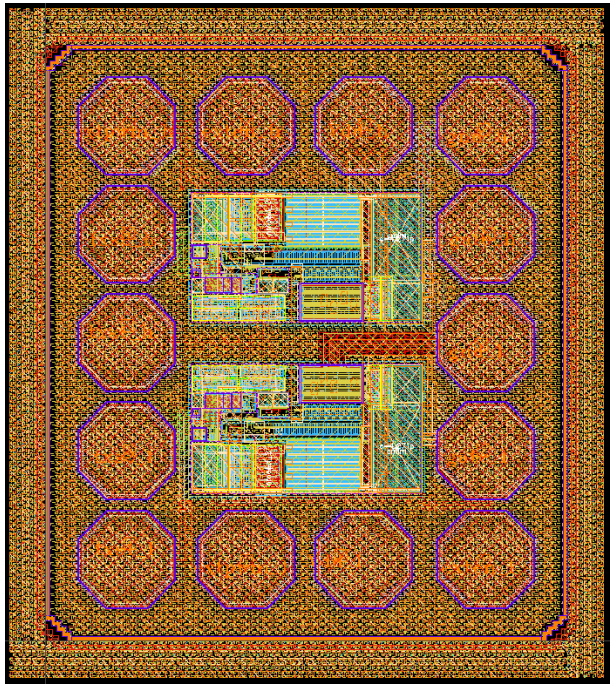
PCB Demo 4 & Chip Level Stretch Demo 2

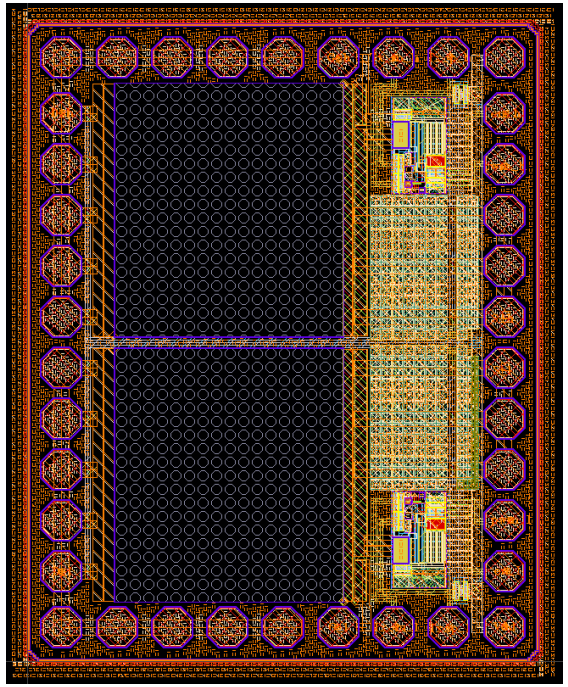
- High frequency GaN switch application requires integrated gate driver
- High side switches require isolated gate drive.
- Magnetic coupled power and signal creates the best possible solution
  - The alternative is capacitive. Capacitive coupled gate driver power creates common mode transient injection due to high dV/dt on switching nodes (100-500V/ns).
- TNIUCC and IHP, in partnership, taped out, a 2-Chip chip-set to validate Magnetics–on-Silicon (MoS) gate driver isolation transformer – this can be the basis of a *smart CMOS gate driver for* GaN switches.
- TNIUCC taped out a 3rd IC to create a low voltage CMOS synchronous rectifier set for 4A output isolated or high frequency resonant point-of-load (POL) converter (Will suit 12, 24, 48V POL)



Transformer (signal) Isolated Gate Drivers and LV Synchronous Rectifiers (3-chip set) for 10-30MHz converter (ex. Isolated LLC or resonant POL)





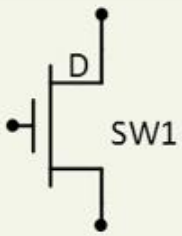
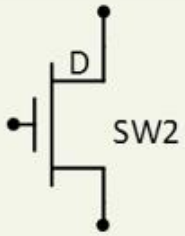
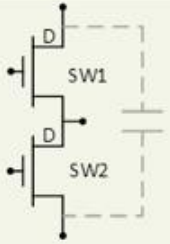
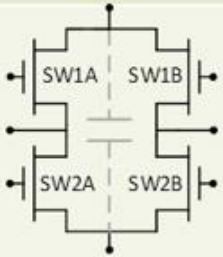
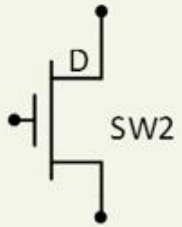
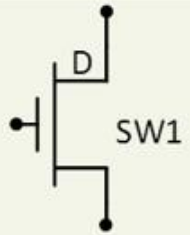


0_txdr
signal coupling primary driver
10Vns *50nH 1:1 Magnetics-on-Silicon Gate Drive Transformer (MoS GD Tx)*
600 X 762.8 µm

0_txhbdr
signal recovery secondary driver for 100pF load (GaN HEMT)
428 X 490 µm

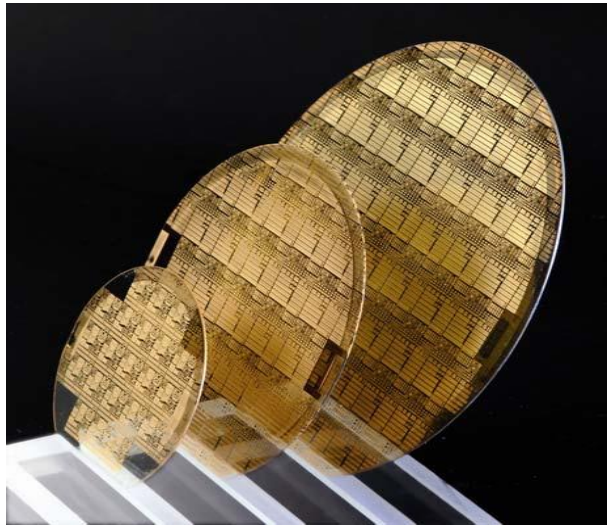
0_lvdswdr
signal recovery secondary driver for 3V3 synchronous switches
1.0028 X 1.25096 mm

A variety of 25V and 100V Switches and Monolithic Bridges are being developed by Fraunhofer IAF

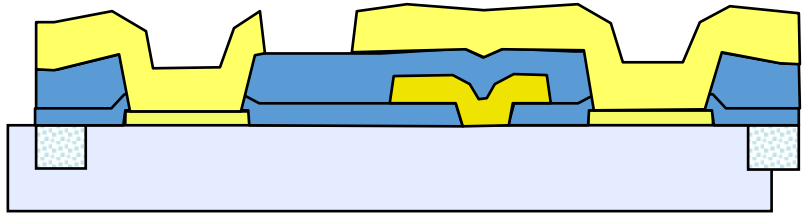
25V GaN Prototype Device Plan (Design Iteration 1)					100V GaN Prototype Plan (Design Iteration 1)	
Name	**SW1**	**SW2**	**HB1**	**HB2**	**SW4**	**SW5**
R_{ON} (mΩ)	HEMT- SW1: R_{ON} = 28 mΩ	HEMT- SW2: R_{ON} = 11 mΩ	HEMT- SW1: 28 mΩ HEMT- SW2: 11 mΩ	HEMT- SW1A: 28 mΩ HEMT- SW2A: 11 mΩ HEMT- SW1B: 28 mΩ HEMT- SW2B: 11 mΩ	HEMT- SW4: R_{ON} = 500 mΩ	HEMT- SW5: R_{ON} = 20 mΩ
V_{BR} (Steady State)	22	22	22	22	80	80
V_{BR} (100ms)	28	28	28	28	100	100
$I_{NOMINAL(DC)}$	0.5	2	0.5,2	0.5,2	0.5	10
I_{PEAK}	3	3	3,3	3,3	3	25
PHASE COUNT	-	-	1	2		
Schematic (Monolithic) Layout to facilitate low inductance loops through MLCC and Gate Drivers Circuits.						

Also creating some which will be appropriate for Multi-Level

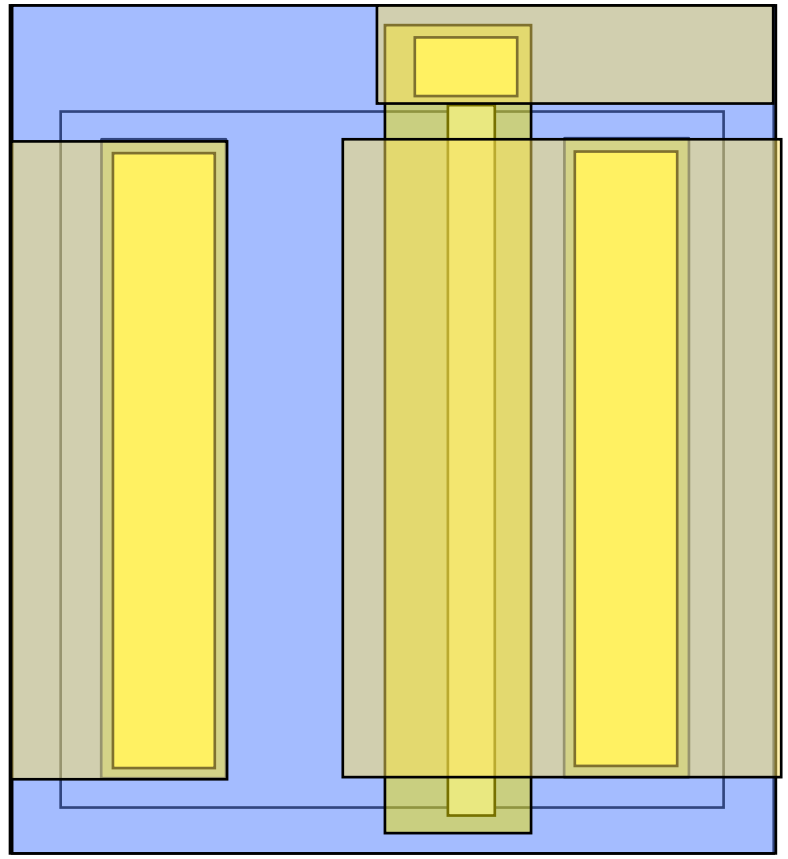
GaN/ AlGaN HEMT - Final Interconnect Stages of Fabrication



Interconnection metal → Ti/Pt/Au
Source shield



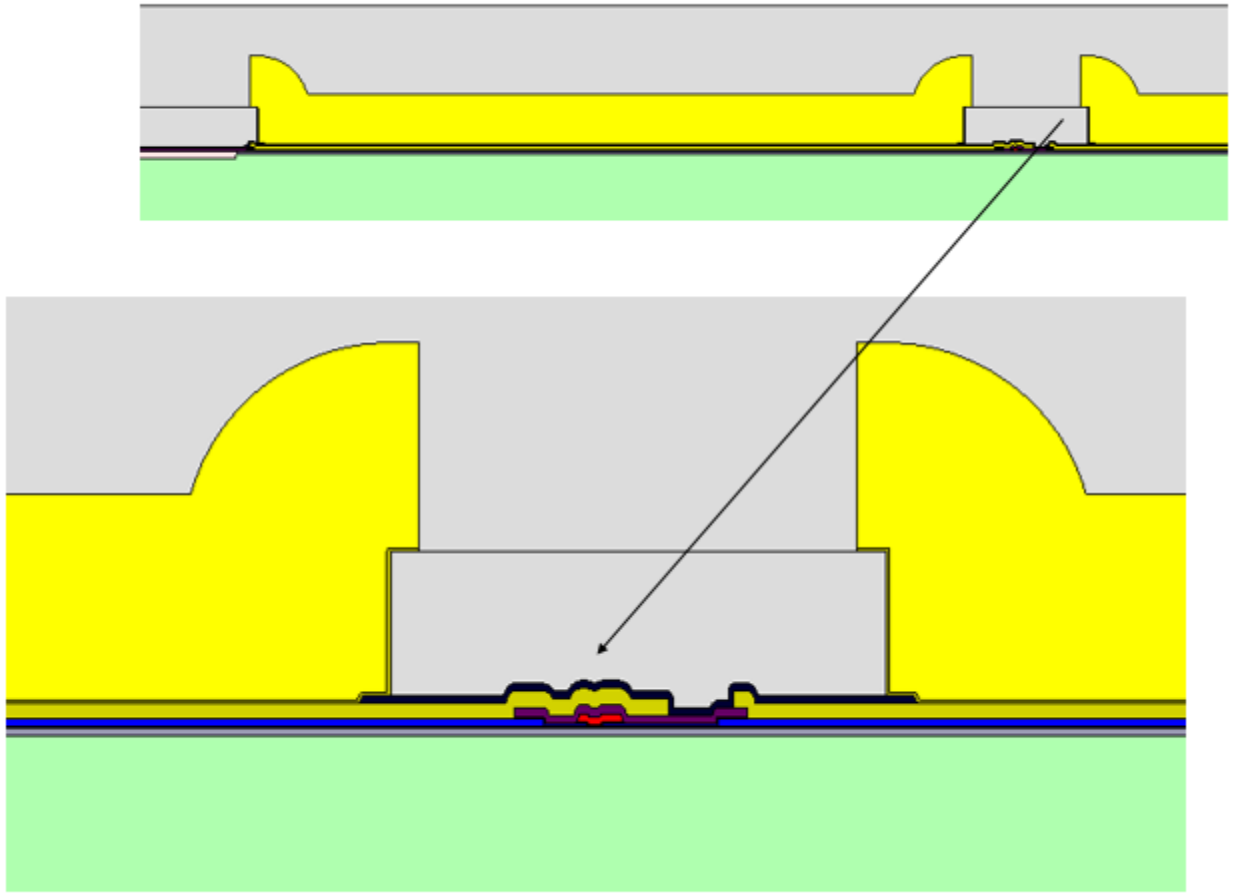
Ohmic contacts → Ti/Al/Ni/Au
Device isolation by implantation
NiAu Gate
SiN passivation stages
Ti/Pt/Au Source Shield & Interconnect



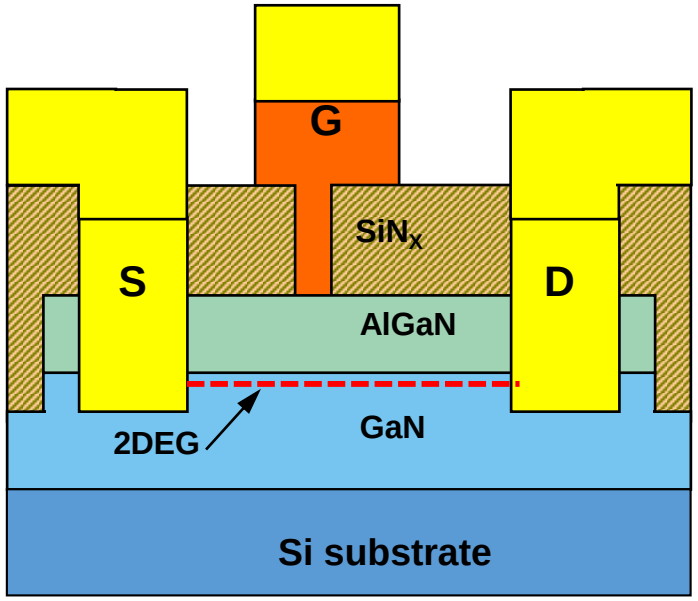
F.Benkhelifa, W.Pletschen; 04.05.2009

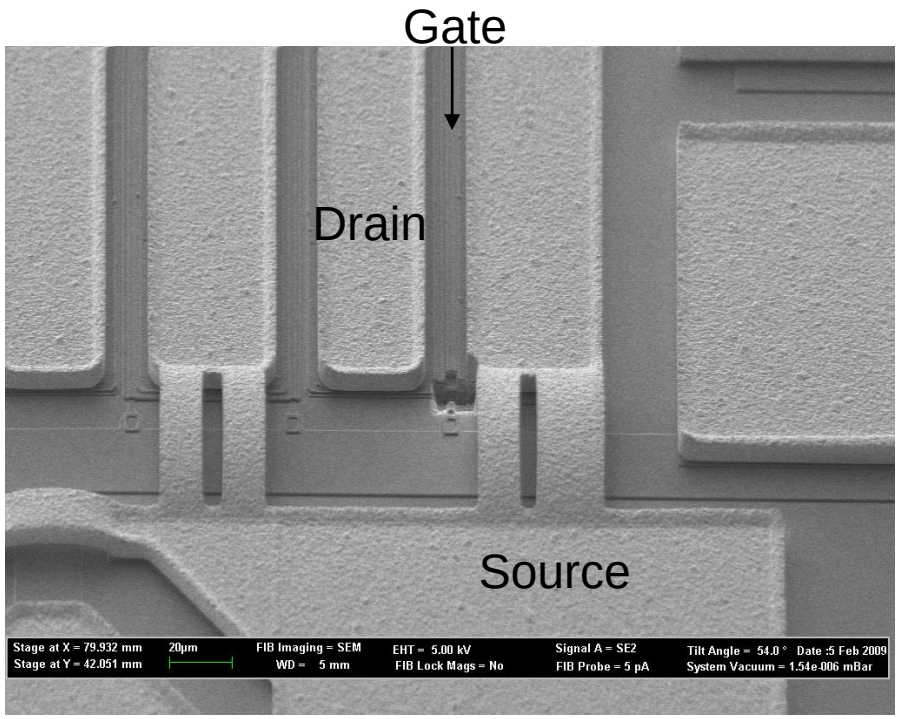
Final Passivation Opening and Copper Plating

5 um Copper Plating

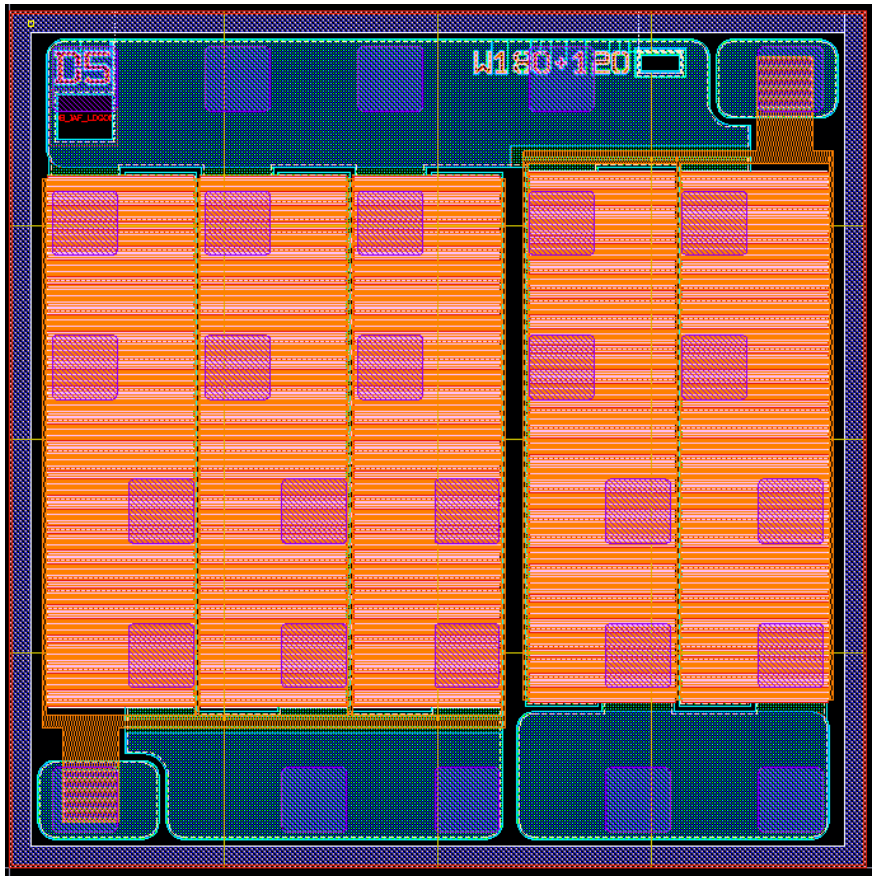


AlGaN/GaN High Electron Mobility Transistor





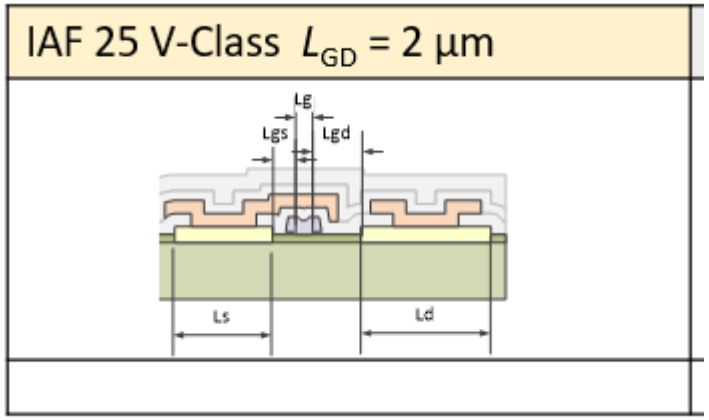
25V Asymmetric Monolithic Half Bridge

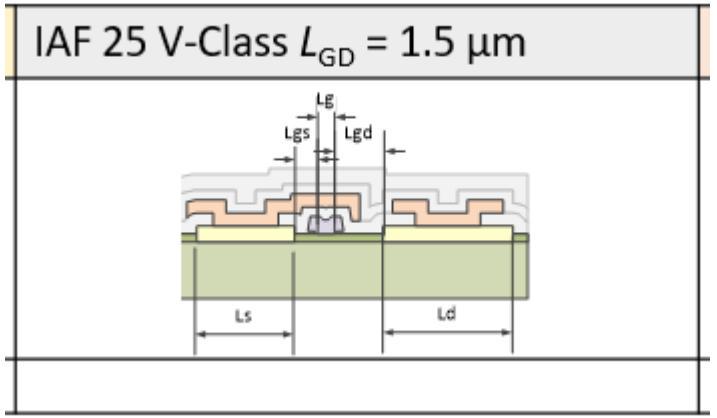


Higher Step Down Ratio means that greater size asymmetry will be required.

- 12V to 1V => ~ 1 to 5 size ratio top to bottom switch ratio.

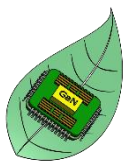
Testing a range of design “technology push”



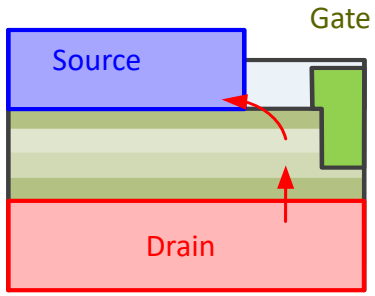


F.Benkhelifa, W.Pletschen; 04.05.2009

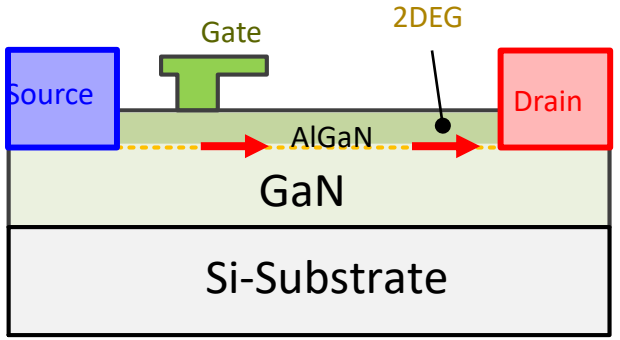
PCB Embedding Technology

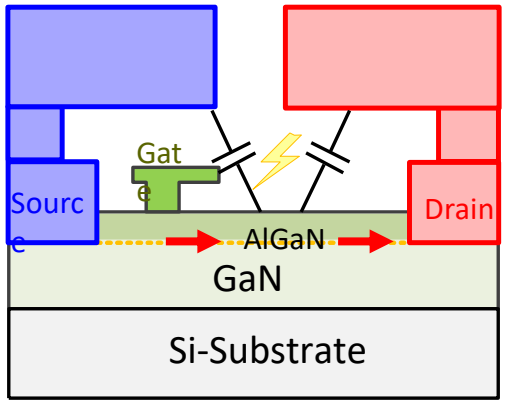


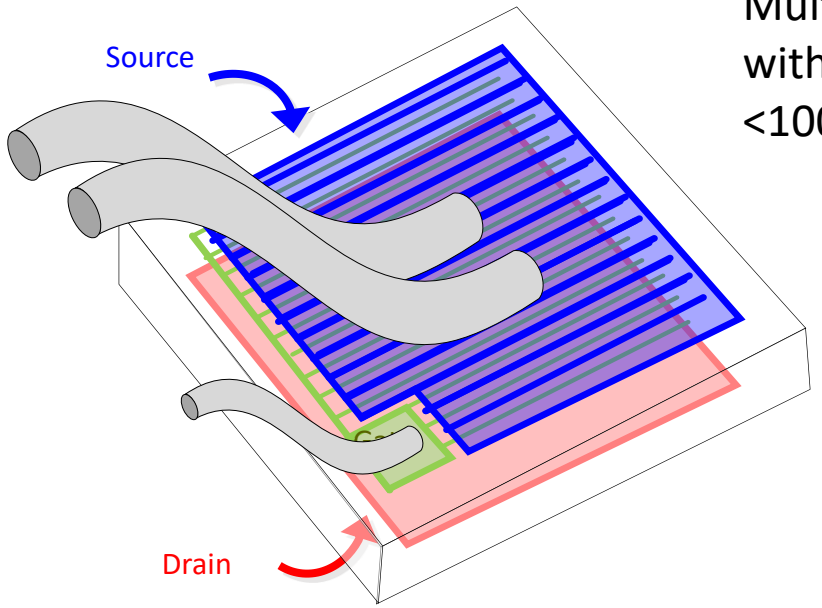
Vertical – Power Transistor (Si, SiC)



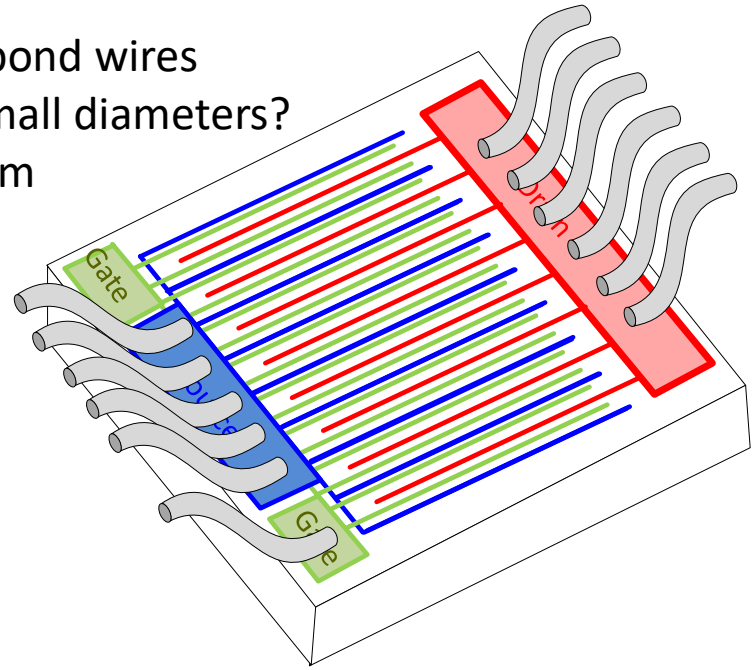
Lateral – GaN-on-Si Transistor

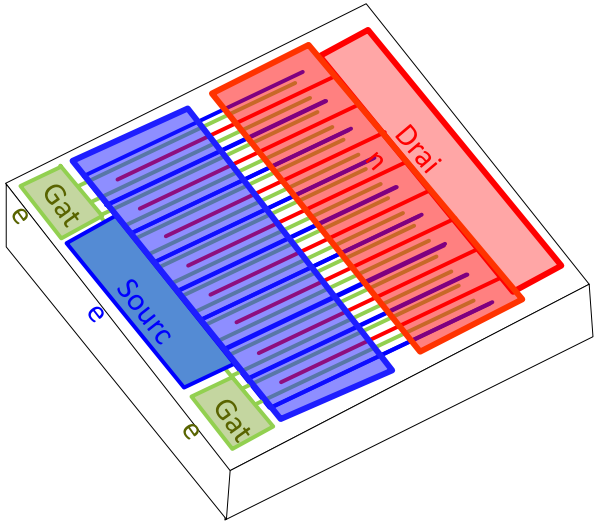




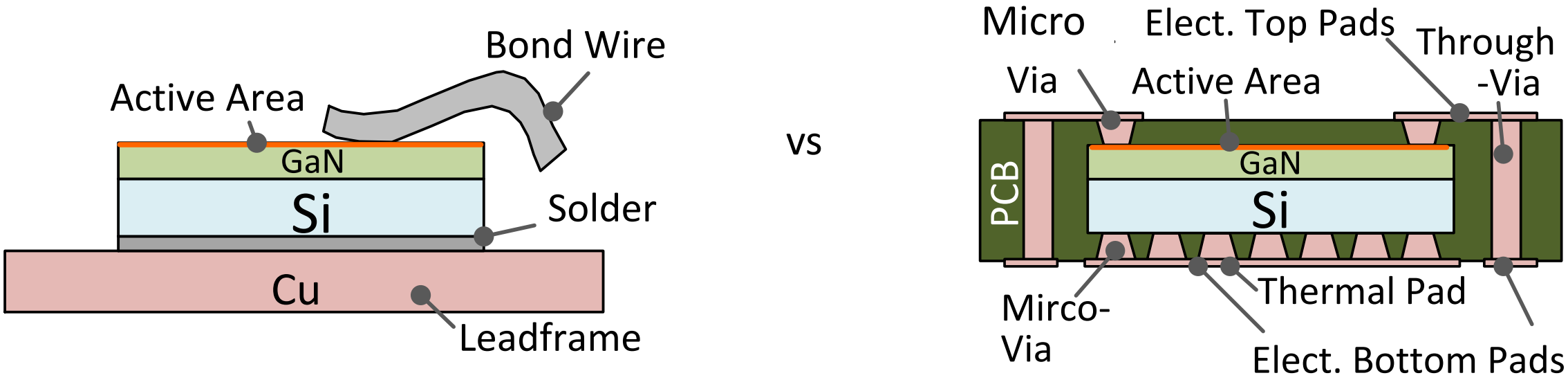


Multi-bond wires
with small diameters?
<100 µm





PCB Embedding



PCB-Embedding for GaN-on-Si Power Devices and Ics – CIPS 2018, R.Reiner et al.

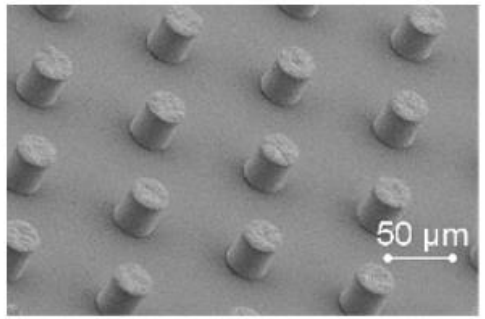
- shows interconnect inductances LD and LS ~ 1nH (by comparison 1nH/mm for bond wire solutions)

- shows thermal performance < 1K/W achievable with large diameter micro-vias

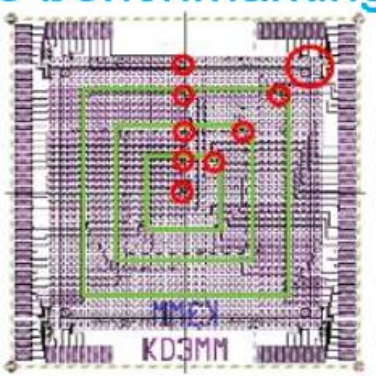
GaN-on-CMOS working to improve with heavy Cu devices contacts and patterns to match PCB manufacturing technology.

All-Copper Interconnects … performance benchmarking

Test Chip

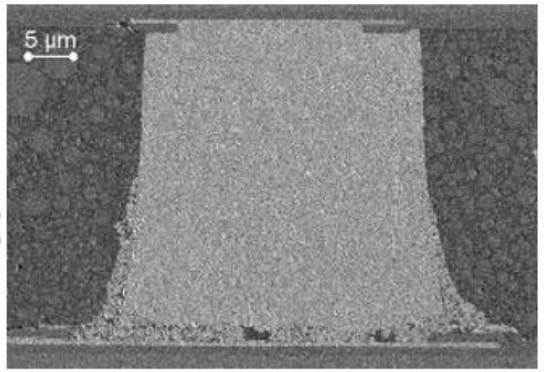


Pillar Height: 40 µm
Pillar Diameter: 30 µm
Pillar Pitch: 100 µm
Chip Size : 8x8 mm²

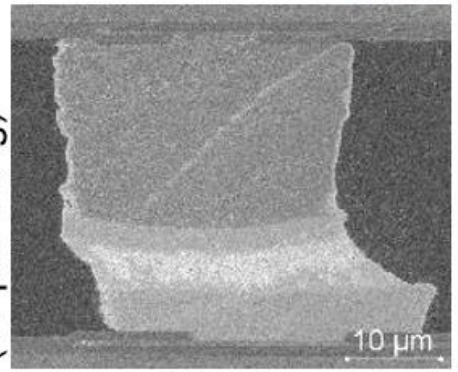


Courtesy SINTEF

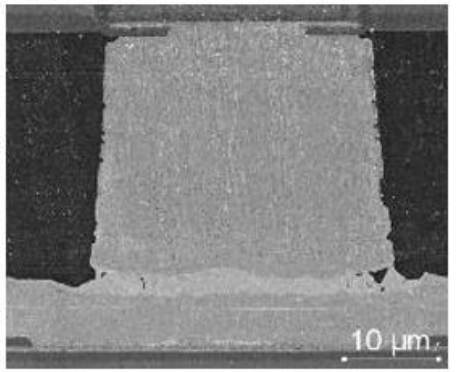
All-Copper



Solder (13 µm SnAg)



Fully IMC (6 µm SnAg)



Parameter	All-Cu	Solder	Fully IMC
Bonding temperature	200 °C	265 °C	265 °C
Bonding pressure	0 N	20 N	50 N
Interconnect resistance	1.7 ± 0.5 mΩ	3.1 ± 1.0 mΩ	1.3 ± 0.7 mΩ
Shear strength	19 ± 5 MPa	75 ± 7 MPa	65 ± 15 MPa

🕮 Zurcher, ECTC, 2016

All Copper – No brittle inter-metallics

Low Processing Temperature

CMOS Gate Driver Development

Design of Driver IC Version 2

Relaxed design due to new GaN switches

- Voff ≈ -3.5 V →

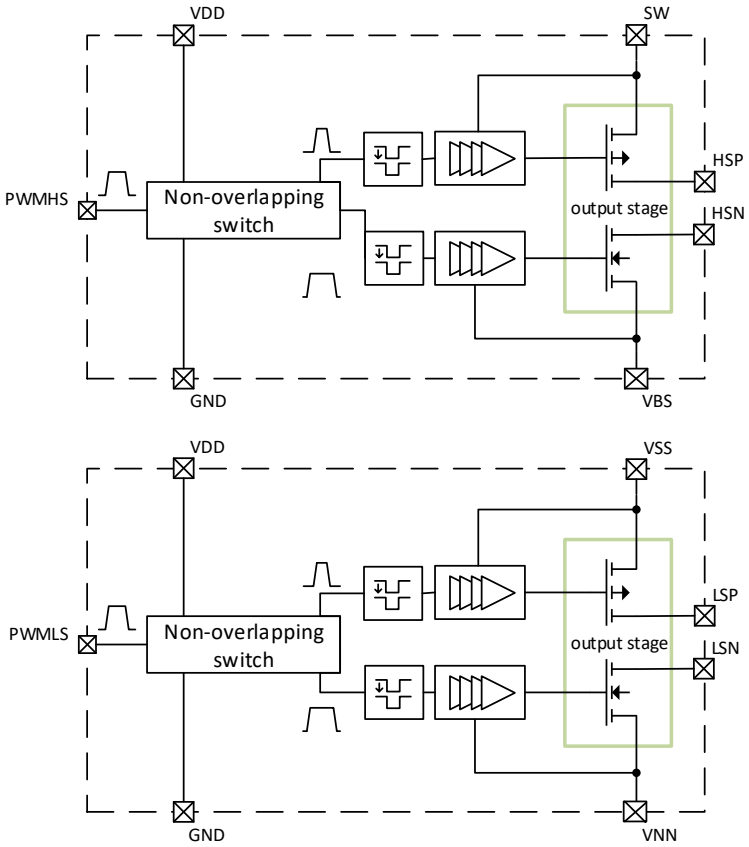
New level shifter circuit

- Galvanically isolated up to 25 V
- Adaptable to some hundreds of volts

Optimized switching transitions

- Adjusted to minimum losses
- 2 A peak output currents

Working from 1 to 30 MHz



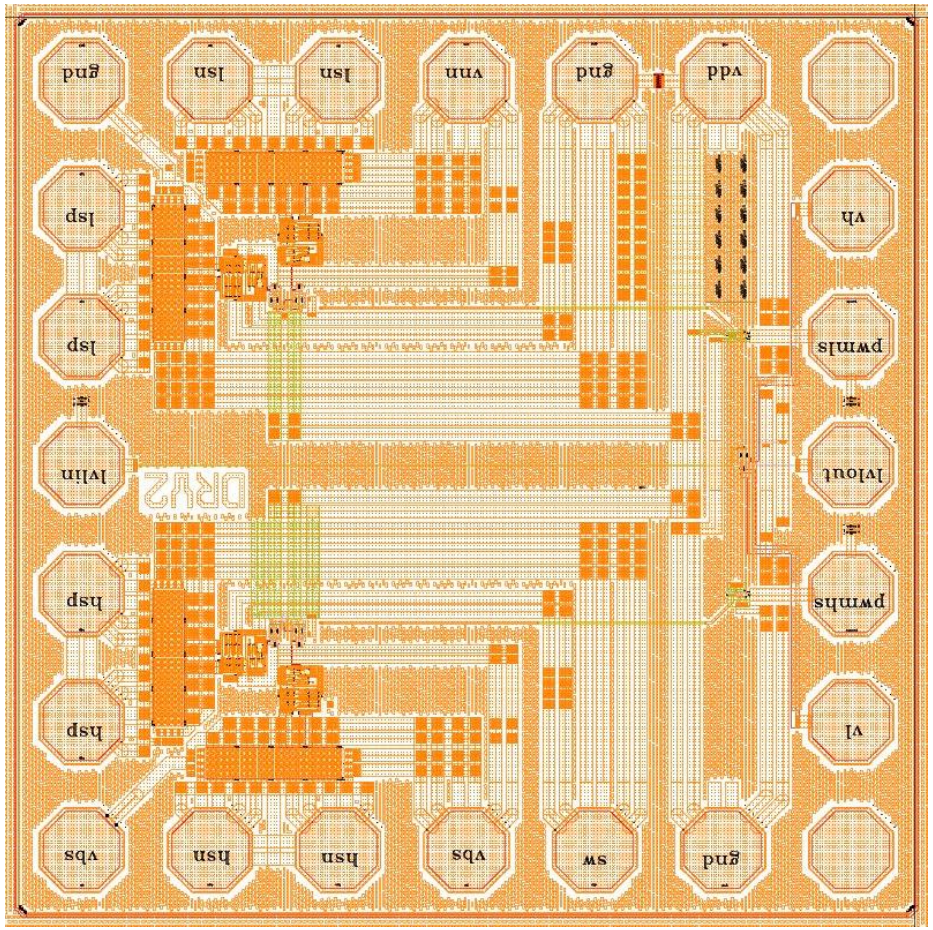
Galvanically Isolated Driver IC

Building blocks

- Half-bridge driver
- IHP and Peregrine Driver driving 1nF.
- 66.7% rise time for 3V3 input pulse:
  - IHP – 1.798nS,
  - PD – 2.79nS
- High side branch with bootstrapped supply
- Isolated domains
- 200 µm octagonal pads as of v1

Taped out chip

- Taped out: Aug 29 2018
- Wafer out : beginning of 2019
- Area: 2.1 x 2.1 mm², pad limited



Passive Components
Inductor(s) and Capacitors

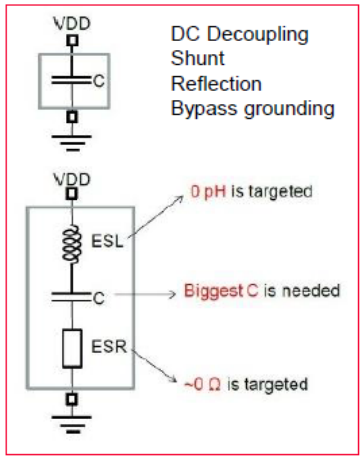
Silicon Capacitors for High Density Solution

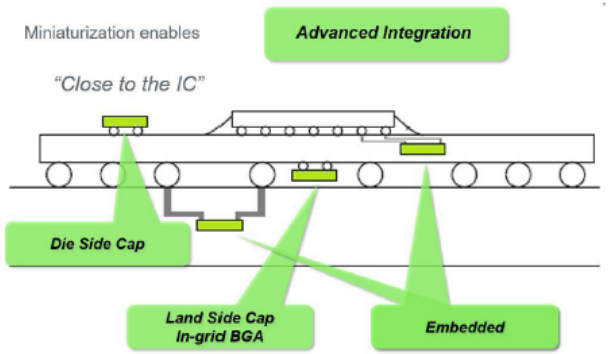
Low Profile Integrated Silicon Capacitors Tailored for power supply on chip

muRata INNOVATOR IN ELECTRONICS

Ultra Low ESL Silicon capacitor with:

- **World record of 500 nF/mm²** in Silicon, 470 nF in ultra compact 0404 form factor
- Ultra-low ESL (< 20 pH) and ESR (< 50 mΩ)
- <100 µm thickness
- Mechanical robustness of silicon during assembly



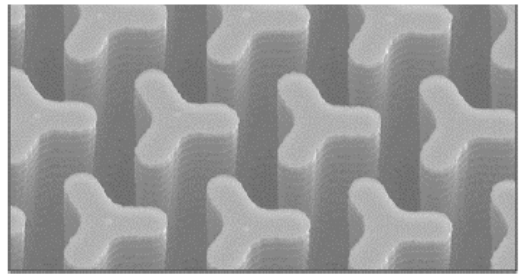


Market description	- Electronics for Power and Signal integrity
Typical use cases	- High speed IC - Power distribution network - Application processors in smartphone
Key challenges faced	- Space constraint - Low ESL - BGA pitch size
Market drivers and trends	- Need ultra low ESL capacitor in ultra low profile - Need to decrease the Power Delivery Network impedance

13 May 2019 6

Murata-IPDiA

3D:
We have invented a unique technology based on **3D structures**.
These 3D structures enable unprecedent **integration** and **miniaturization** of capacitors.



ESL provides necessary ripple advantage

High SRF – 100's MHz

GaN-on-CMOS Magnetic Materials & Device Design

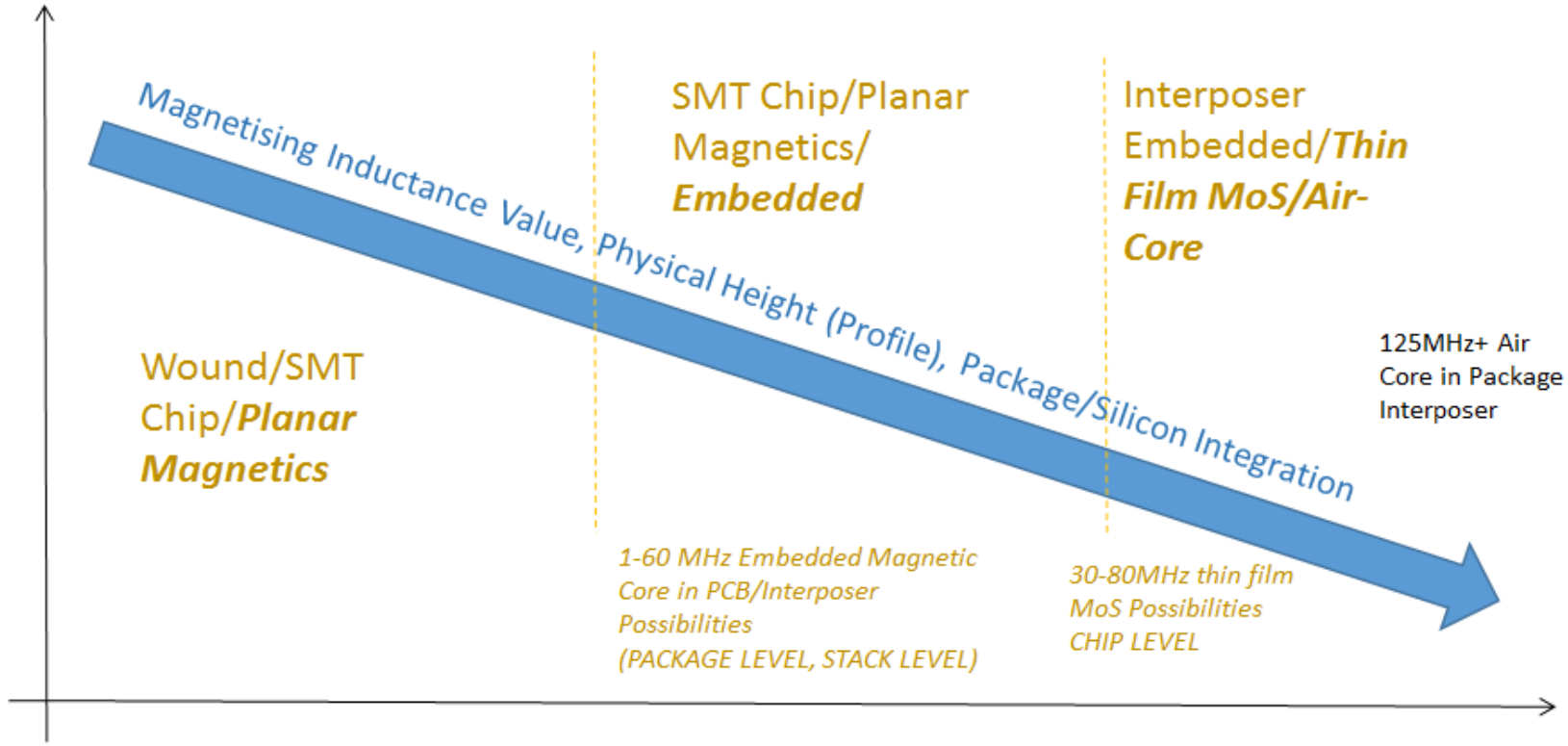
- The POL inductor is by far and away the largest component when in low profile format 5-15 X semiconductor size at 1-2MHz

- => Change topology to Multi-Level (3-L for 4X reduced L value) and push switching frequency
  - Inverse Phase coupling arrangements cancel DC field and may give steady state ripple (L-value) advantage. Multi-Level helps by extending Duty (optimum coupling values) for Low Voltage POL

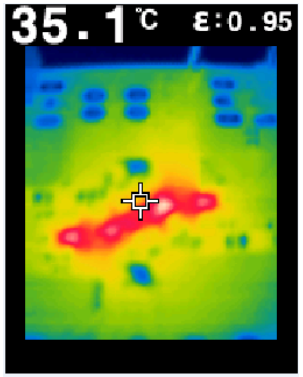
- Searching and Qualifying COTs materials for Embedded PCB Applications – Co-operation AT&S

- Tyndall is developing new multi-laminate thin film (plated and sputtered) PCB embeddable magnetic cores
- Planar Embedded with 300-500 um Cores are most appropriate for 1-10MHz low profile GaNonCMOS POL. They can have low DCR with AT&S thicker Cu.

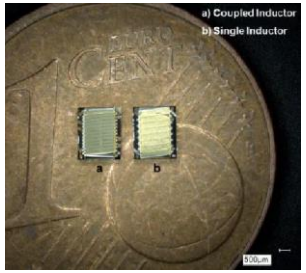
Magnetic Component Technology based on Peak Q Frequency

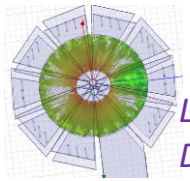


** A base converter topology refers to a fundamental mainstream topology, such as Buck Converter. Derivative topologies such as Multi-Level-Buck will allow L-value reduction which may allow more integrated inductor assembly technology at a lower switching frequency.*



White-hot regions are CMOS Gate Drivers and GaN switches at 30MHz. 50 nH MoS Inductor does not appear on heat map.





Low DCR

High Q_{AC}

Tyndall designed and fabricated world's highest Q **MoS** inductor at 30MHz for on-chip power conversion
< 45um height.

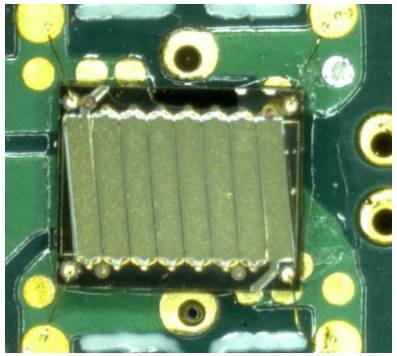
Magnetics-on-Silicon (MoS) thin film Gate Driver Isolation Transformer

Is being designed for GaN-on-CMOS Smart Driver Application

Thin film solenoidal and Racetrack Constructions - 50 µm Profile

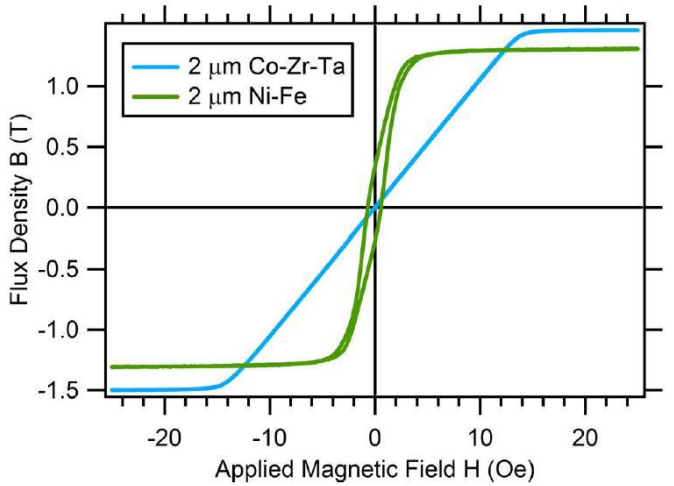
<<10 V.ns

~ 1mm²



Based on highest Q thin film MoS by Tyndall as reported at IEEE PwrSoC 2019

MoS step improvement in mid. 2000's



Donald S. Gardner et al. (INTEL)
Review of On-Chip Inductor Structures With Magnetic Films
IEEE TRANSACTIONS ON MAGNETICS, VOL. 45, NO. 10, OCTOBER 2009

GaNonCMOS Embedded Magnetics will extend this type of analysis to Low Profile Magnetics (PCB Embedded)

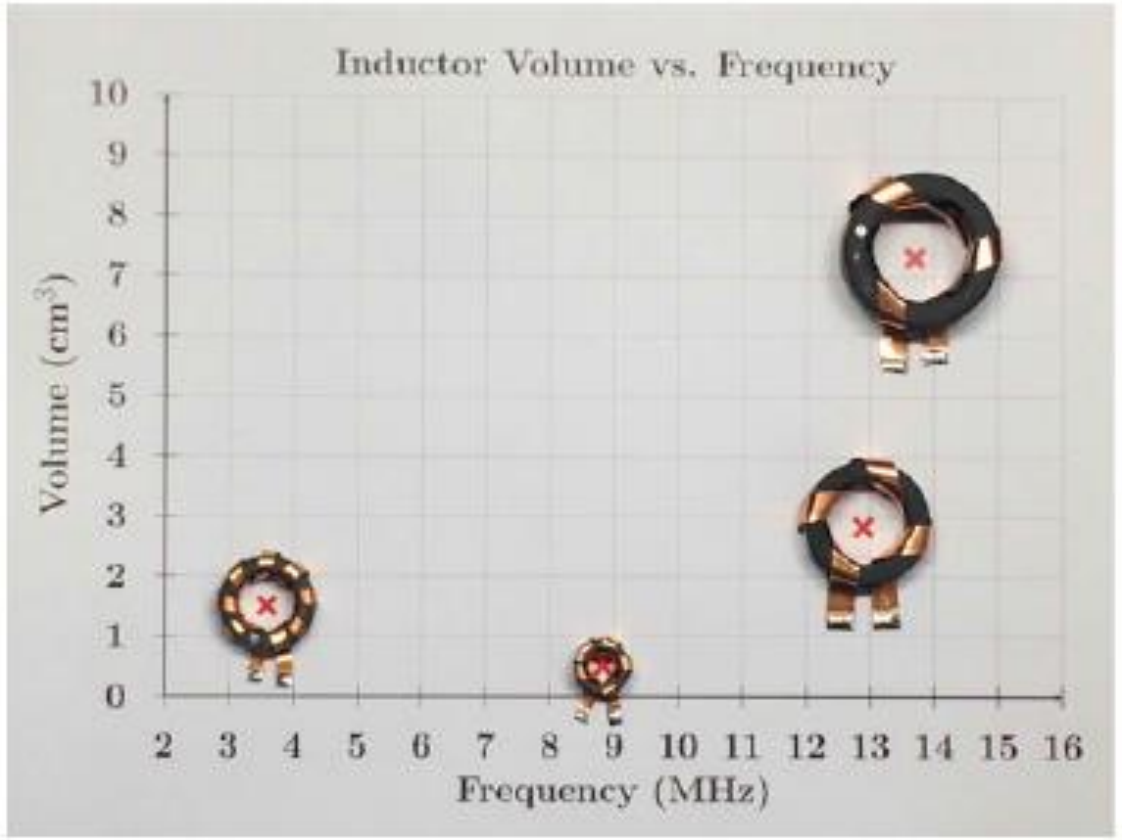


Fig. 4. Inductors using ungapped toroidal cores of Fair-Rite 67 material

SOA High Frequency Ferrite

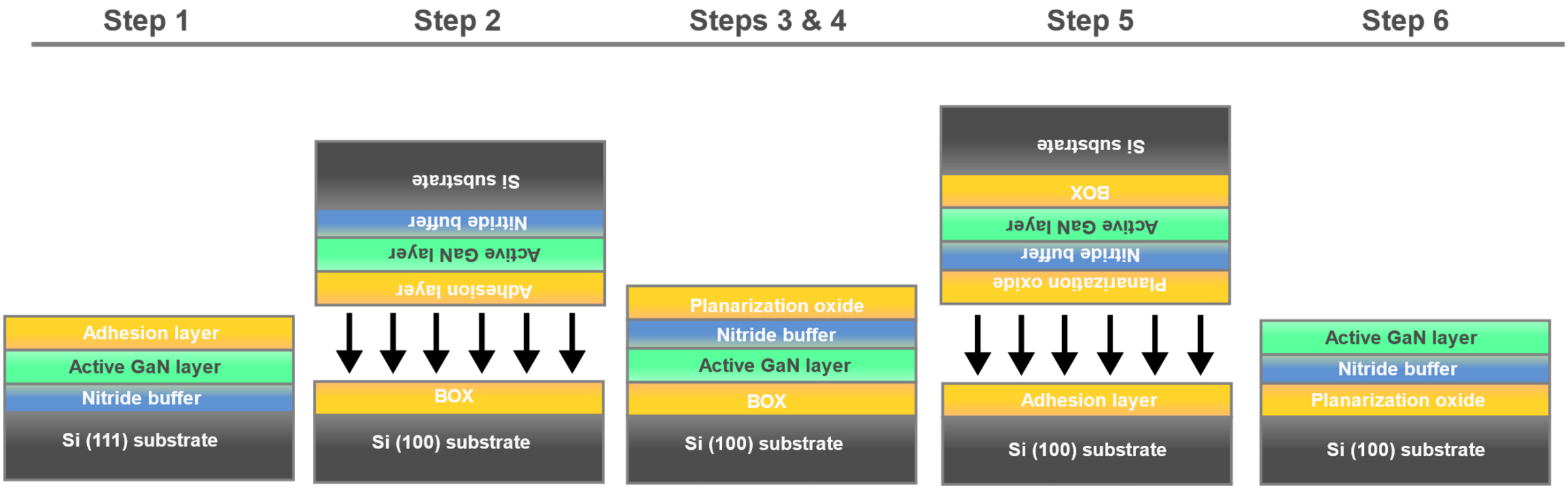
Wound Magnetic Device Performance Factor

"Measurements and Performance Factor Comparisons
of Magnetic Materials at High Frequency"
Alex J. Hanson, *Student Member, IEEE*, Julia A. Belk, *Student Member, IEEE*,
Seungbum Lim, *Student Member, IEEE*, Charles R. Sullivan, *Fellow, IEEE*, and David J. Perreault, *Fellow, IEEE*

We will create a similar **Embedded Device Performance Factor** *for material in planar toroid format in PCB windings*

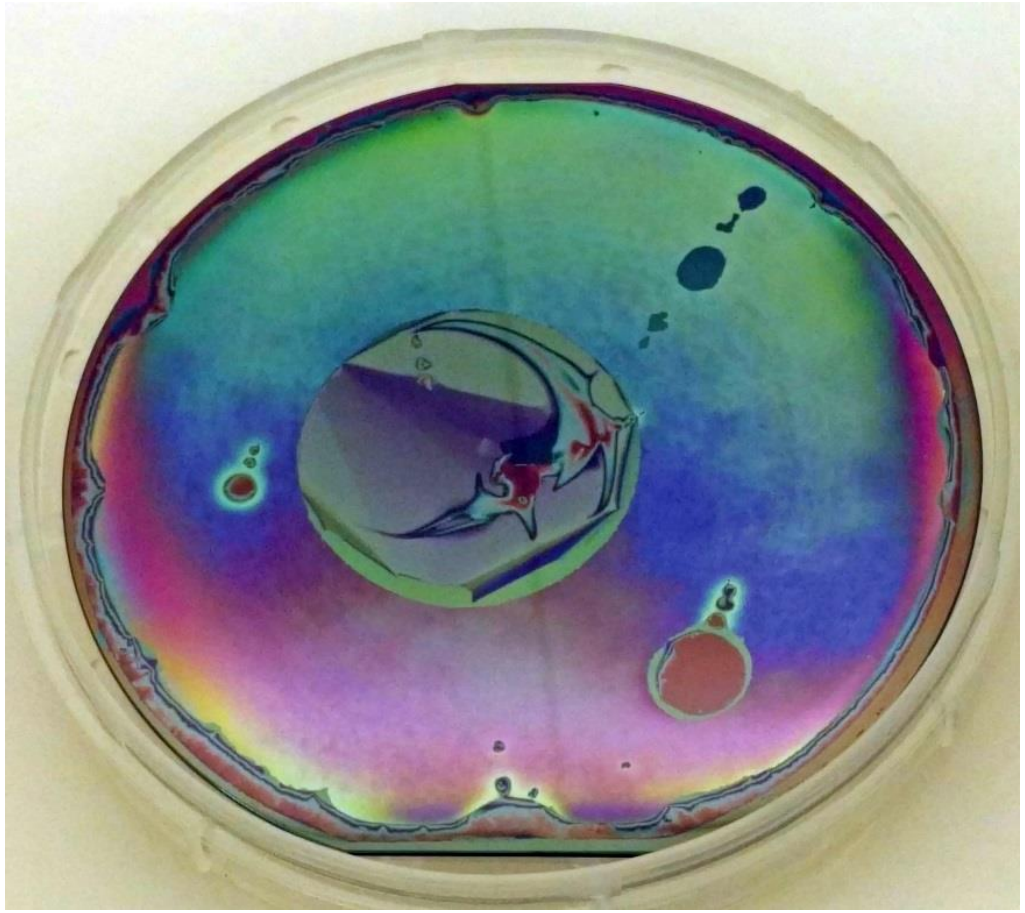
Wafer-Wafer Bonding Trials

Double DWB Integration of GaN on Si (100)

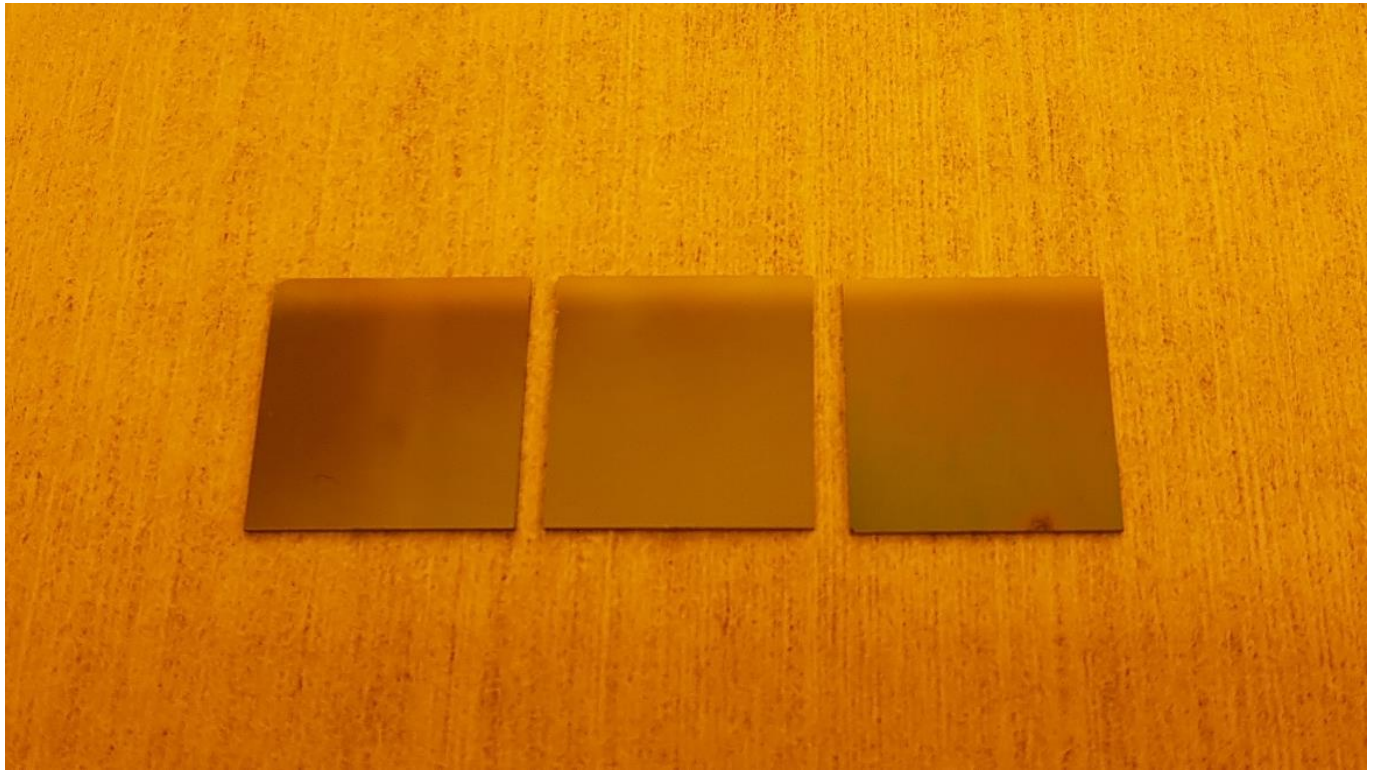


- Starting point is a HEMT stack grown on Si (111).
- Bonding to an intermediate transfer layer allows to realign the GaN charge for subsequent device fabrication
- Double doubling process may impact yield and requires sub-0.5 nm mean surface roughness on all bonded surfaces

2XDWB – GaN on Si (100)

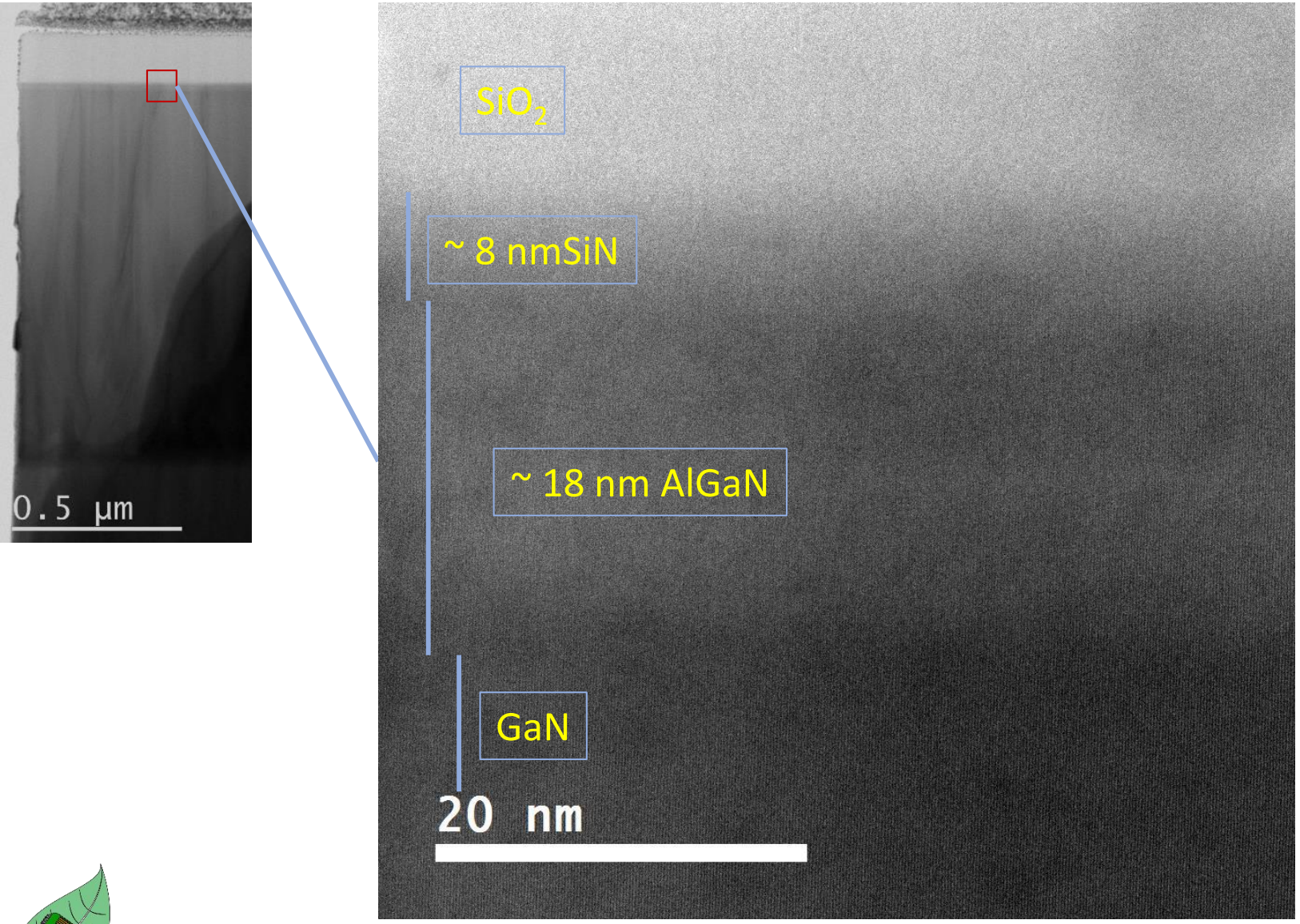


SiN capping layer exposed,
~8 pieces of 1.5cm chips



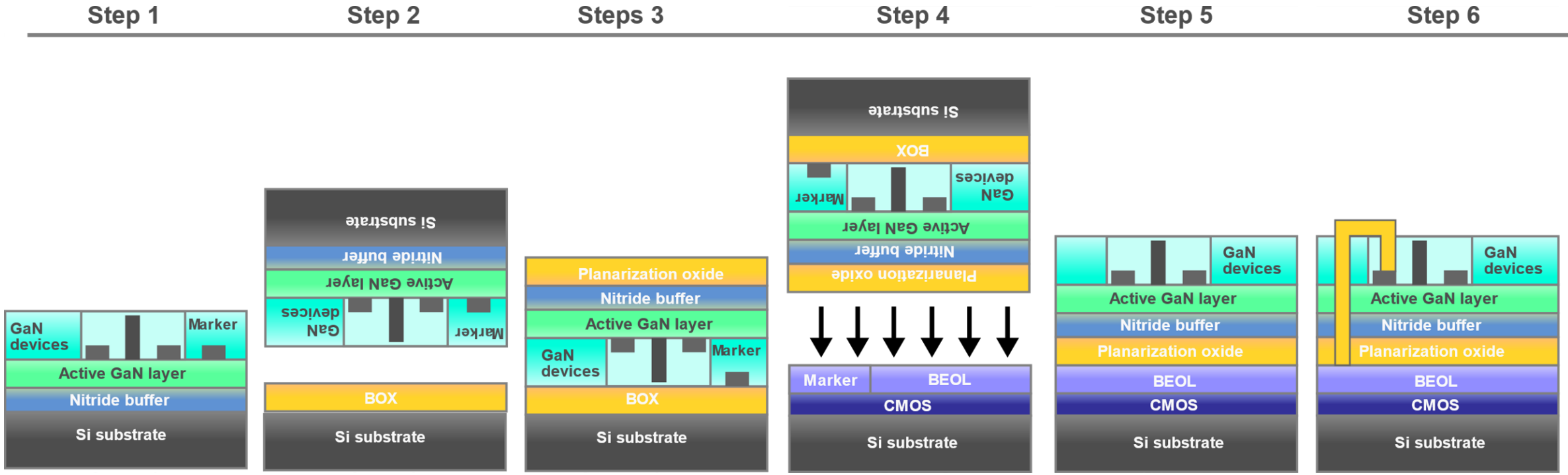
- 2XDWB after Si removal, with bonding oxides remaining
- Bowing results in delamination in the center area.
- Can be optimized by strain engineering

Crystal Quality of Bonded GaN Layer



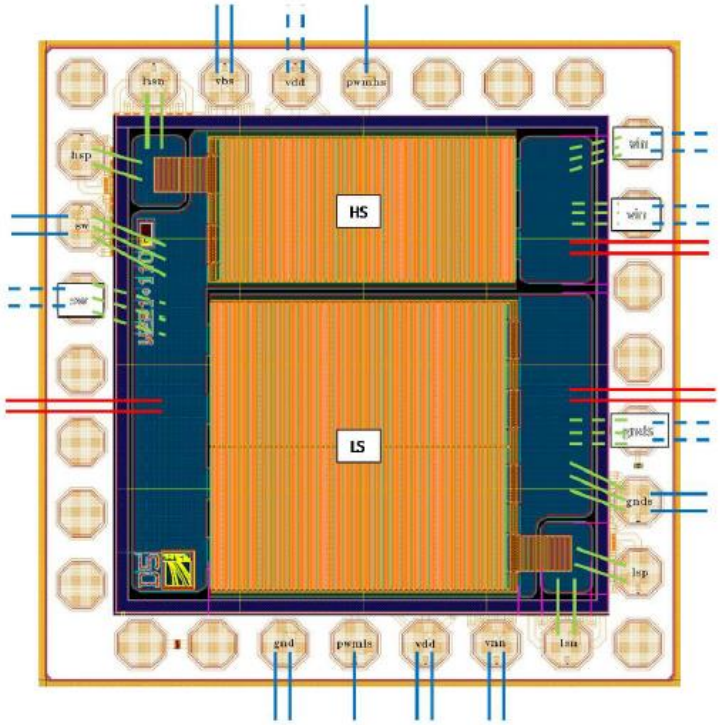
- TEM analysis of double-bonded layer
- Active device layers crystal quality not affected by bonding process

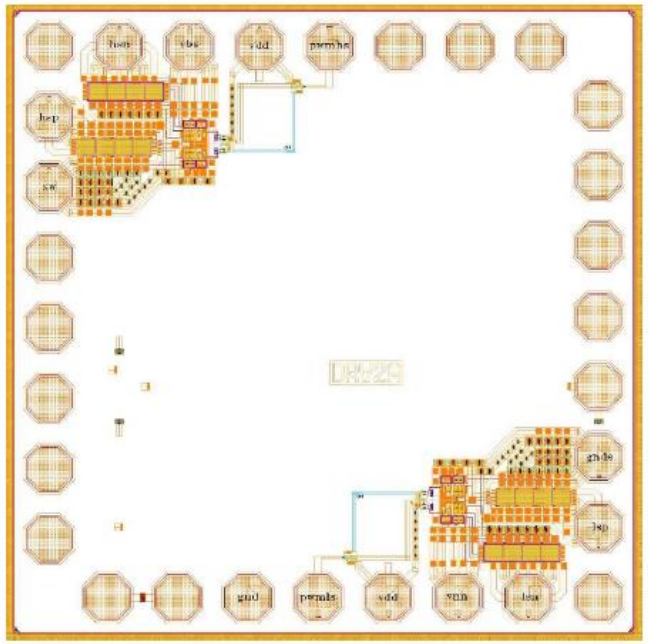
3D Integrated Power Switch and CMOS Driver



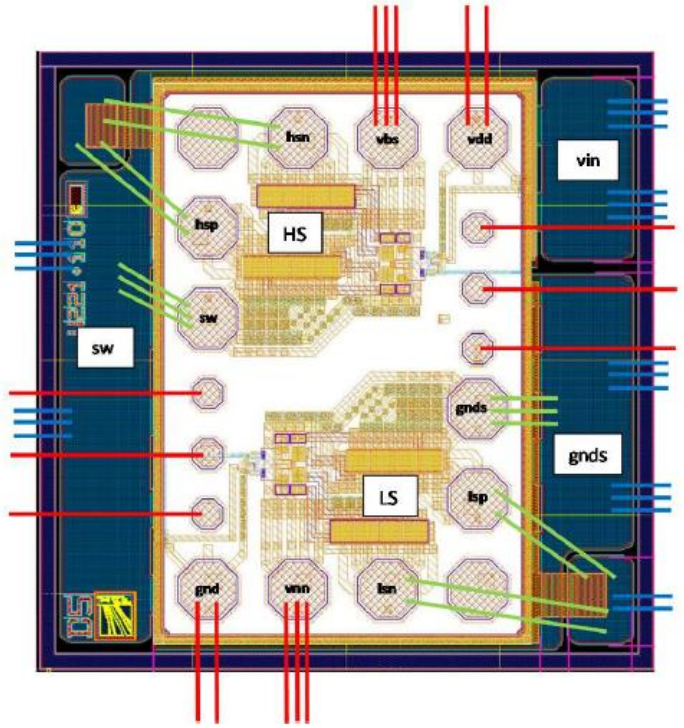
- Double wafer bonding process allows to integrated GaN switches with CMOS drivers monolithically
- Alignment between the two device layers is achieved by implementing markers on both layers, and using a retractable double-side camera - ~2 µm accuracy
- Circuit co-design allows straightforward interconnect formation
- Planarisation Process Fraunhofer ENAS

1st Engineering Prototype
Chip Scale GaN-on-CMOS Options





2.65 x 2.65 mm²

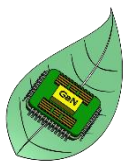


1.26 x 1.86 mm²

Ideal is probably for GaN Switch Design to be Smaller than CMOS design

GaN Device can be flip-chipped down onto Application Substrate with highest current contacts and highest thermal conduction path.

What are the Optimum Ratios of GaN to CMOS?



VR Design Space Exploration (Based on EPC 30V Technology)

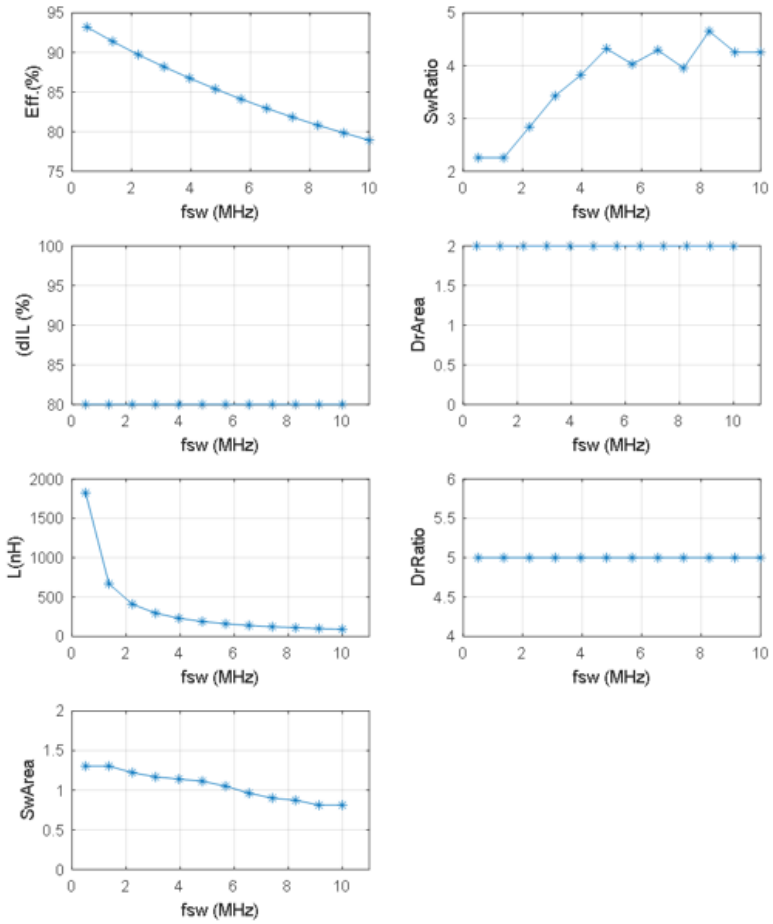


Figure 6: Design parameter values for maximized efficiency over frequency @ 1.25A per phase. Total switch and driver areas are normalized to the areas of EPC2111 and LM5113, respectively. Switch and driver ratio plots represent the ratios of the widths of the respective low and high side switches.

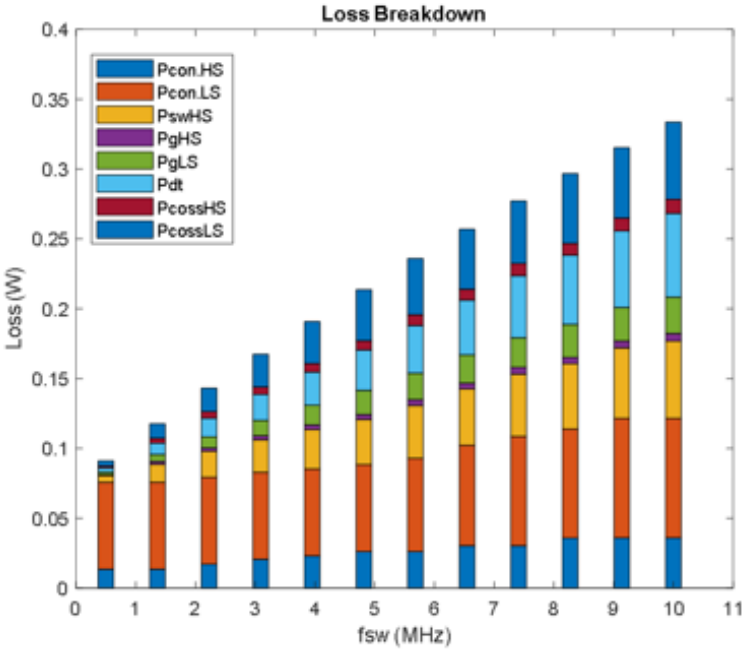
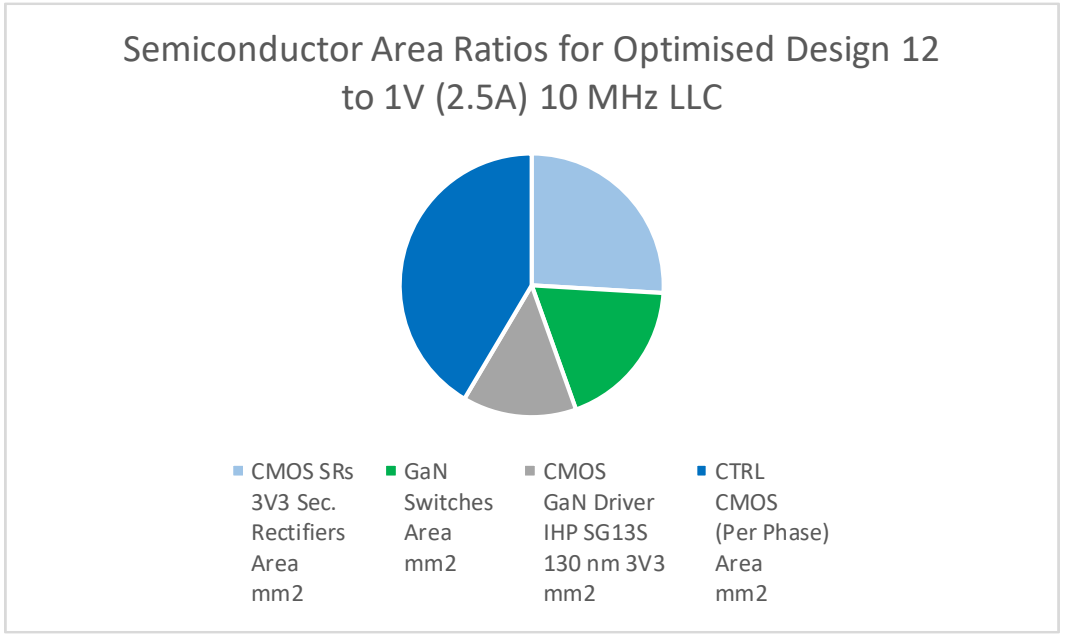


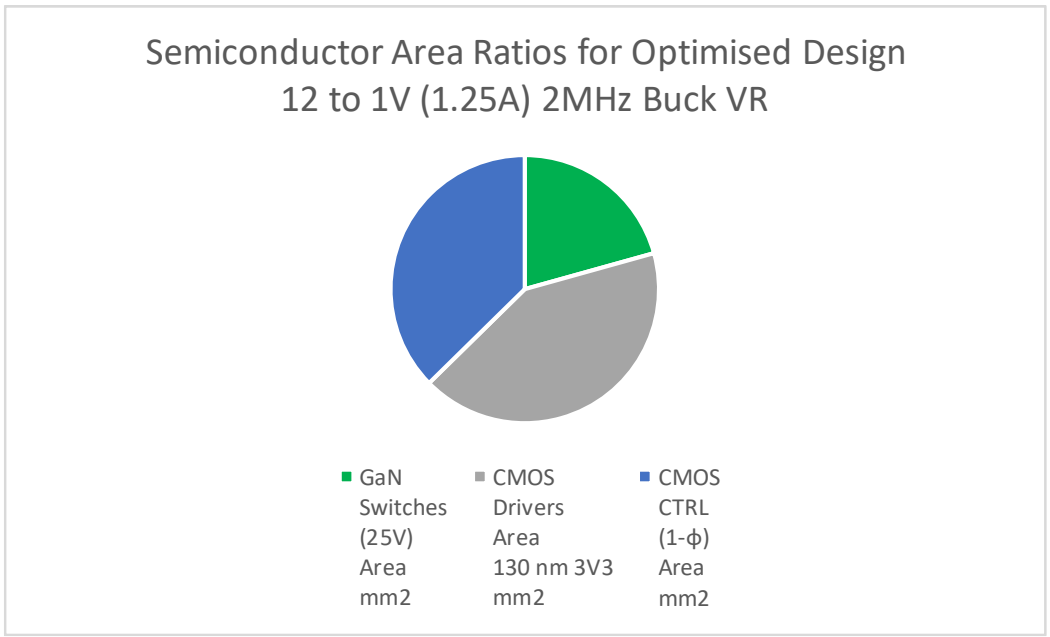
Figure 7: Conduction, switching, gate, dead-time and output capacitance loss for high and low side switches vs. frequency @ 1.25A per phase.

Pareto Front Methodology to project CMOS and GaN Switch Area Match-Ups for Optimised VR Designs – Analytic and Simulation Verified

Refer TI Application Report SLPA009A Power Loss Calculation with Common Source Inductance Consideration for Synchronous Buck Converters

Optimised Semiconductor Designs for 90+% efficient 12-1V 2MHz Buck (4mm^2) and 10MHz LLC (4.82mm^2)





- High *fsw* ZVS (Soft Switched, Resonant) Applications could use GaN-on-CMOS for Smart Switches – nice area balance down to 25V V_{BR}.
- Isolated Stage Capability – CM noise and EMI advantage

Buck POL: Silicon Capacitors and Chip Inductor Passives Require 9mm^2

- Large sink current capability on drivers for dV_{SN}/dt requires large drivers in efficiency optimised design – area imbalance at 25V V_{BR} => Higher Vin *& higher Duty* applications => R_{DSon} scales with V_{BR}^2 but $R_{DS}.Q_G$ FOM(V_{DS}) => Gate driver strength can decrease strongly as V_{SW} increases. Similarly for Qoss loss.
- Low Duty Cycle (low Vo) POL application challenged for SR FET.

GaN with Integrated Driver

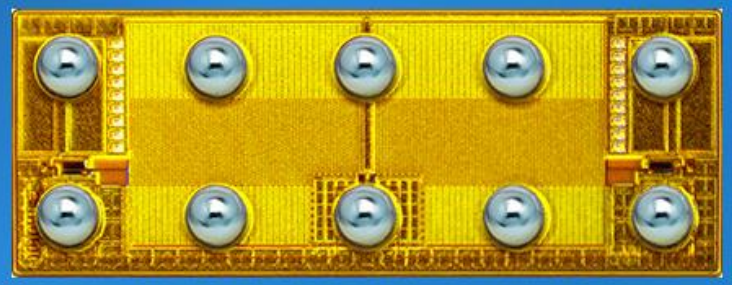
EPC2115: Dual 150 V, 5 A Integrated Gate Drivers eGaN® IC

Integrated Gate Driver

- Low Propagation Delay
- Up to 7 MHz Operation
- Operates from 5 V Supply

Dual 150 V, 88 mΩ eGaN FET

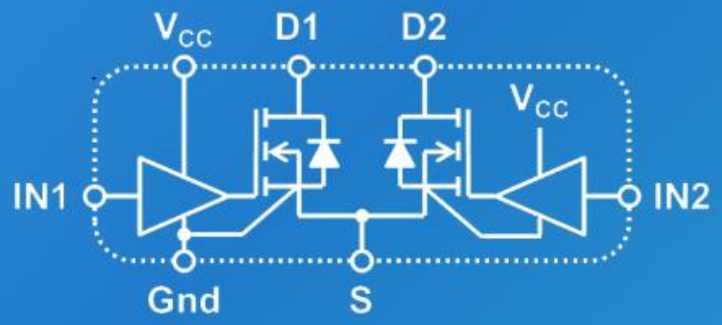
Low Inductance BGA



Die Size: 2.9 mm x 1.1 mm

Applications

- Wireless Power
- High Frequency DC-DC Conversion

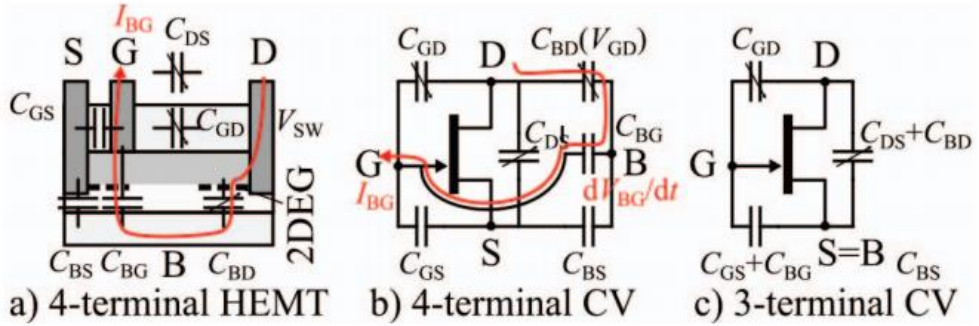


Status: Engineering

Engineering devices, designated with an ENG* suffix at point of purchase, are on engineering status and should not be used for reliability stress testing or other qualification testing without contacting your local field application engineer for the latest status.

- CMOS Drive is better
- Specific On Resistance for Low Voltage CMOS drivers are much lower than 25V GaN
- 3V3 – 5V CMOS
  - $Sp.R_{ON}$ = 2.5 – 6 $m\Omega.mm^2$
- Smart Driver Features require CMOS
  - Isolated GD (Pulse) Signal recovery
  - Adaptive Delay Management
  - 3rd Quadrant Drive
  - Protection Features

Monolithic Bridge Considerations - floating bulk?



S. Moench, C. Salcines, R. Li, Y. Li and I. Kallfass, "Substrate potential of high-voltage GaN-on-Si HEMTs and half-bridges: Static and dynamic four-terminal characterization and modeling," *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Stanford, CA, 2017, pp. 1-8.

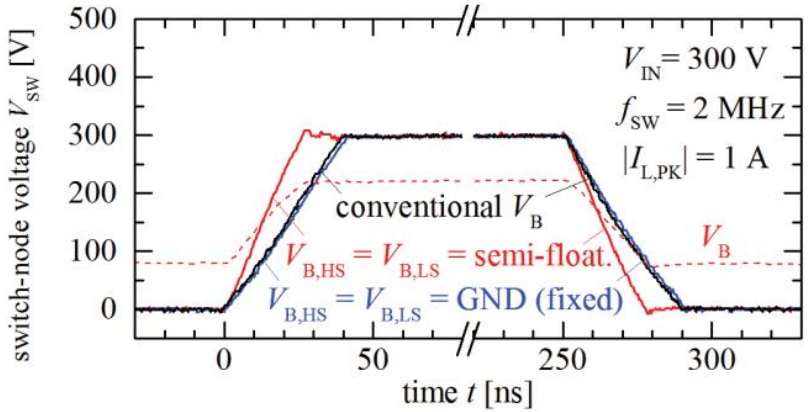


Fig. 11. Measured resonant turn-off switching transitions for three substrate terminations with same electrical switching parameters. For semi-floating substrate, the measured common backside voltage V_B is also shown.

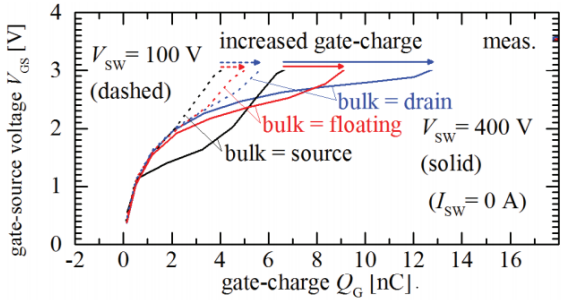


Fig. 8. Measured gate-charge Q_G is increased for floating and drain-connected substrate compared to source-connected.

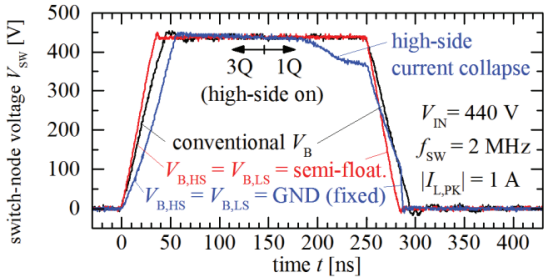
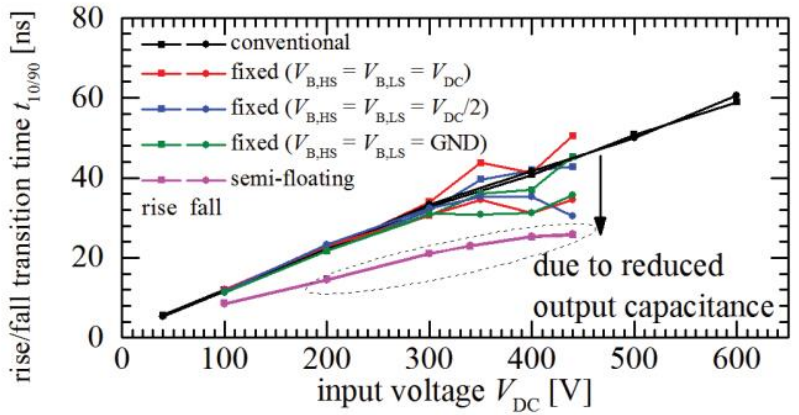


Fig. 13. Measured current-collapse of high-side transistor for fixed-to-ground substrate termination compared to source-connected and semi-floating substrate. (440 V, 2 MHz, 1 A).



Q_G ↑

Current Collapse ↓

Switching Speed ↑ C_{OSS} ↓

Technical Competition for GaN

- Silicon Switch Stacks for 600V Applications
  - Multi Level Topology and lower Voltage LDMOS/ VDMOS Switch Stacks per Cell

- Fine Geometry CMOS Switch Stacks and ML for 12V Applications?
  - Isolated switch stacks have large Specific Ron but can have very low switching FOM
  - Economics will have a say!

Conclusion

GaN-on-CMOS can offer highest performance by enabling Smart Switch (Integrated Driver) Applications.

Larger geometry CMOS (130 – 180nm) would enable excellent integrated Smart Driver.

Very good CMOS Smart Driver AREA match-up to GaN Switch for many optimised designs – ZVS designs to 25V and at higher V_{BR}, higher duty cycle topologies.

Smart Switches will be of rapidly growing importance

- ***Multi-Level converter Gate Drives, Isolated Power, Protection & Control Telemetry***
- 3rd Quadrant Drive to minimise conduction voltage drop
- Protection features at stacked switching cell level
- Minimisation of Common Source Inductance and Gate Driver Switching Loop Inductance drive issues.
- Delay management between upper and lower drives
- Drive signal logic recovery from Gate Driver Galvanic Isolation circuits
  - Gate Driver Transformer size minimisation (<10nVs) or minimisation of GD coupling capacitors
- Refreshing pulses to counter Gate Leakage

Advanced CMOS PWM Control and other CMOS (LV SRs etc.) might be more ideally implemented on **fine geometry CMOS** and would probably not be a part of the GaN-on-CMOS wafer.

GaN-on-CMOS Applications

- ***Smart Switches and Smart Bridges*** for Automotive, Energy (Distributed Generation, Prosumer), Aerospace, Data-Centre Power and Servers, Industrial Drives, … everywhere from today's > $50V_{BR}$ switches is technically hugely attractive.

- **Multi-Level Topologies** are very important (solution density) => **100-200V GaN & Smart Switches**

- Heterogeneous Integrated Monolithic Bridge Converter solutions for Multi-Level/Multi-Phase for Multi-Node HPC – more attractive for 48V
  - 12V POL challenged to get to higher switching frequency
    - LV switch technology needs to improve 3X with regard to switching FOMs
    - Magnetising Inductance value requires 10X in switching frequency
    - Resonant requires large area low silicion voltage rectifiers

- Other areas such as 5G Envelope Trackers (ET) in Cell Site RF Transmitters
  - Massive MIMO will require large array of GaN ET with CMOS drives
  - ET bandwidth must generally extend to several hundred MHz
  - Some solutions may usefully use GaN switches at 25-50V type voltage levels or possibly GaN/low voltage CMOS Cascodes.

Acknowledgements

– Project partners who supplied material IBM, RECOM, AT&S, IAF, IHP

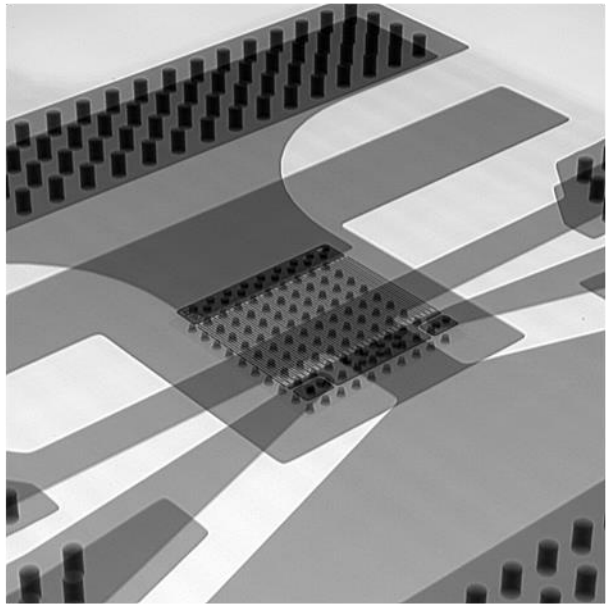
- All Project Partners

- KU Leuven Project Co-ordinator and Project Leader

H2020-NMBP-2016-721107

Back-Up

100 V-Layout-Design for AT&S - ECP®-PCB-Embedding



Experience in previous work:

IAF Fraunhofer and AT&S