Reliability issues in GaN power devices

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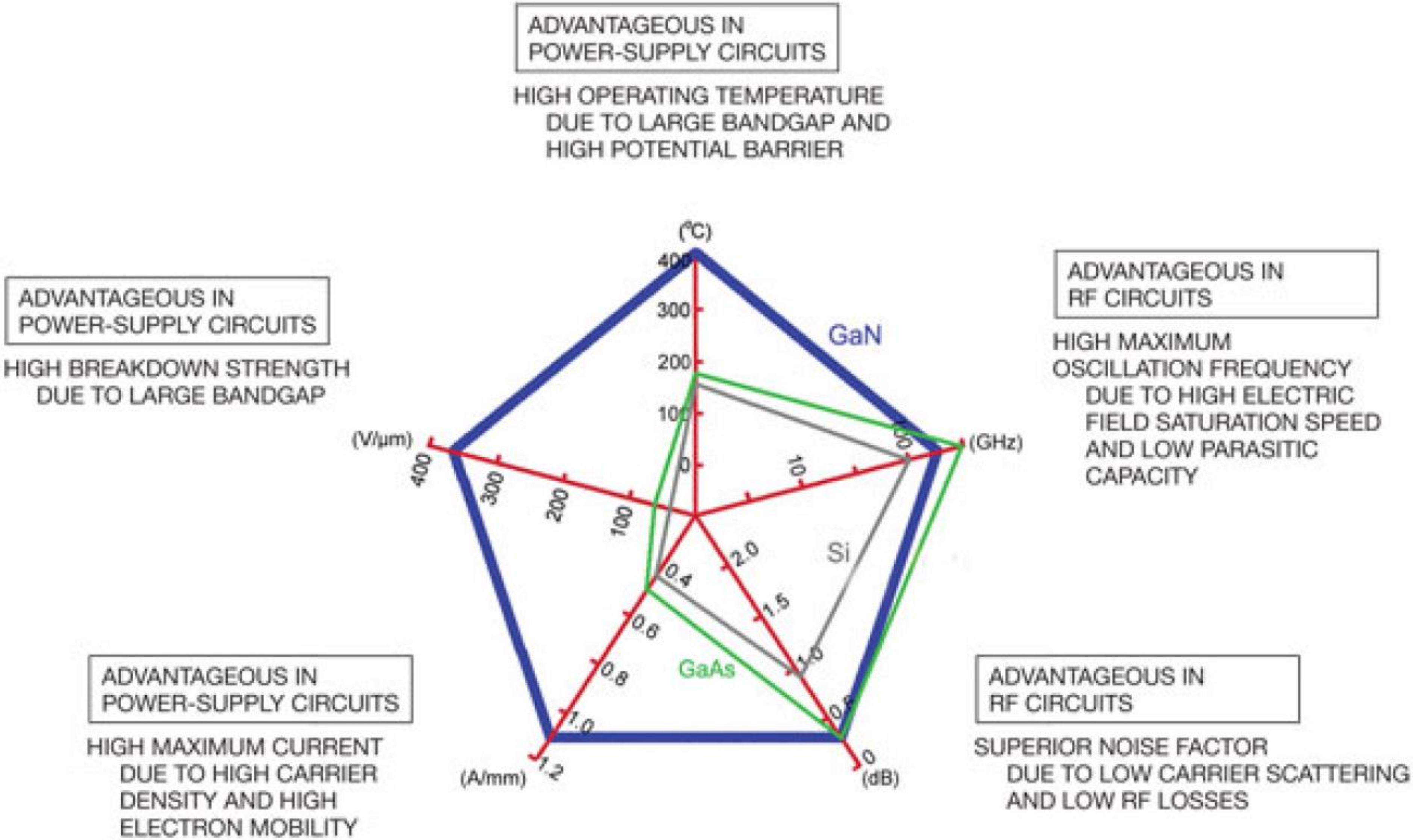
Outline

- Introduction on GaN-based HEMTs
- Breakdown mechanisms at high drain bias

- Parasitic (trapping) mechanisms → recoverable degradation
  - Current/Ron collapse
  - Methods for analyzing defects in GaN-HEMTs
  - A database for deep levels in GaN
- Permanent degradation mechanisms
  - Degradation in off-state → Schottky-gate
  - Degradation under FW bias → p-GaN gate
  - Degradation under FW bias → MIS gate
- Conclusions

Pay attention to the symbol

Advantages of GaN (compared to Si and GaAs)



http://www.edn.com/Pdf/ViewPdf?contentItemId=4409627

GaN vs other semiconductors

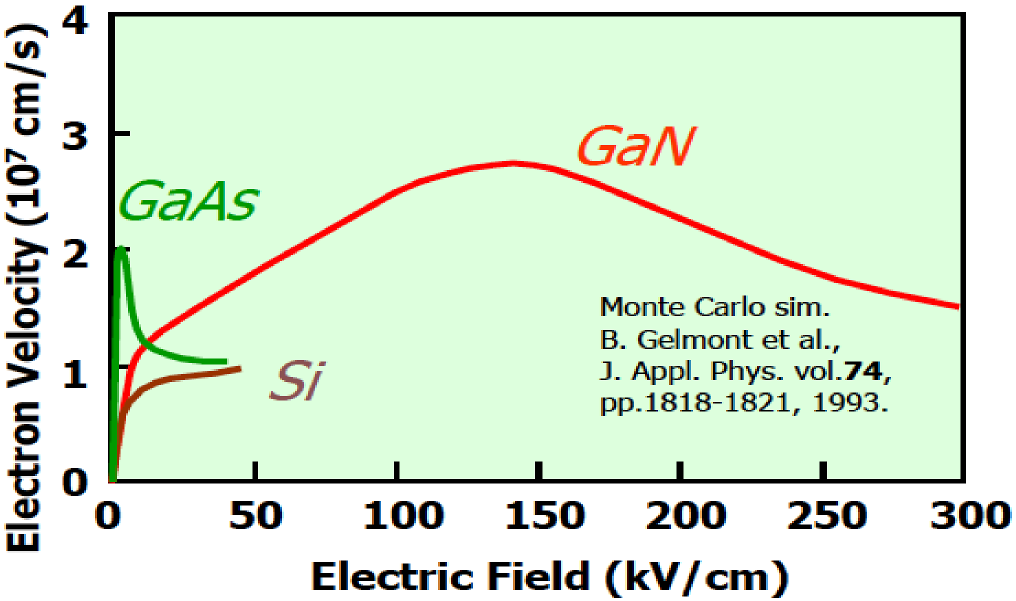
	Si	GaAs	4H-SiC	6H SiC	GaN/ AlGaN
Band gap energy E_g (eV)	1.1 ind.	1.43 dir.	3.26 ind.	3.0 ind.	3.42 dir.
Electron mobility μ_e (cm^2/Vs)	1500	8500	1000	500	1300 >2000 (2DEG)
Electric breakdown field E_{crit} (10^6 V/cm)	0.3	0.4	2.0	2.4	3.3
Saturation velocity v_{sat} (10^7 cm/s)	1.0	2.0	2.0	2.0	2.7
Thermal conductivity κ (W/Kcm)	1.5	0.46	4.9	4.9	2.4
Johnsons Figure of Merit ($\sim V_{Br}^2 \times v_{sat}^2$)	1	7	180	260	760
Maximum operation temperature T_{max} (°C)	200	300	500	500	500

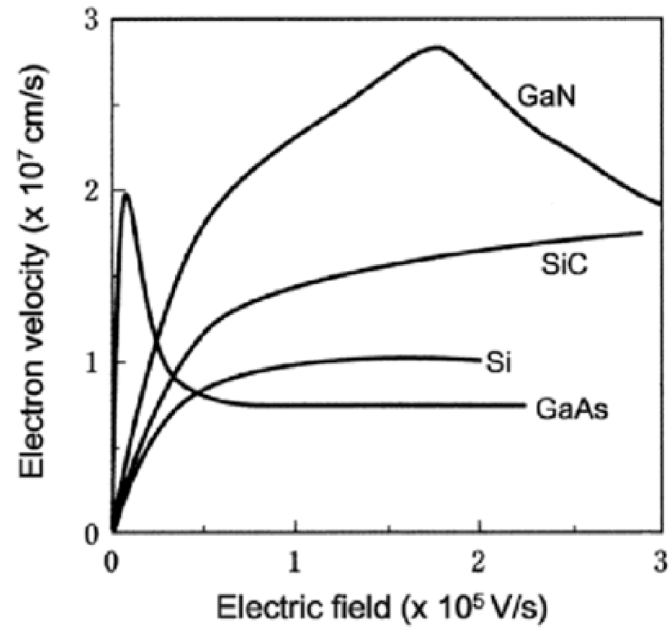
…. but fully usable only if heat dissipation can be managed

→ trade-off

Joachim Würfl, "GaN Power Devices (HEMT): Basics, Advantages and Perspectives", ECPE Workshop 2013

GaN vs other semiconductors





Kiyoshi Takahashi, Akihiko Yoshikawa
and Adarsh Sandhu (Eds.)

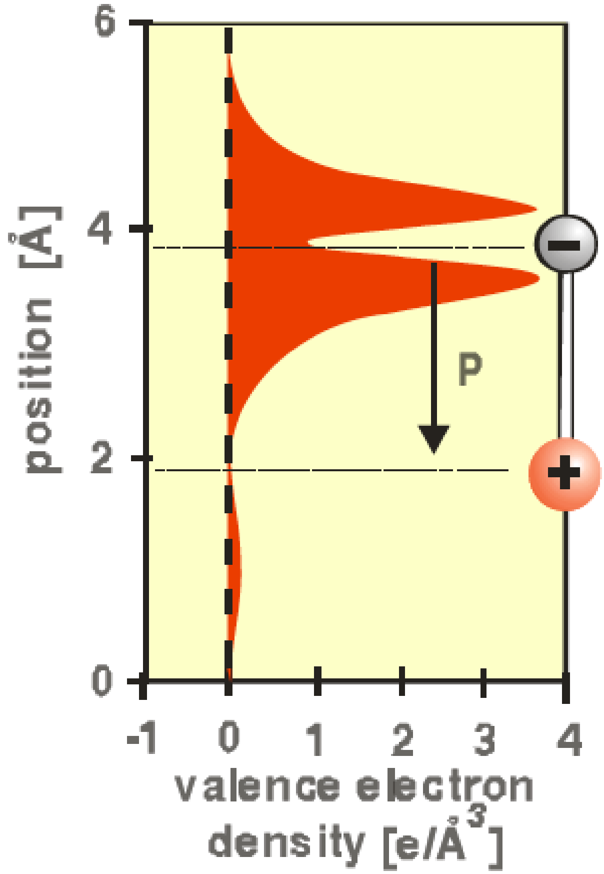
Wide Bandgap Semiconductors

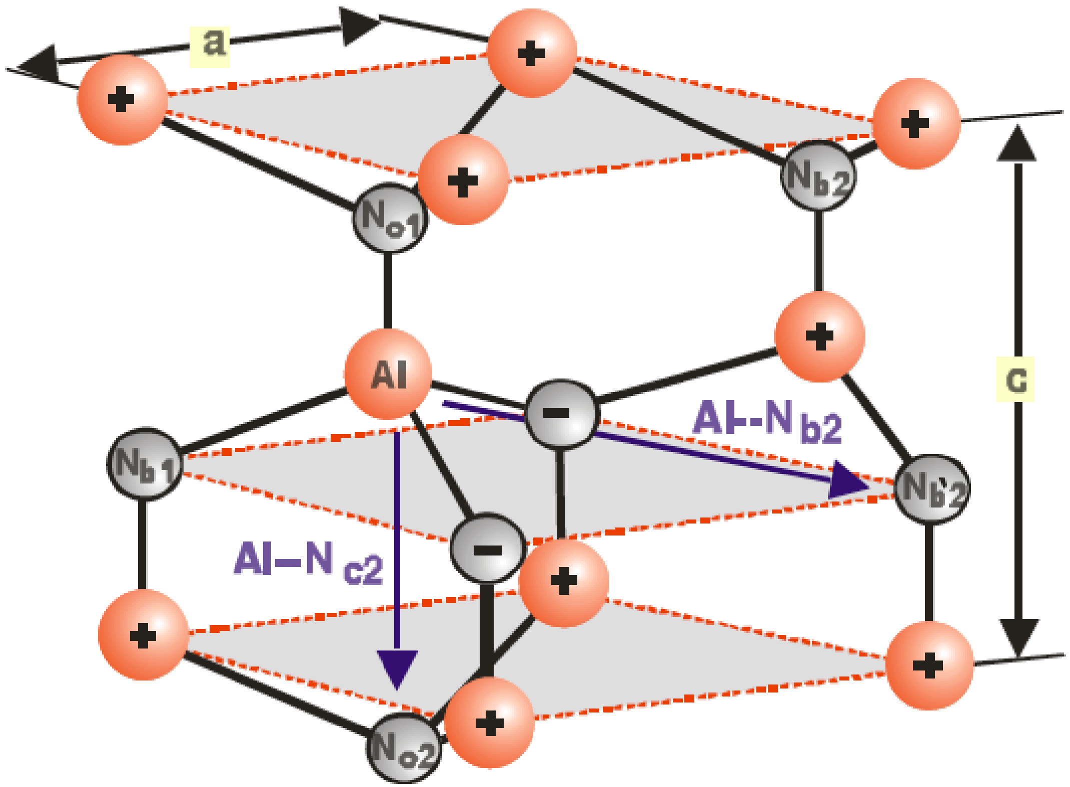
Fundamental Properties and Modern Photonic and Electronic Devices

ISBN-10 3-540-47234-7 Springer Berlin Heidelberg New York
ISBN-13 978-3-540-47234-6 Springer Berlin Heidelberg New York

Springer

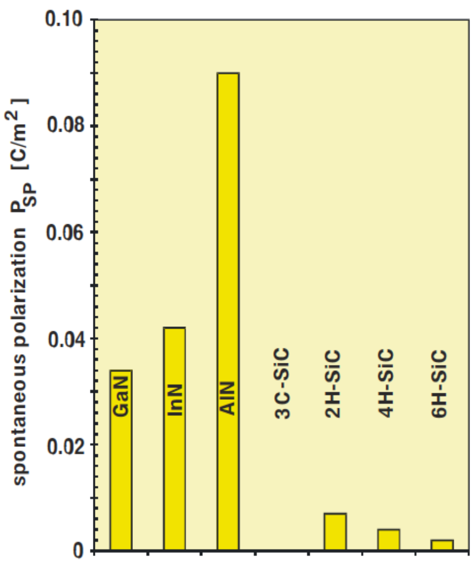
GaN: Pyro- and Piezo Electric

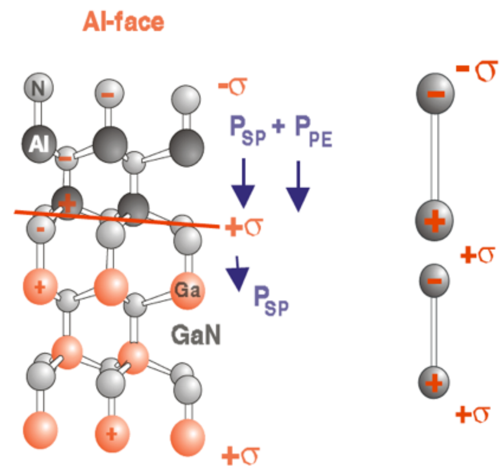


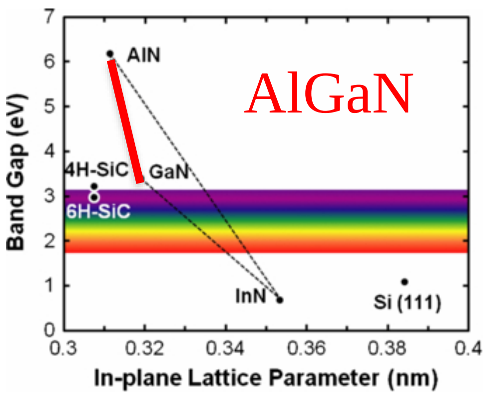


O. Ambacher et al JAP 87, 334 (2000)
O. Ambacher et al. J.Appl. Phys. 85, 3222 (1999)

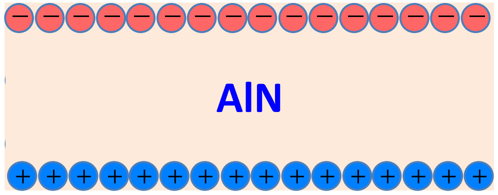
GaN: Polar Material

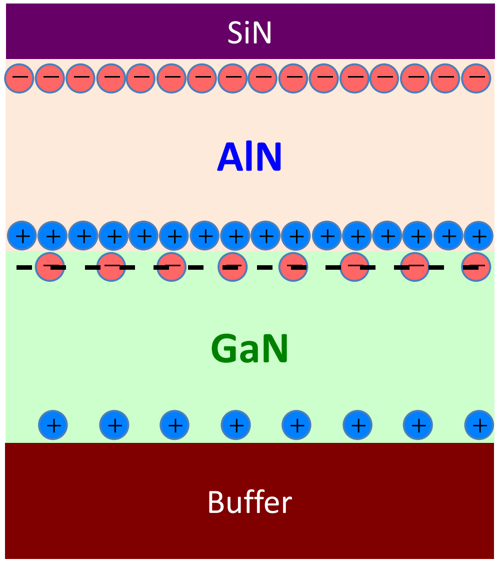




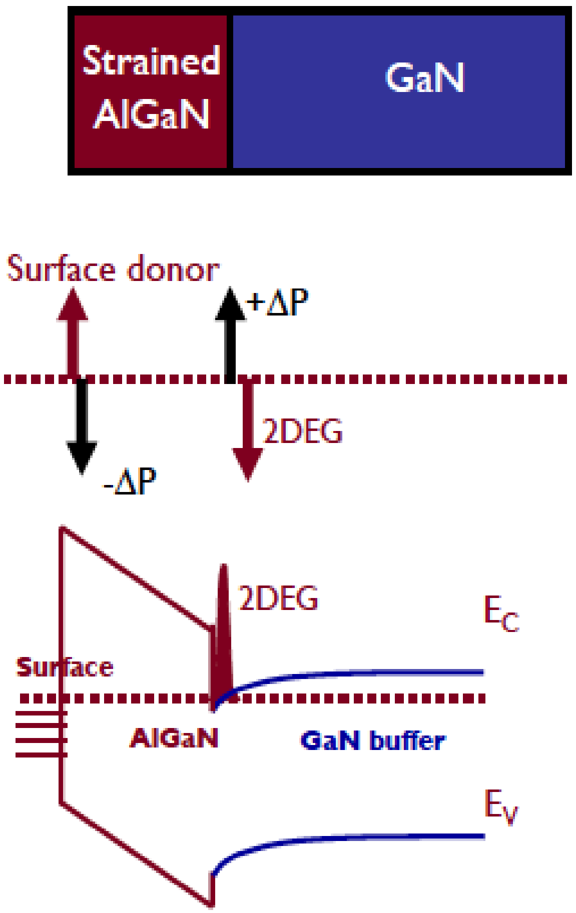


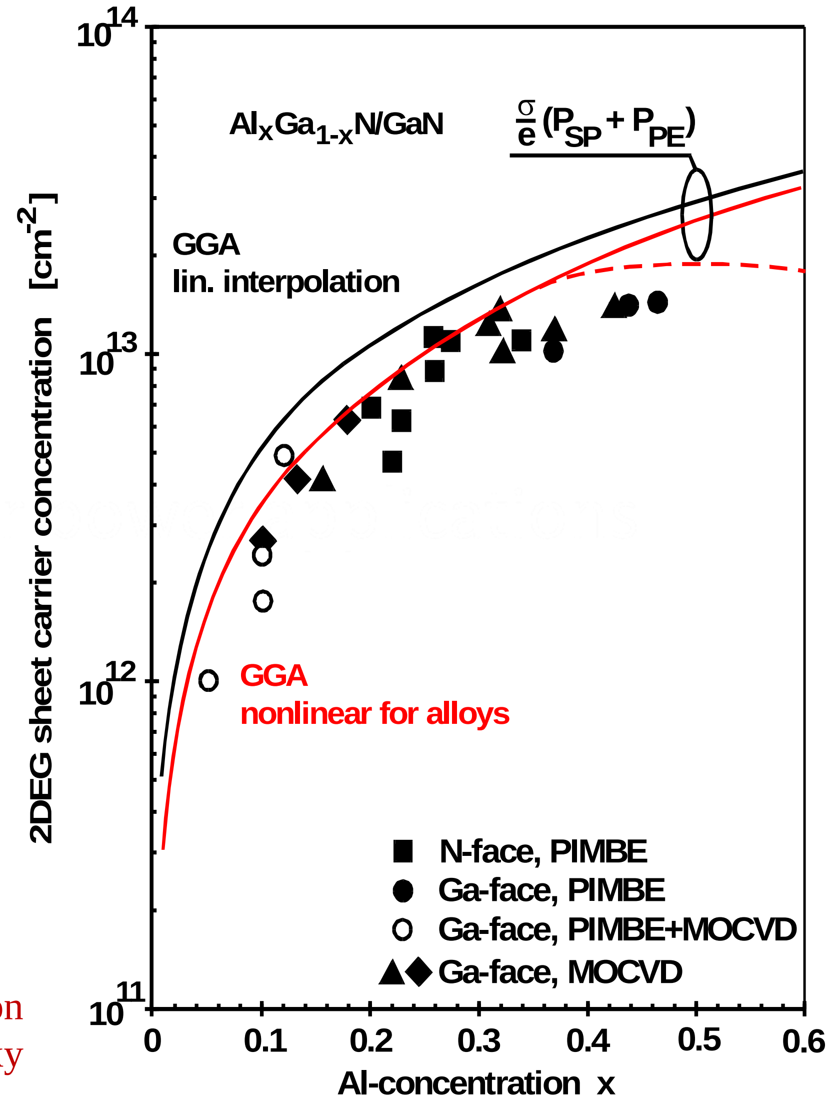
Typically 20-25% Al composition





GaN HEMTs: 2DEG w/o doping!

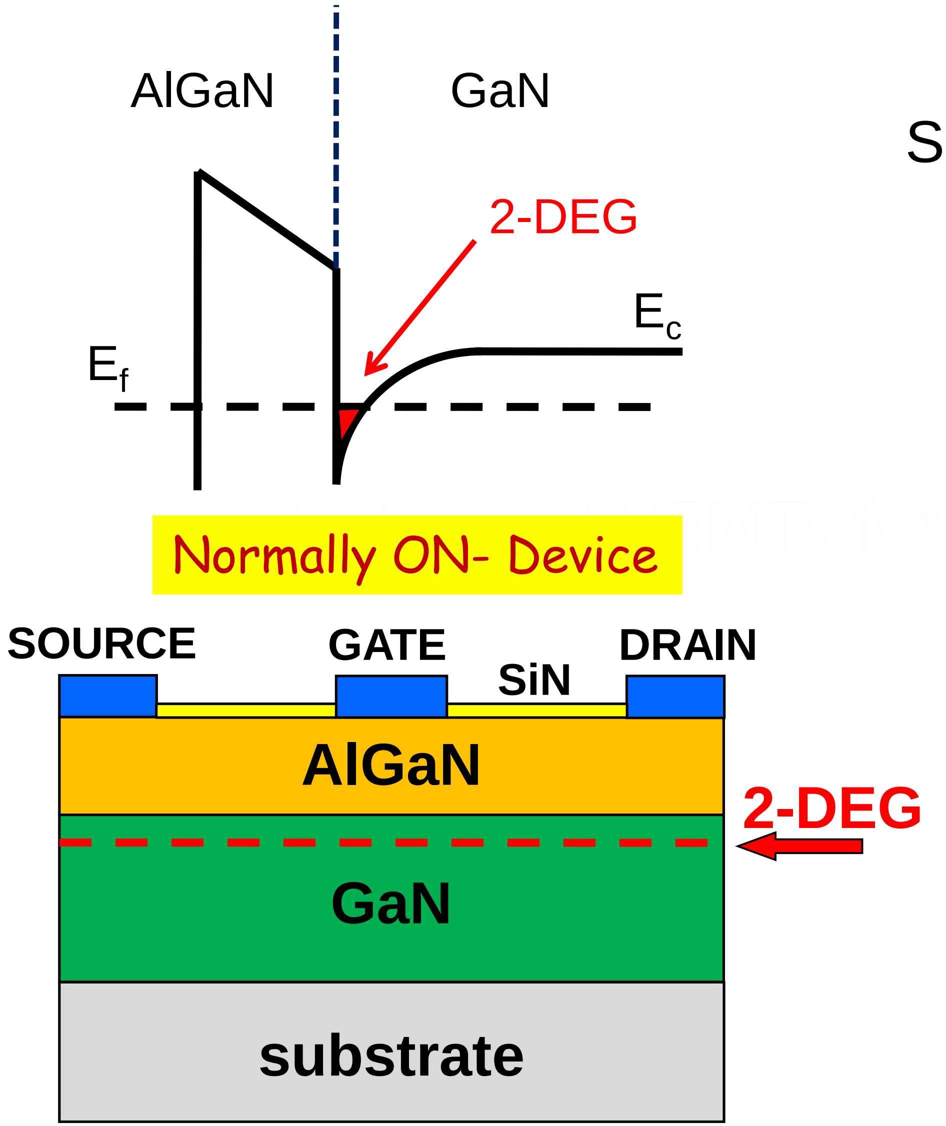




GGA generalized gradient approximation

PIMBE plasma-induced molecular beam epitaxy

Basic GaN HEMTs design



Spontaneous + piezoelectric polarization

⇓

2-DEG channel

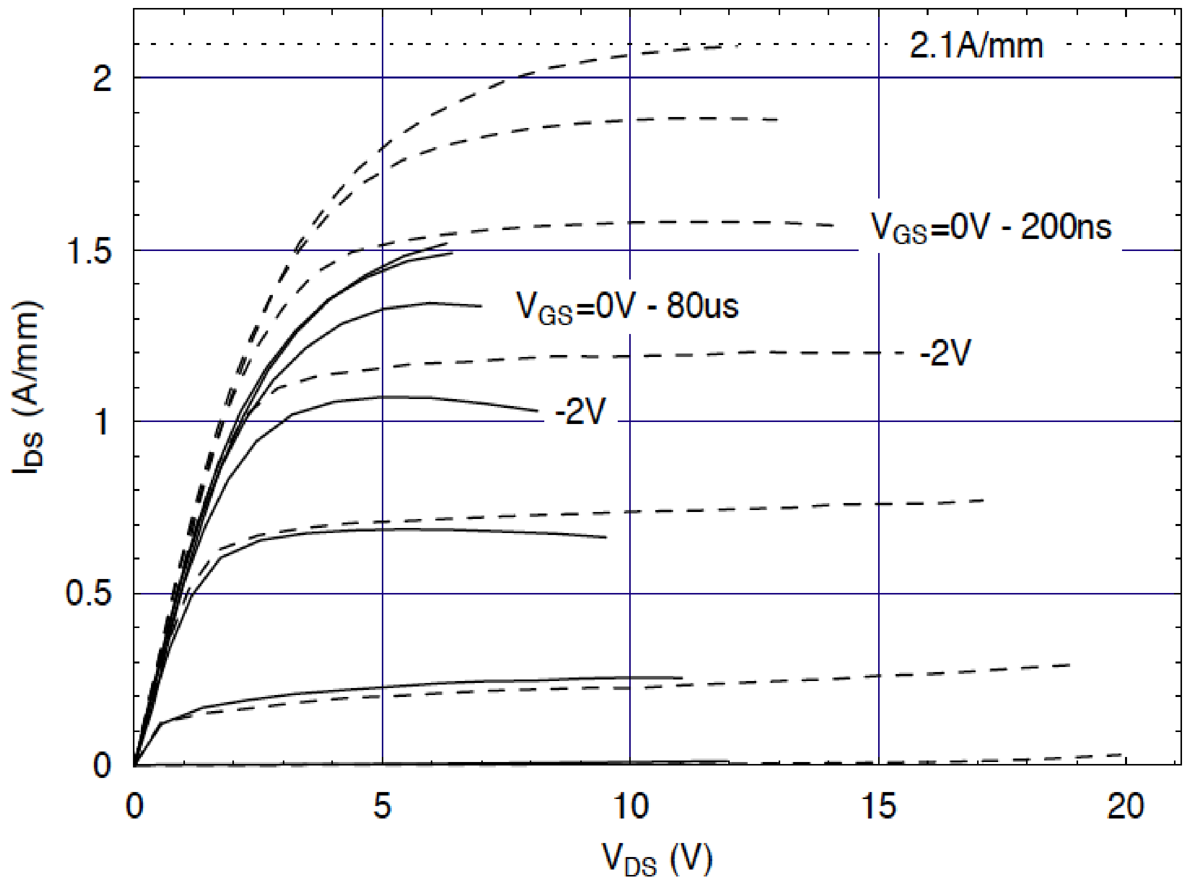
⇓

High carrier concentration
+
High mobility

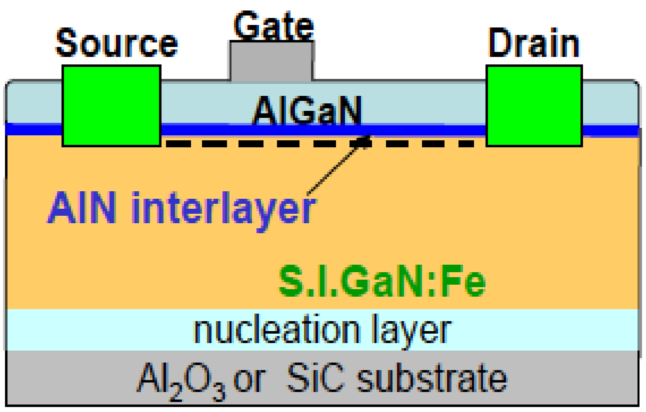
⇓

Ready for power and RF applications

Basic GaN HEMTs design

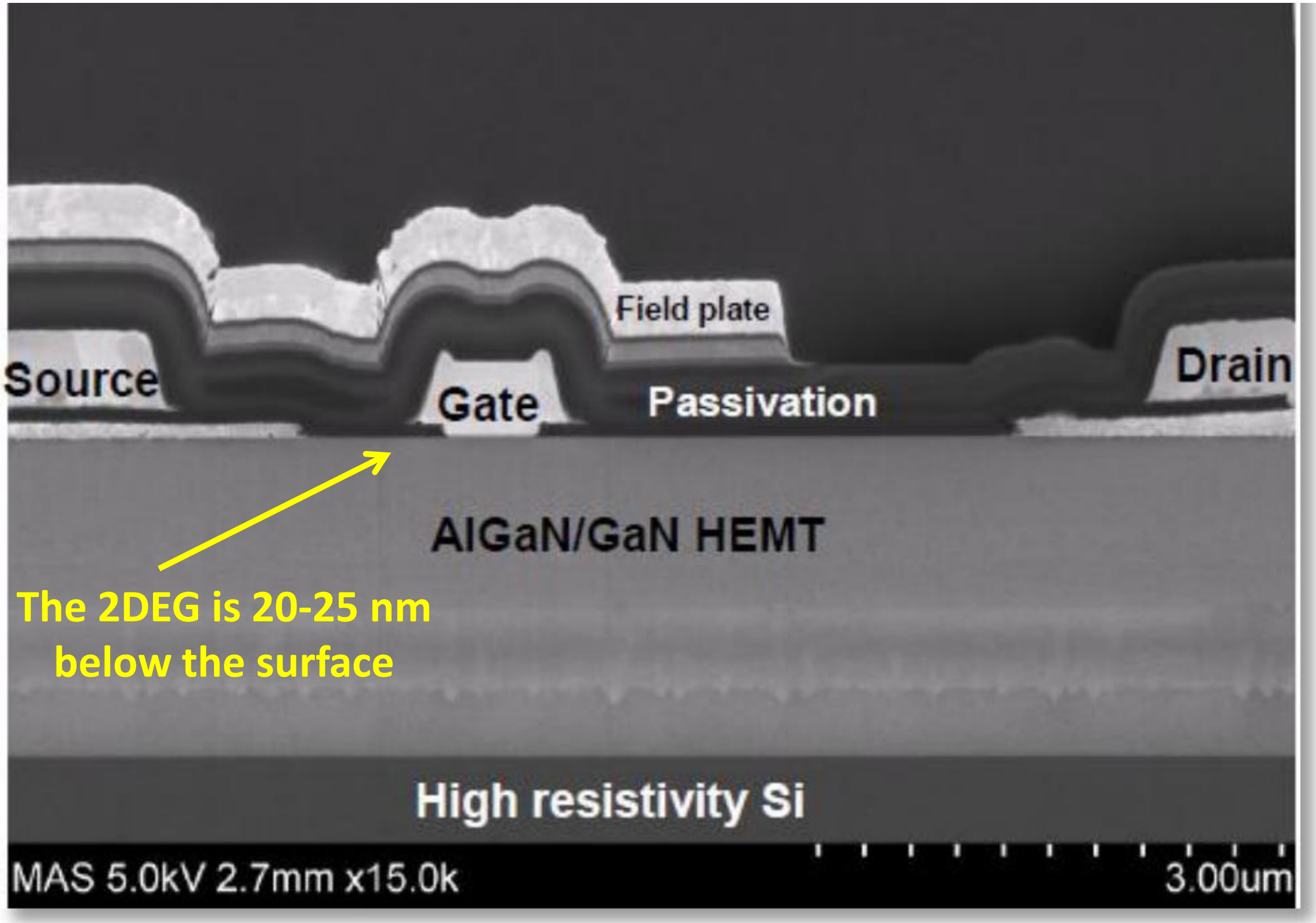


Normally ON- Device



A. Chini, R. Coffie, G. Meneghesso, E. Zanoni, D. Buttari, S. Heikman, S. Keller, and U. K. Mishra "**A 2.1A/mm Current Density AlGaN/GaN HEMT**", IEE Electronics Letters, vol. 39, N. 7, April 2003, pp. 625-626

Typical structure of AlGaN/GaN power HEMTs



Cross section SEM image of 0.5/m NRF1 field plated AlGaN/GaN HEMT technology (Nitronex)

http://www.i-micronews.com/upload/Rapports/Yole_III-V_Epitaxy_April_2012_Report_Sample.pdf

GaN HEMT for RF applications

- Telecommunications:
  - ✓ Mobile base stations
  - ✓ Wi-Fi
  - ✓ Satellite communications
  - ✓ Military communications

(Output power range: 10 W – 100 W)

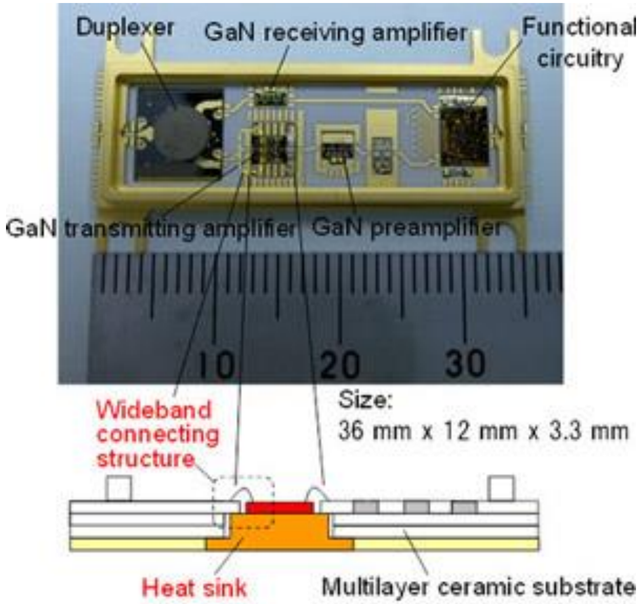
The Proba-V satellite

- Radars:
  - ✓ Weather
  - ✓ Aeronautics
  - ✓ SAR/phased array
  - ✓ Satellites

(Output power range: 100 W – 1 kW)

Radar

GaN HEMT for RF applications



Fujitsu's mobile WiMAX "BroadOne WX300" base station for outdoor use

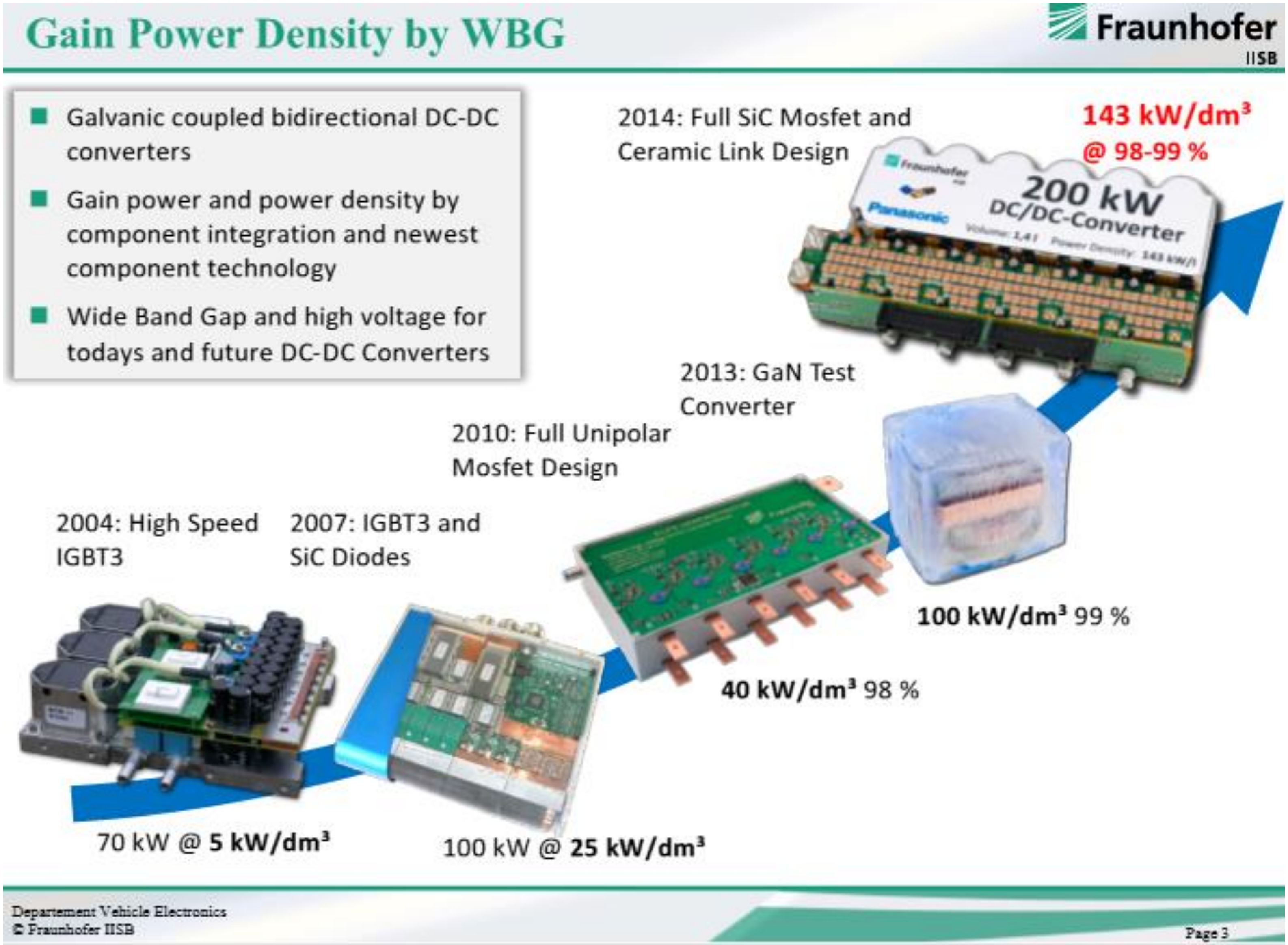
The volume of the unit is approximately 20L.

… high-frequency signals passing through the module can be transmitted at up to 40GHz

… It was possible to shrink the size of the millimeter-wave transceiver module. With dimensions of 12mm × 36mm × 3.3mm, **the new module is less than 1/20 the size of conventional integrated units.**

http://www.semiconductor-today.com/news_items/2013/JUN/FUJITSU_100613.html

The potential …



System benefit …

Mobile Systems: Automotive

IALB

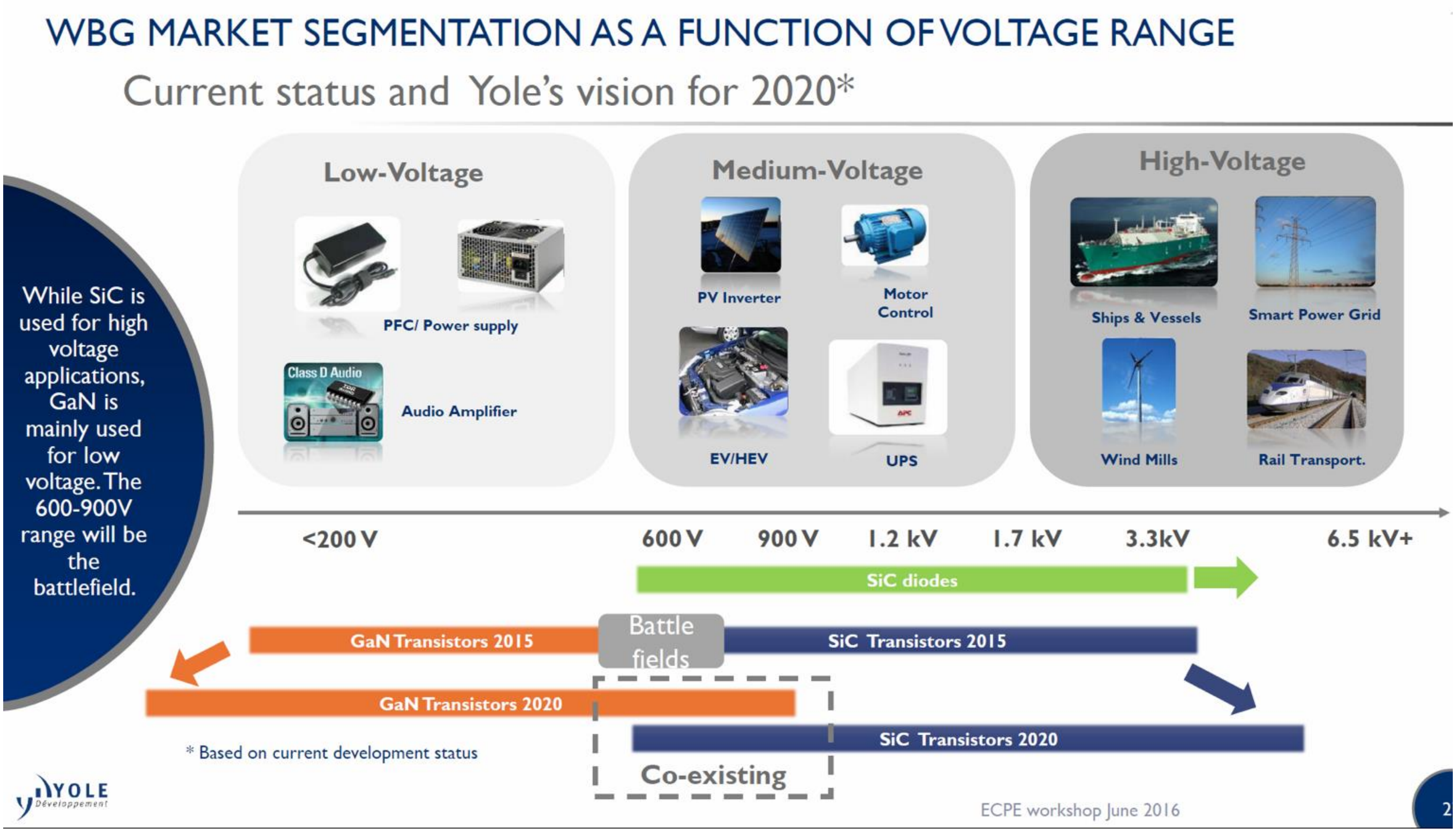
- Any mobile system should benefit
  - Higher efficiency is higher range or smaller storage
  - Smaller volume and lower weight of the converter and cooler
  - By leverage effect even smaller volume and lower weight of the storage
- Good example is Toyota
  - 10% fuel savings targeted, 5% achieved on prototypes already
  - Power control unit down to 20% of volume, weight from 18kg down to 4kg
  - On the market in 2020

Source: Toyota

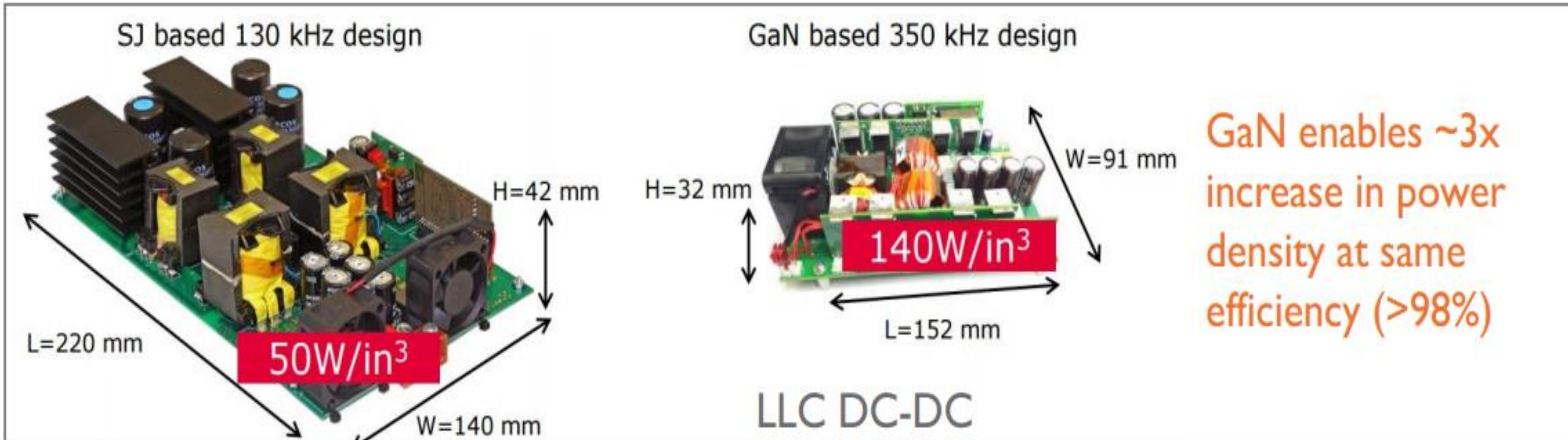
Universität Bremen

Source: ECPE Roadmap Workshop 'Power Electr. 2025', Munich, 26.03.2015

GaN & SiC for power applications



GaN & SiC for power applications



Electric vehicles

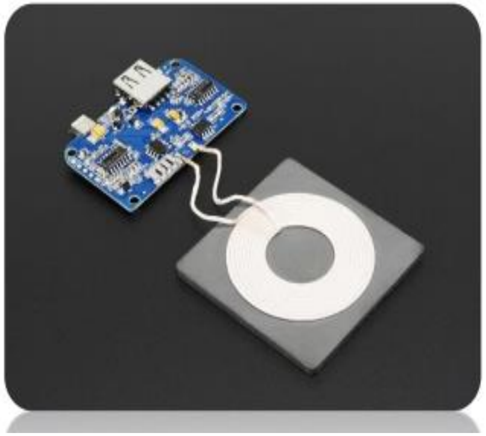
48V, 12kW motor drive inverter demo at APEC 2016:

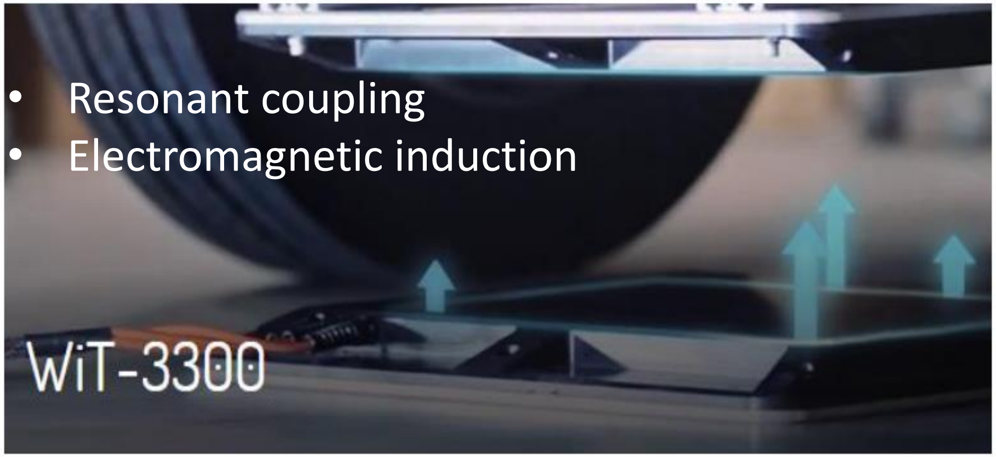
- *Air cooling*
- *3.43 kW/L*
- *10 kW generation*
- *36 GaN transistors: GaN Systems GS61008P*

48 V, 12 kW motor drive inverter for hybrid cars

Source: YOLE 2017

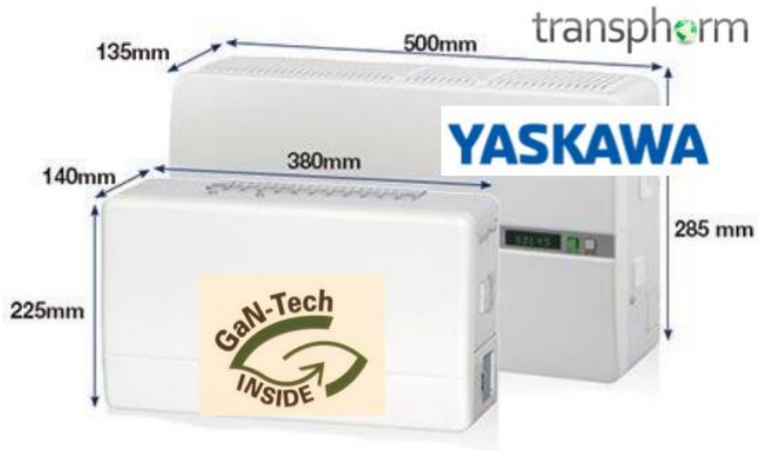
Wireless charging





- Resonant coupling
- Electromagnetic induction

PV Inverters (<10 kW)



GaN & SiC for power applications

Primary energy

- oil
- gas
- nuclear
- water
- wind
- solar cell

→ **Electricity** → DC/AC amplitude frequency →

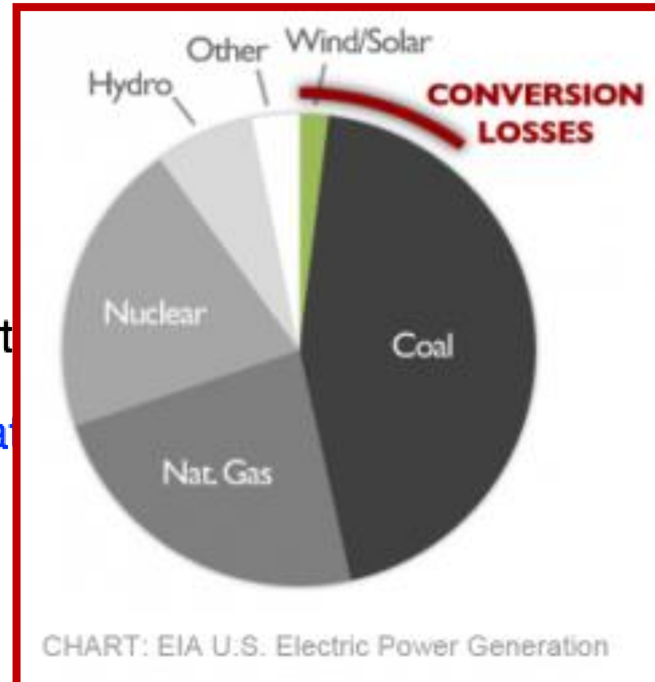
Power consumption

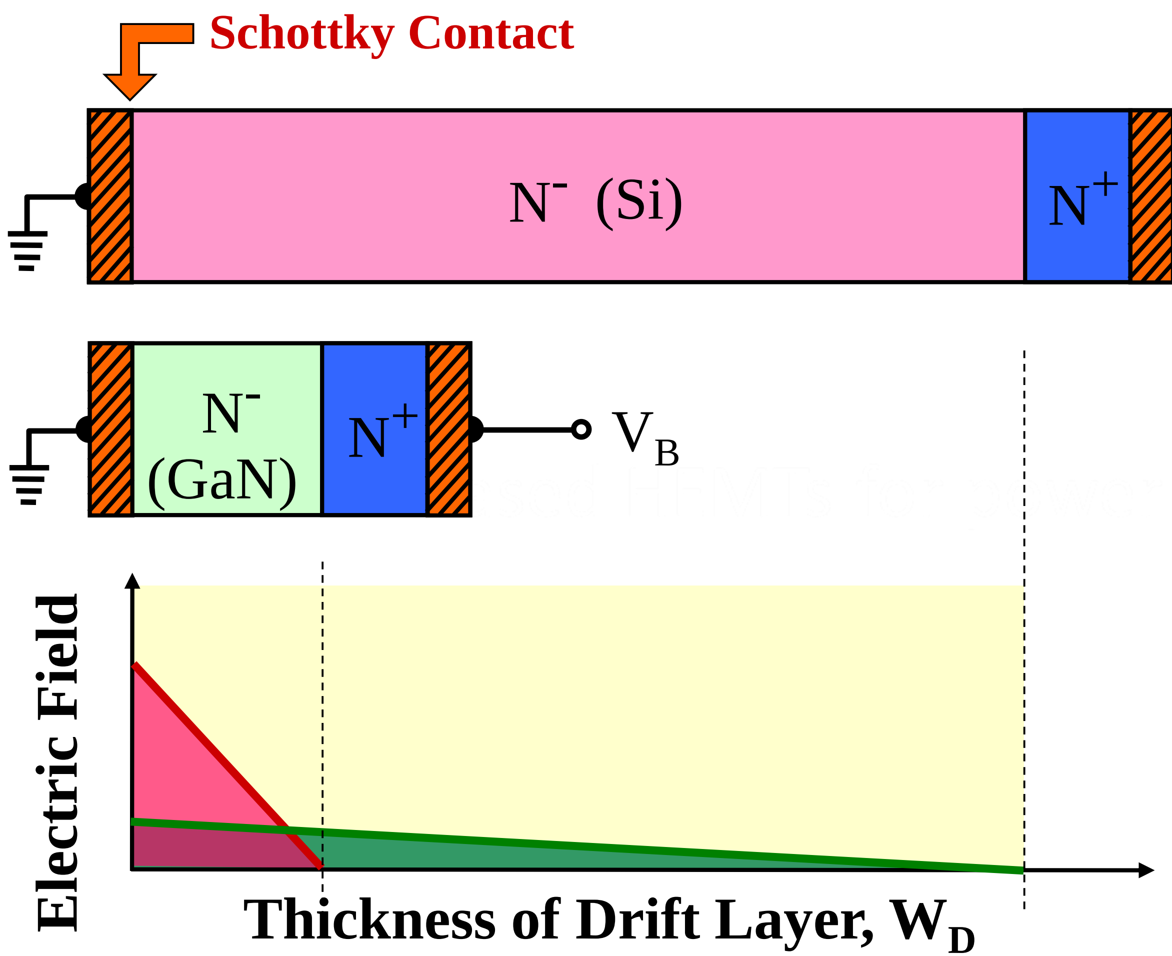
- heat
- industry power
- information communication
- transportation
- office
- home

Si-based inverter devices play important roles in power conversion process

Efficiency of present inverter : 80~ 90%
10~20% loss still remains !!
mainly due to the limitation of material propert

Ultra-low loss inverter is a key device for next-genera
energy saving society





Why nitride?

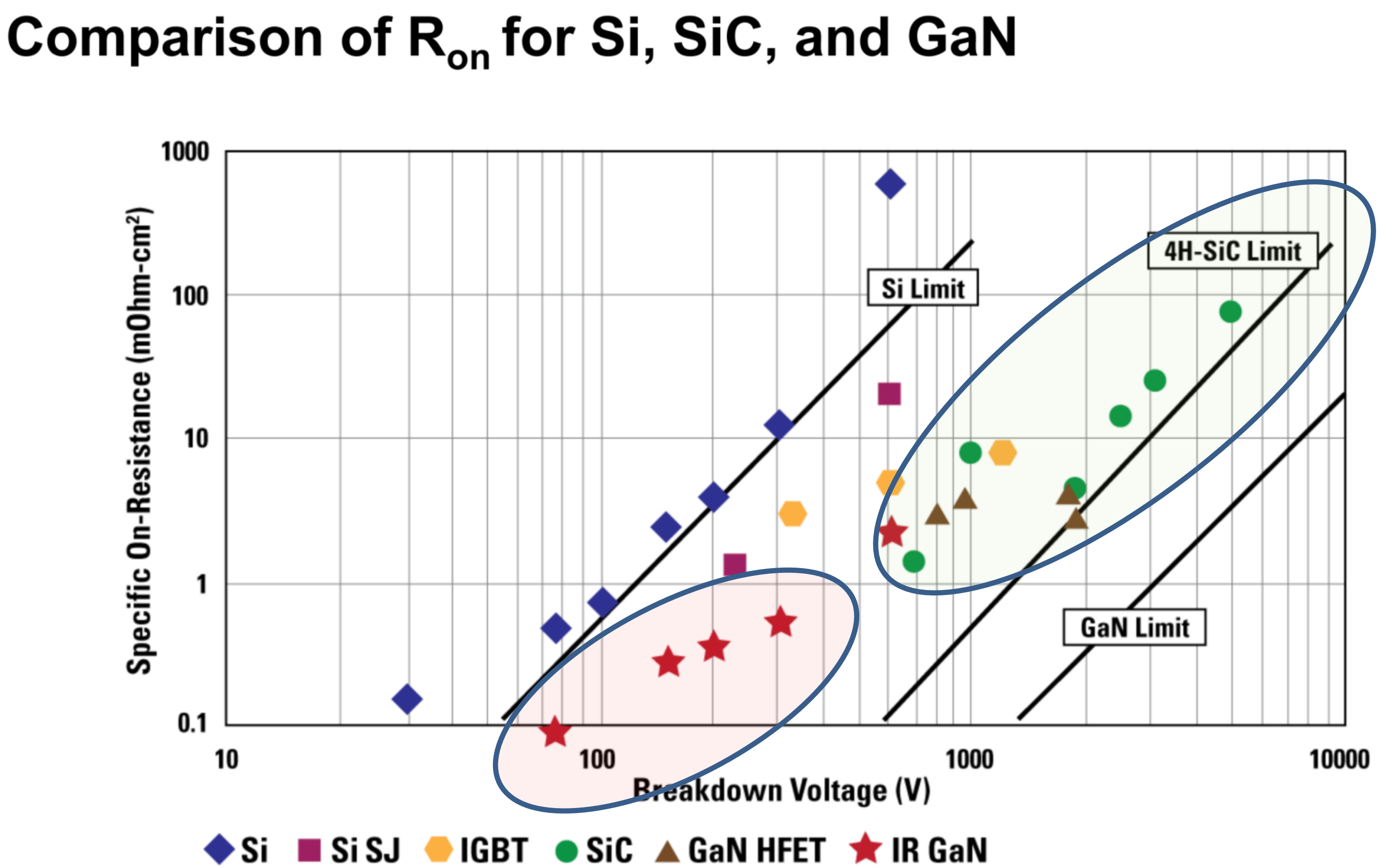
$$V_B = E_C \times W_D$$

$$R_{ON} = W_D / q \mu_n N_D$$

$$E_{max} = \left(q \times N_D \times W_D\right) / \varepsilon_{Si}$$

$$R_{ON} = \frac{V_B^{\,2}}{\varepsilon_{Si} \mu_n E_C^{\,3}}$$

Ron x10^3 lower for GaN



SiC is the semiconductor for very high voltages (> 1 kV)

GaN is the semiconductor for very low on-resistance (<1mOhm –cm^2)

Figure of Merit in semiconductors

Table 1 Figures of merit of various semiconductors

	Si	GaAs	4H-SiC	GaN
JFM	1	11	410	790
KFM	1	0.45	5.1	1.8
BFM	1	28	290	910
BHFM	1	16	34	100

JFM : Johnson's figure of merit for high frequncy devices = $(EbVs/2\pi)^2$

KFM : Keyes's figure of merit considering thermal limitation= $\kappa(EbVs/4\pi\varepsilon)^{1/2}$

BFM : Baliga's figure of merit for power switching = $\varepsilon\mu Eg^3$

BHFM : Baliga's figure of merit for high frequency power switching = μEb^2

GaN HEMT for power applications

Unbeatable

But nothing is easy,
problems are always present

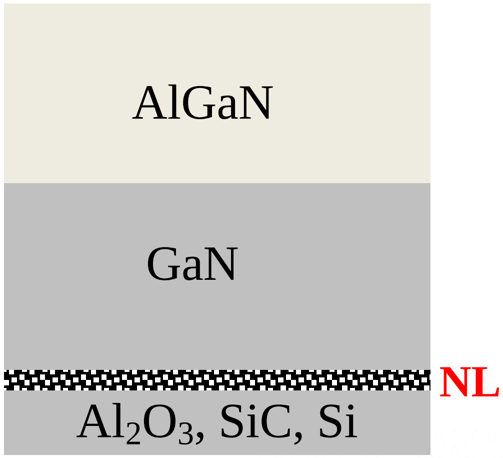
Stop dreaming, sit down and
let's analyze all the issues

Major issues of GaN-based devices:

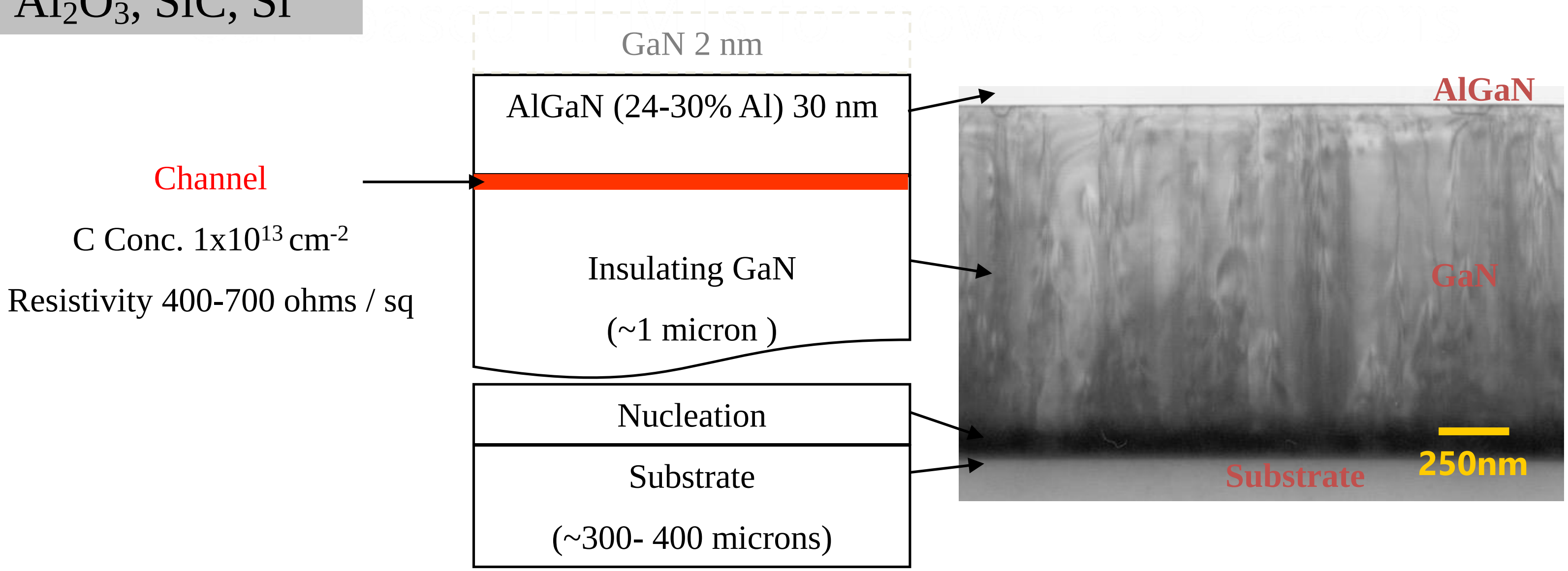
Technological and material issues

- Material (substrates, quality, reproducibility, supply chain, wafer size, maximum thickness for heteroepitaxial growth)
- Processing issues (contacts, gate, isolation)
- Normally off operation (hybrid or intrinsic)
- Isolated gate (MIS) devices
- Sustainable breakdown, Operational (rated) voltage
- Robustness (UIS, short circuit) & Reliability
- Passive components
- Packaging (high power, low inductance, cooling, surface mount, ...)
- Gate drivers
- ....

No GaN substrates available!!



- No GaN substrates free standing
- Still very high material defectivity
- Very expensive substrate/EPI
- Processing is not trivial
- Alloy contacts (no self aligned)



GaN: cost vs performance

GaN economically possible on foreign substrates only

- GaN on SI-SiC, would be the best in terms of performance, but cost is high (GaN on GaN is starting becoming attractive, early development)

GaN on Si

- very cost efficient
- Scalable to large wafer diameters 8” → mass production in CMOS line feasible
- Performance trade-off? Thermal management must be optimized

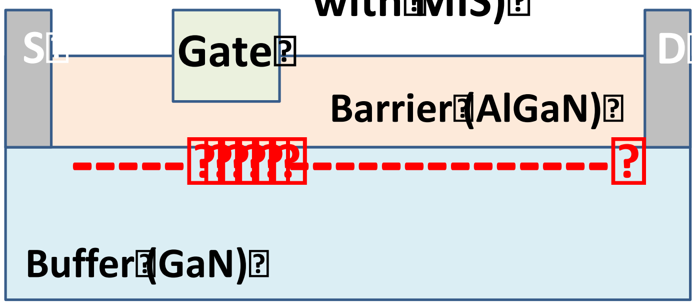
	n-type SiC	s.i. SiC	GaN bulk	Si
Lattice mismatch (%)	3.1	3.1	0	17
Availability / Price (4“, €)	700	2500	6000	80
Thermal conductivity (W/cmK)	4	4	1.3	1.48

Best performance versus **Cost efficient realization**

Joachim Würfl, “GaN Power Devices (HEMT): Basics, Advantages and Perspectives”, ECPE Workshop 2013

GaN: Normally off

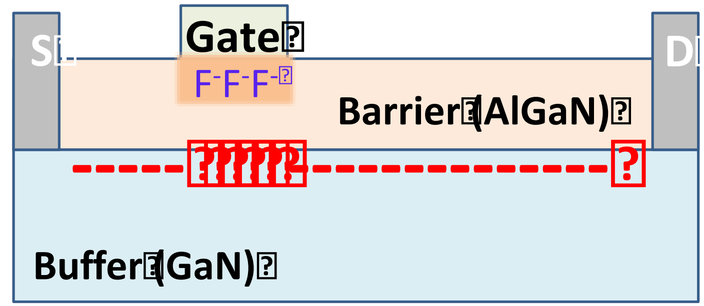
Recess on the Schottky Gate (also with MIS)



- Leakage, trapping, ...

Oka et al., IEEE EDL 29, 668 (2008)

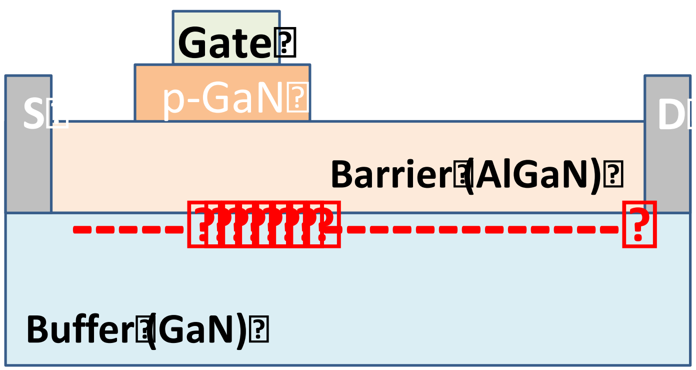
Fluorine Implantation



- Vth instabilities, leakage, ...

Feng et al., IEEE EDL 31, 2386 (2010)

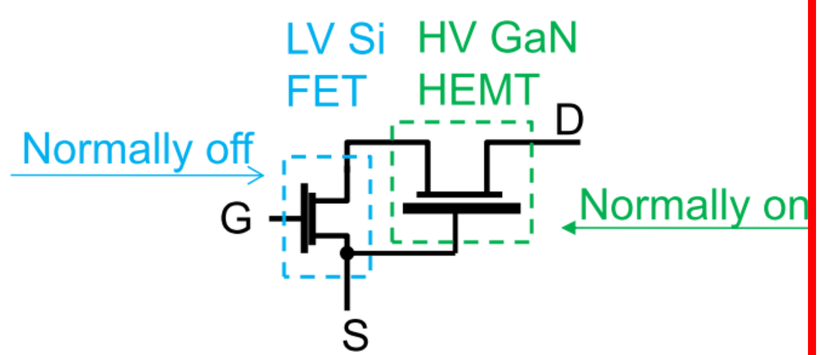
p-type Gate



- Need for p-type, Vth~1.5 V, ...

Uemoto et al., IEEE TED 54, 3393 (2007)

Cascode configuration



- Combined Si/GaN, MIS gate, ...

Eg. Transphorm, ...

GaN: Vertical vs Lateral GaN HEMT

IOP Publishing | Semiconductor Science and Technology
Semicond. Sci. Technol. **28** (2013) 074014 (8pp) | doi:10.1088/0268-1242/28/7/074014

INVITED REVIEW

Current status and scope of gallium nitride-based vertical transistors for high-power electronics application*

Srabanti Chowdhury[1], Brian L Swenson[2], Man Hoi Wong[3] and Umesh K Mishra[4]

Semicond. Sci. Technol. **28** (2013) 074014 | Invited Review

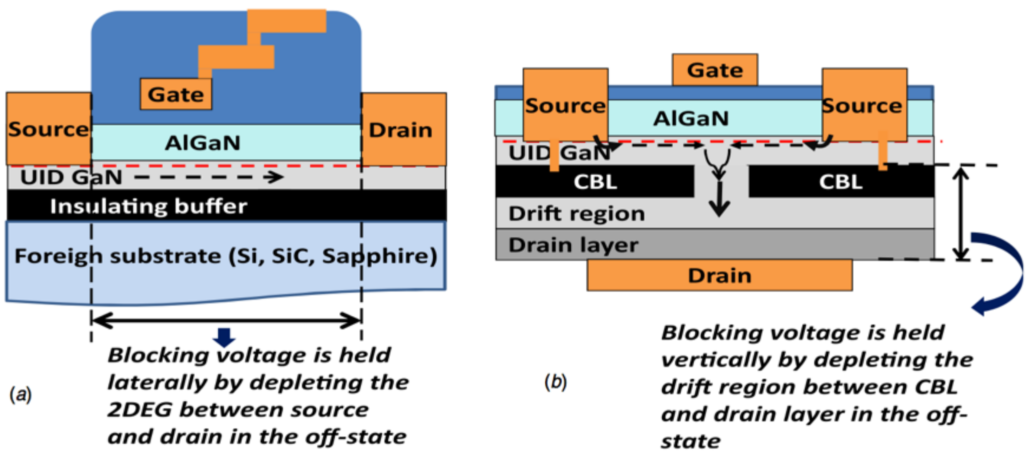
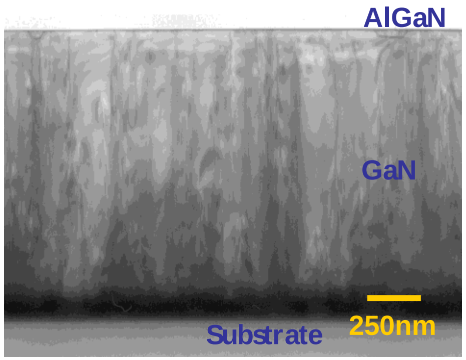


Figure 4. (*a*) A lateral AlGaN/GaN power HEMT (*b*) A vertical transistor using AlGaN/GaN layer structure on bulk GaN drift layer and substrate.



Vertical geometry is preferred over lateral geometry to enable

- **Higher Blocking voltage**
- **Higher current density**
- **Smaller chip size and potentially lower cost**

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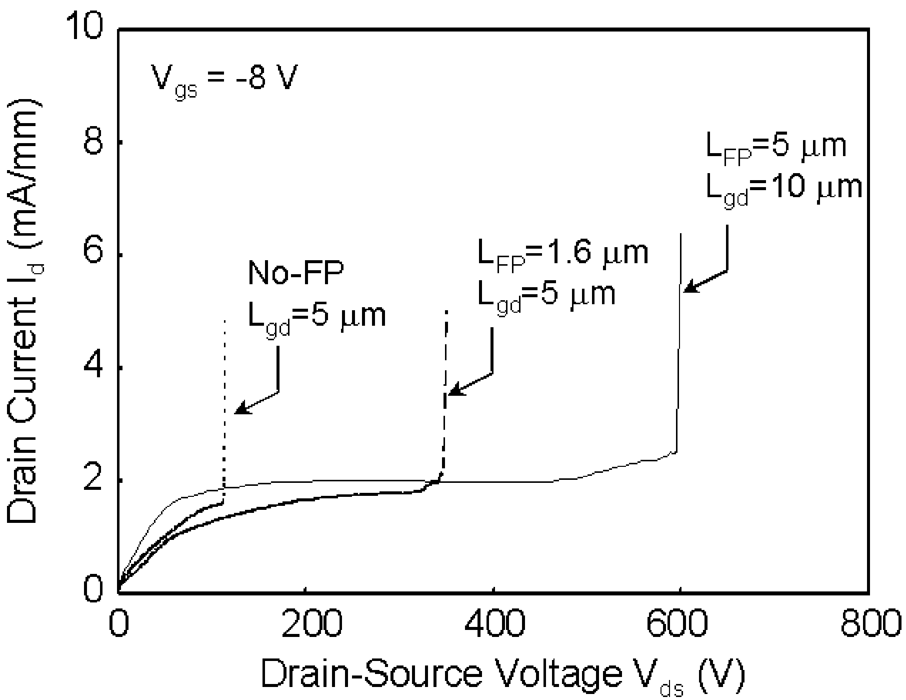
  - A database for deep levels in GaN
- Permanent degradation mechanisms
  - Degradation in off-state → Schottky-gate
  - Degradation under FW bias → p-GaN gate
  - Degradation under FW bias → MIS gate
- Conclusions

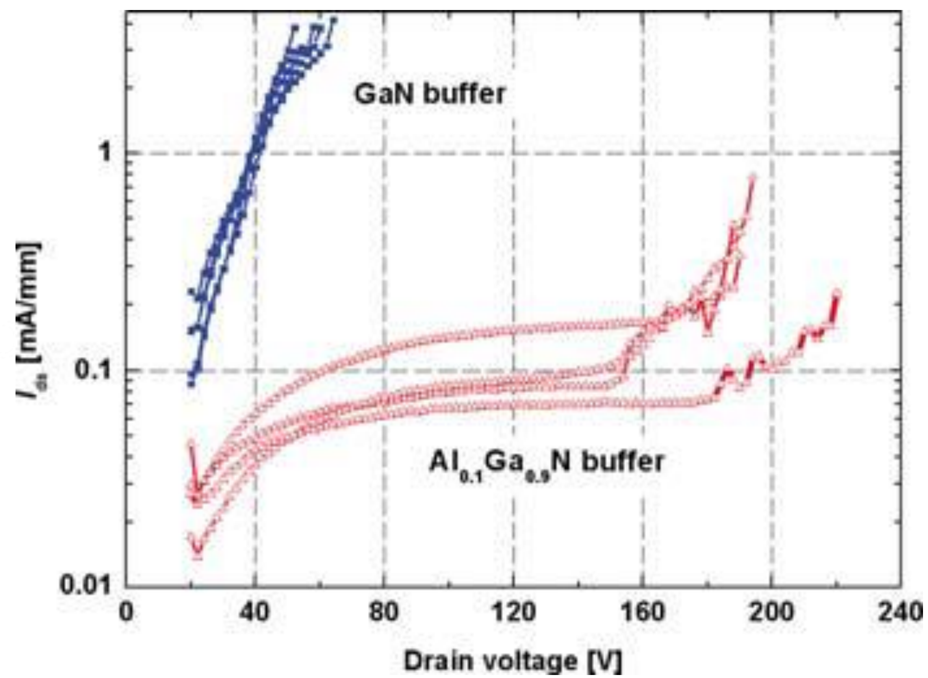
Breakdown: abrupt vs gradual

Steep increase → Leads to catastrophic failure



S. Wataru et al. IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 50, NO. 12, DECEMBER 2003

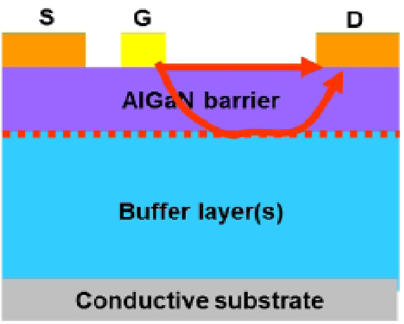
Subthreshold conduction → Gradual increase in drain current (limit, e.g. 1 mA/mm) → A problem for high VDS operation



Wuerfl et al., Microelectronics Reliability 51, 1710, 2011

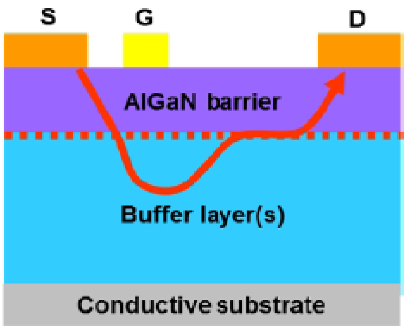
Breakdown mechanisms in HEMTs

(1) Leakage currents origination from gate structure



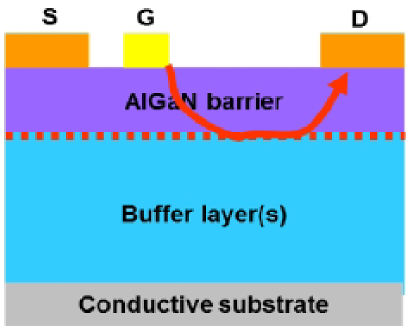
- Surface leakage e.g at passivation layer interfaces [13]
- Leakage current through barrier layer [8]
- Strain induced leakage [14]
- Often as a result of degradation effects [8, 15]
- No classical breakdown effect, however prevents high voltage operation due to excessive gate leakage

(2) Punch through effect



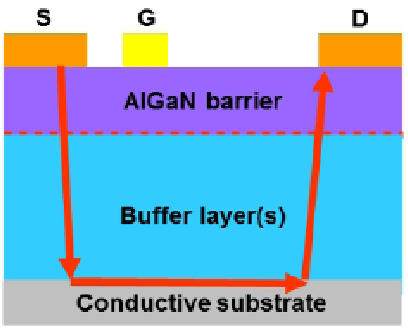
- Electrons bypass control region at high drain bias levels and gate pinch-off condition [6, 7]
- No classical breakdown effect, however limits device operation due to high subthreshold current

(3) Breakdown along channel region



- Classical breakdown effect, scales with increasing gate to drain distance
- Very abrupt breakdown characteristics
- Breakdown strength mainly dependent on buffer properties

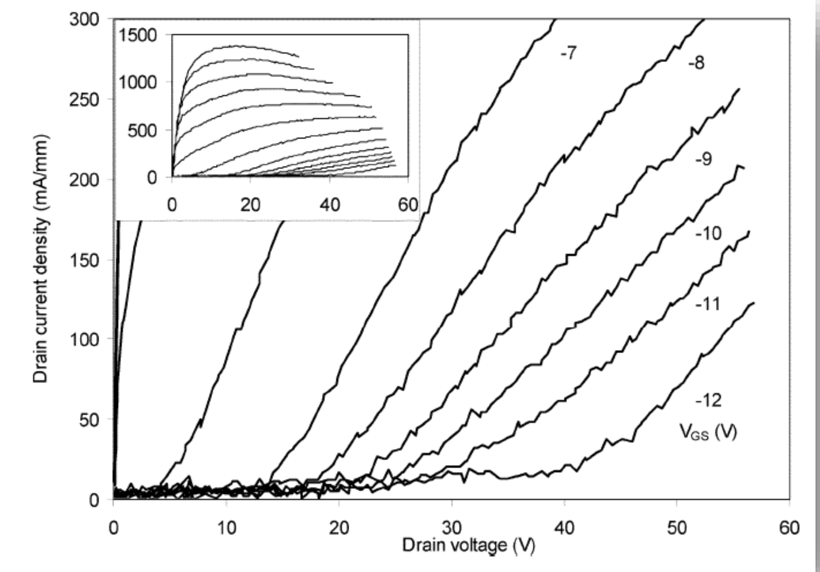
(4) Breakdown through buffer layer

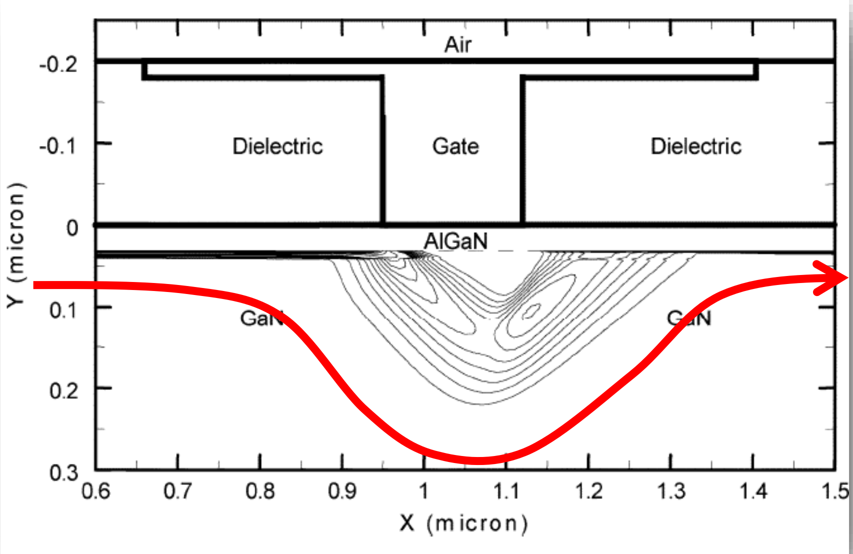


- Ultimately limiting device maximum operation by leakage through buffer layer to conductive substrate [16, 12]
- Depends on buffer thickness and buffer technology
- Also depends on surface contact technology
- Matter of high voltage reliability concerns

Würfl et al., ECS 2013

Lateral breakdown in HEMTs?



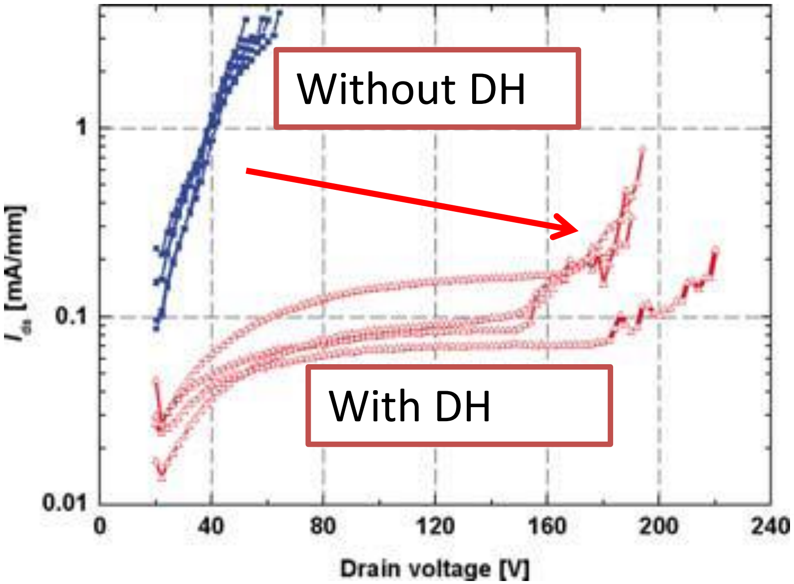


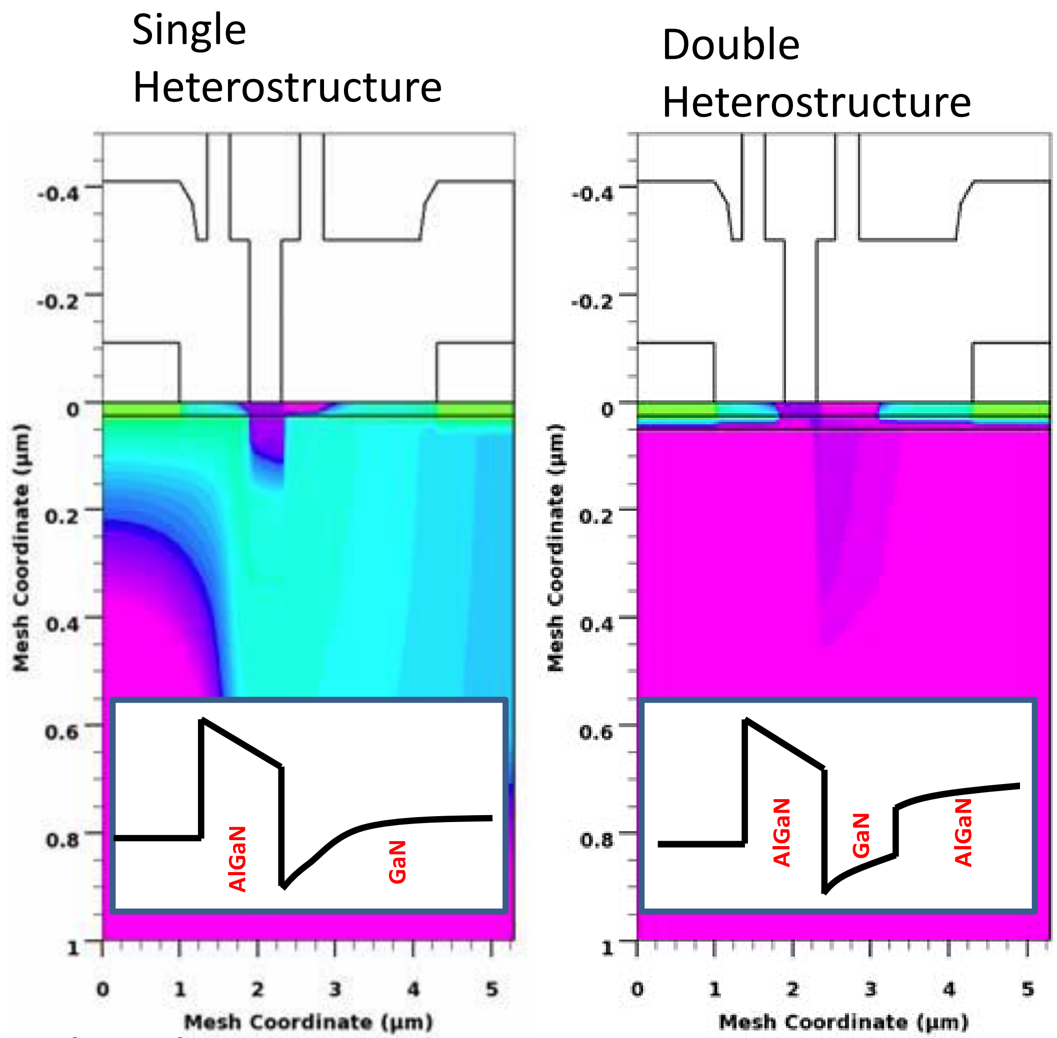
For high VDS levels → The poor confinement of charge at the AlGaN/GaN interface results in current flow within the bulk of the GaN layer → Punch-through, or space-charge injection

The confinement can be achieved by compensating the inherent free carrier present in the UID GaN. Today it can be done by **introducing C or Fe** .... With some unhappy consequences → other solutions?

Uren et al., IEEE TED 53, 395 (2006)

Lateral breakdown in HEMTs?



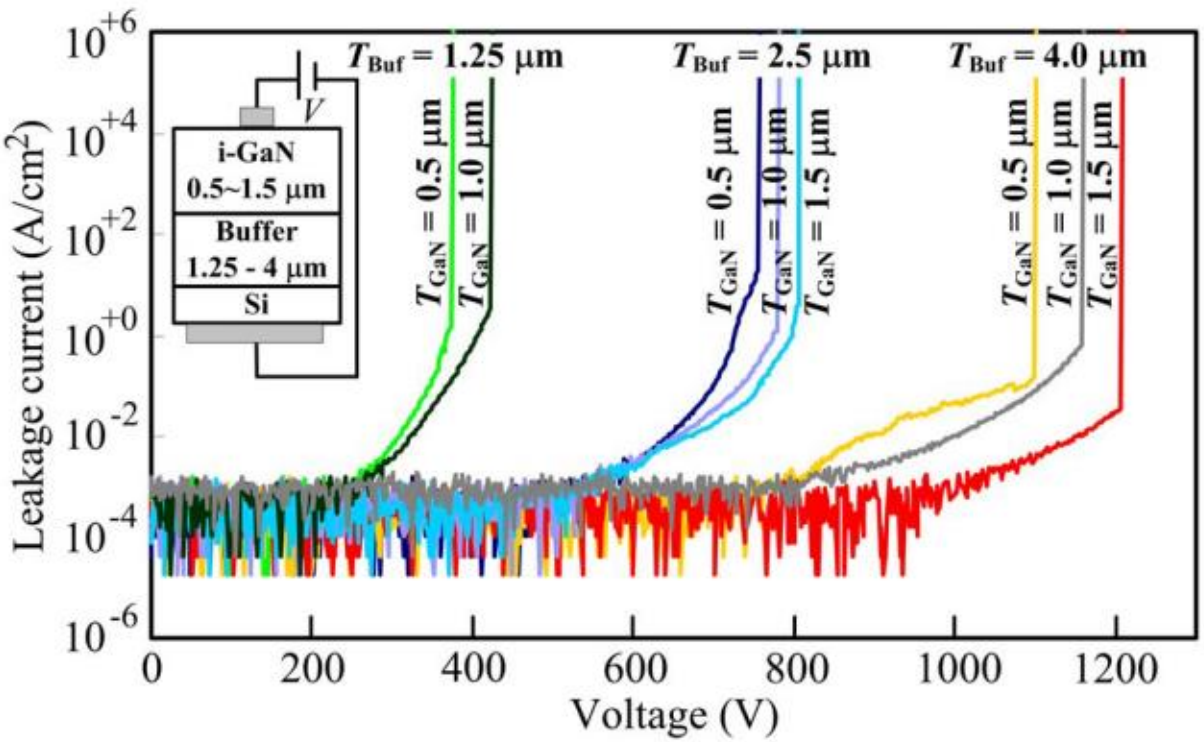


Double Heterostructure largely reduces Punch-through

Wuerfl et al., Microelectronics Reliability 51, 1710(2011)
Bahat-Treidel et al., Phys. Status Solidi C 6, 1373 (2009)

False color: electron density, VG=-6, VD=30

Vertical Breakdown: Buffer thickness vs GaN thickness

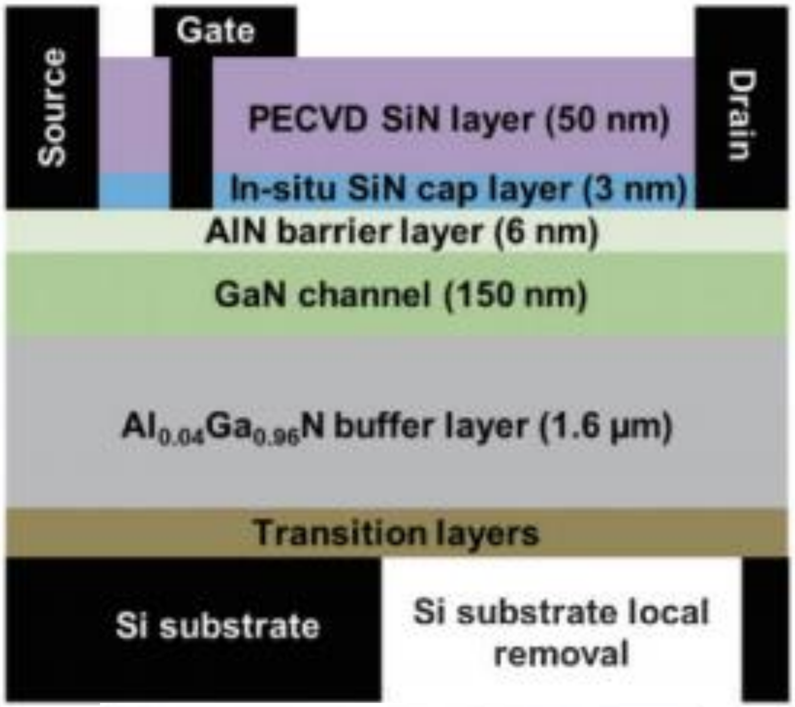


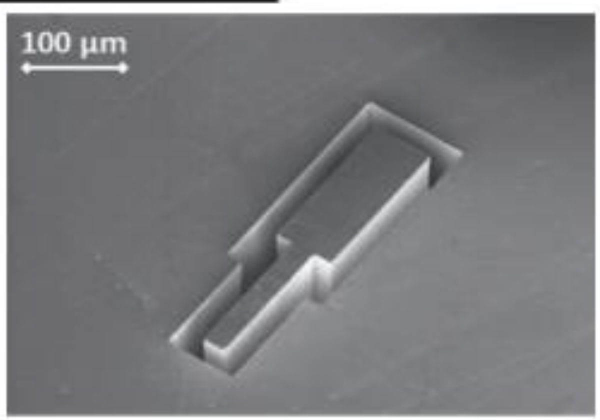
- For a particular T_{Buf} of 1.25 μm, there was a little increase in breakdown as T_{GaN} increased from 0.5 to 1.0 μm.
- However, fixing T_{GaN} at 0.5 μm and varying T_{buf} showed a very large increase in the breakdown values

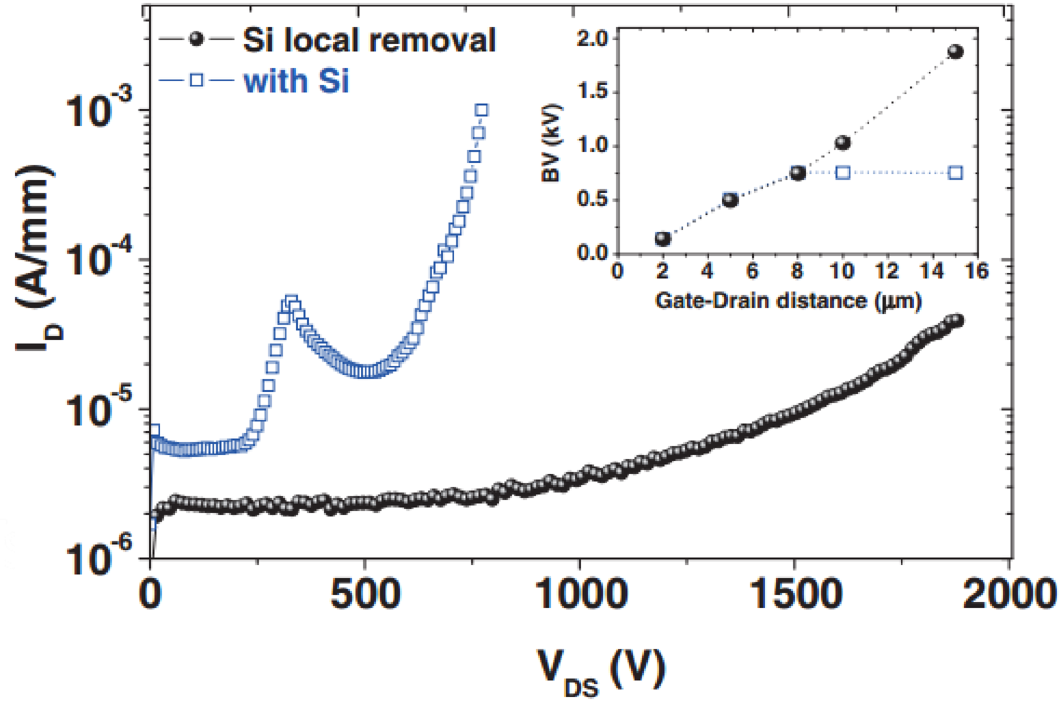
Rowena et al., IEEE EDL 32, 1534 (2011) "The breakdown field was calculated as 2.3 MV/cm against an ideal theoretical value of 3.0 MV/cm. Therefore, growing i-GaN on a thick buffer strengthens the buffer and Si junction, enabling the growth with low dislocation density, offering high resistance" → XRD show that TDD decrease gradually for GaN grown on thick buffers

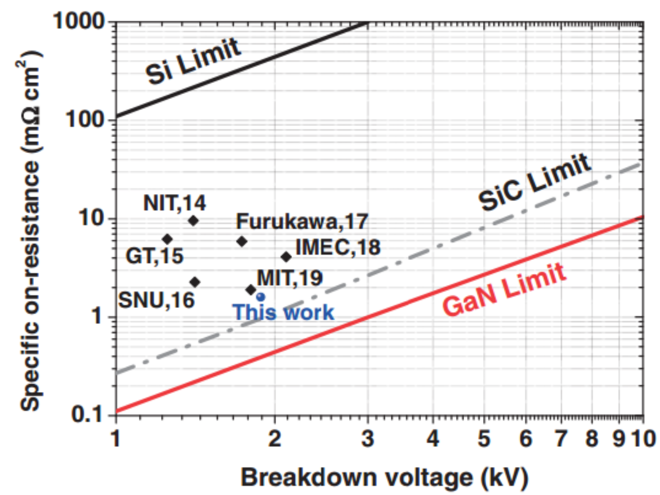
The flow of leakage currents through a large density of dislocation becomes more significant in the case of thin buffers for in- creased contact area

Local substrate removal to increase BDV









Herbecq, Appl. Phys. Express 7, 034103 (2014)

Outline

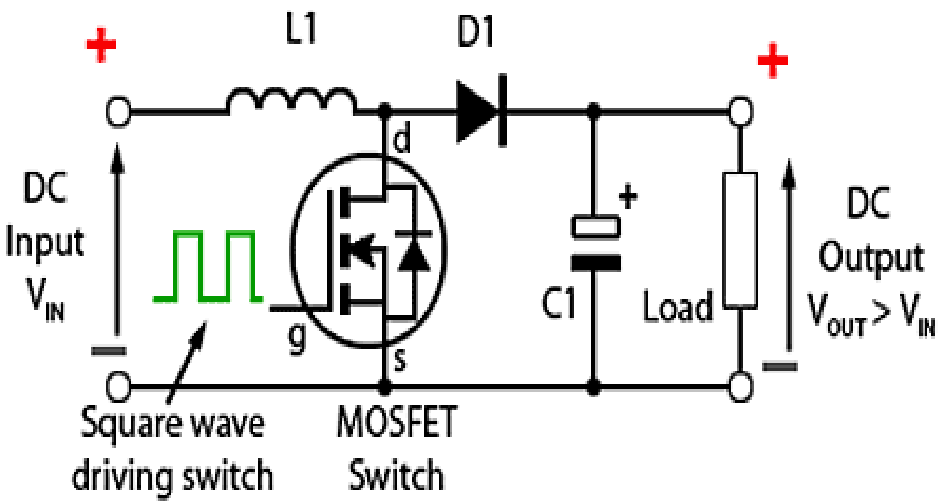
- Introduction on GaN-based HEMTs
- Breakdown mechanisms at high drain bias

- Parasitic (trapping) mechanisms → recoverable degradation
  - Current/Ron collapse
  - Methods for analyzing defects in GaN-HEMTs
  - A database for deep levels in GaN

- Permanent degradation mechanisms
  - Degradation in off-state → Schottky-gate
  - Degradation under FW bias → p-GaN gate
  - Degradation under FW bias → MIS gate

- Conclusions

GaN Power Devices operation - BOOST Power Converter



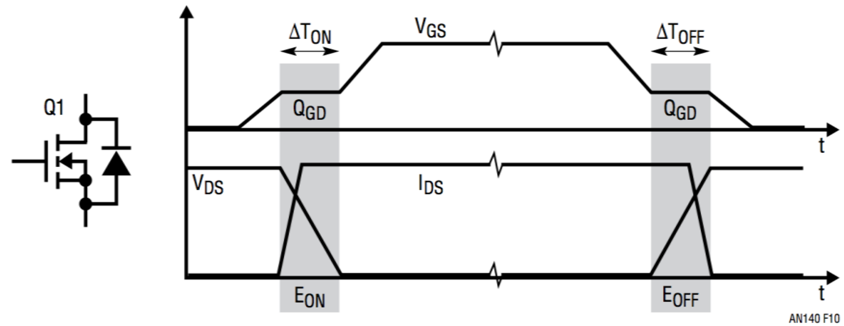
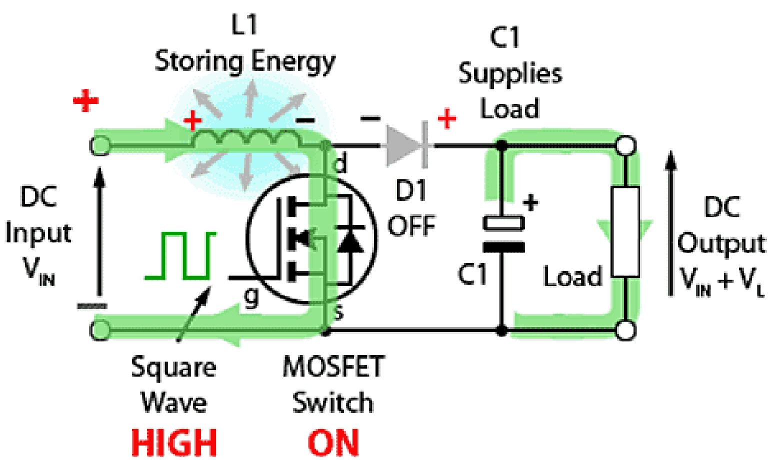
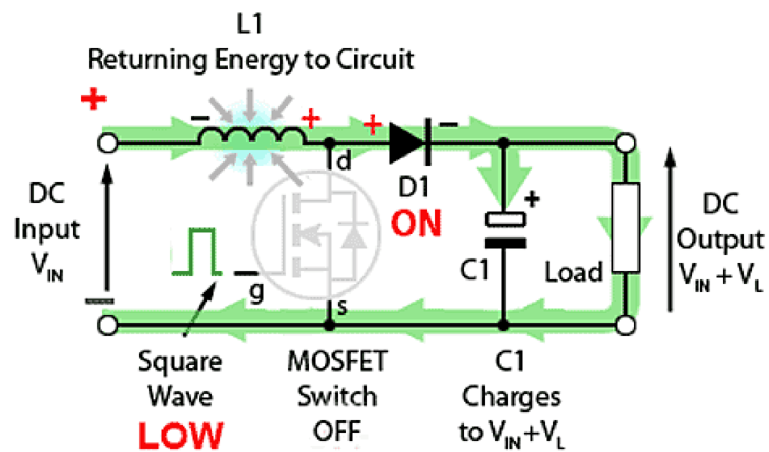
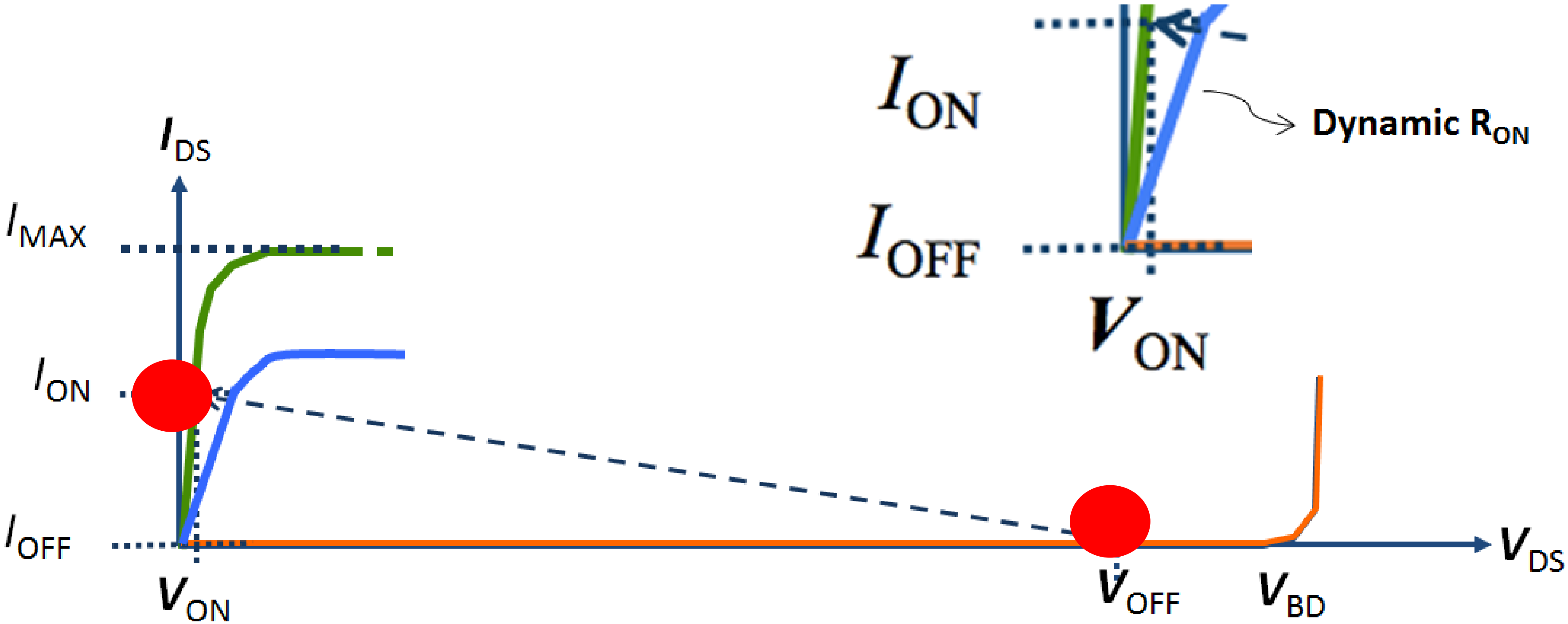


Figure 10. Typical Switching Waveform and Losses in the Top FET Q1 in the Buck Converter



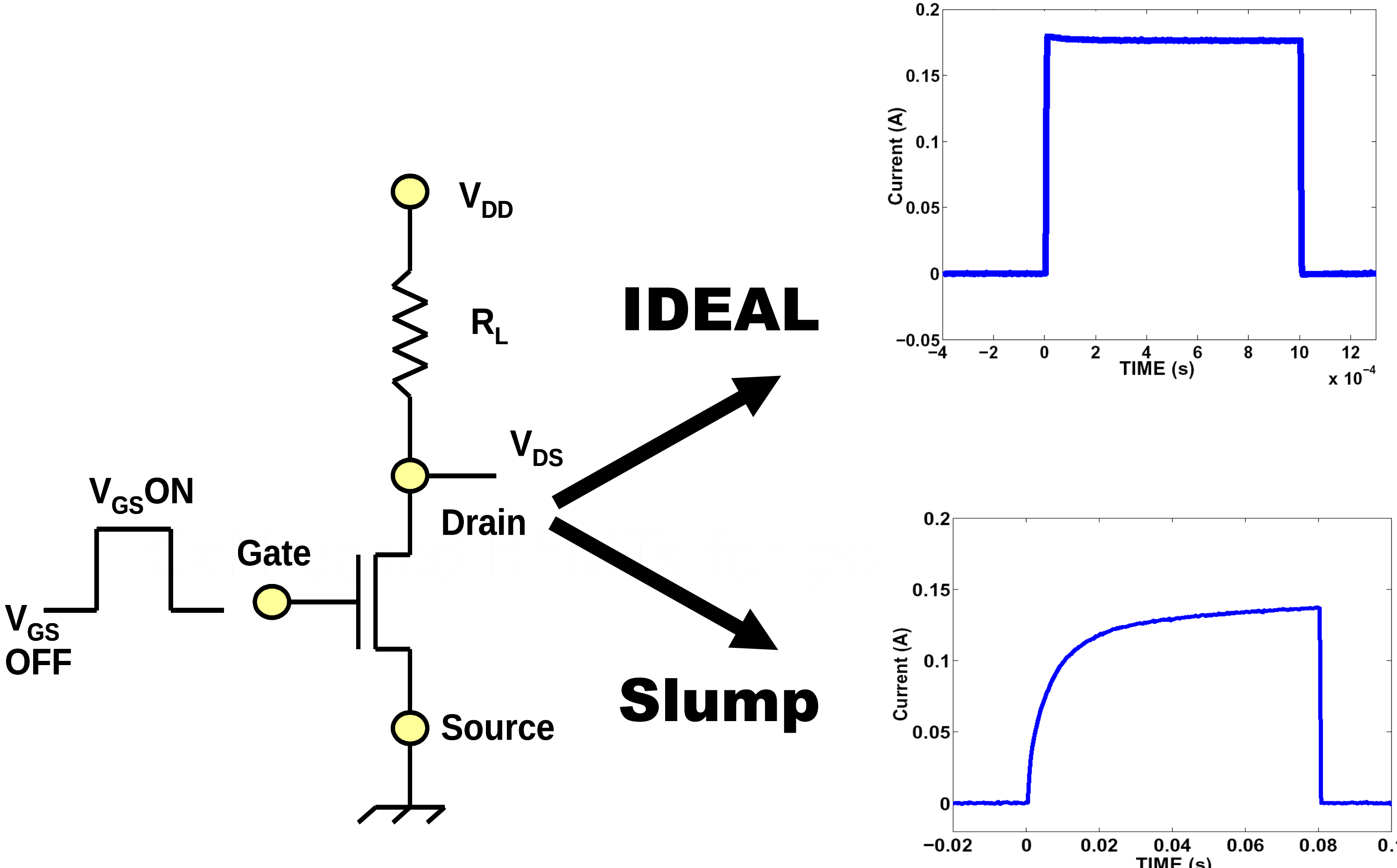


Requirements for power transistor



1. **High max current**
2. **Low Ron → Minimize losses!**
3. **High breakdown voltage ≅ 1.2 kV**

Issues in GaN-based HEMTs: Trapping

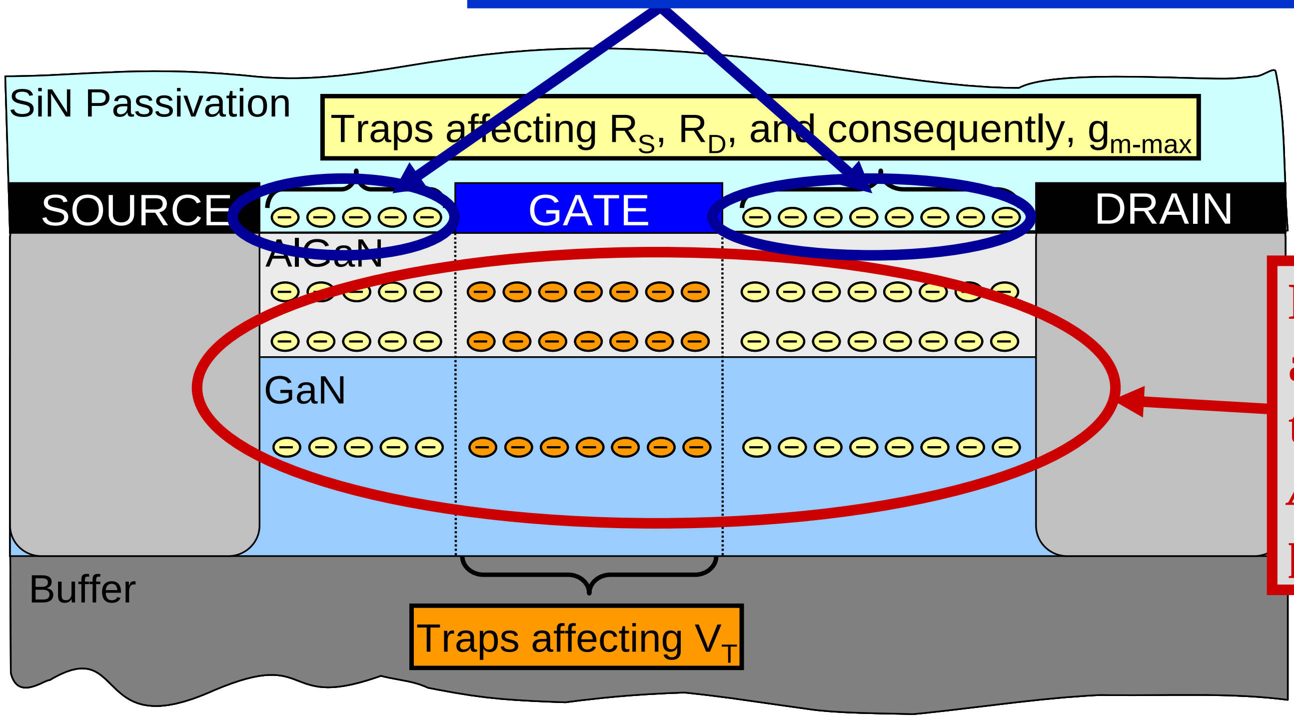


Gate-lag turn on measurement

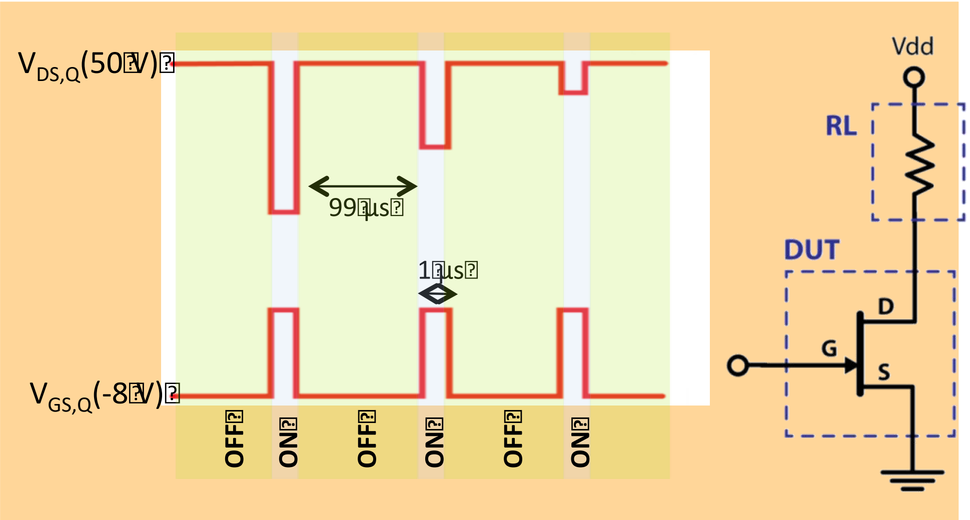
When a HEMT is switched on after a trapping phase → current shows an exponential transient before reaching steady-state value (de-trapping transient)

Traps-related issues

surface traps affect transconductance through series resistance increase they can not affect pinch-off voltage, unless Lg is fairly short



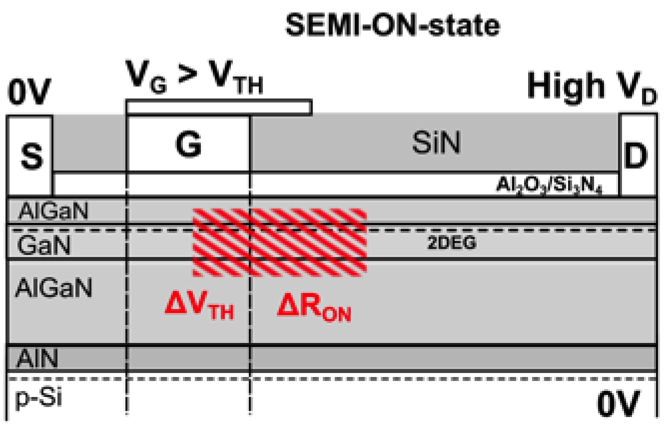
Epi traps affect both transconductance *AND* pinch-off voltage

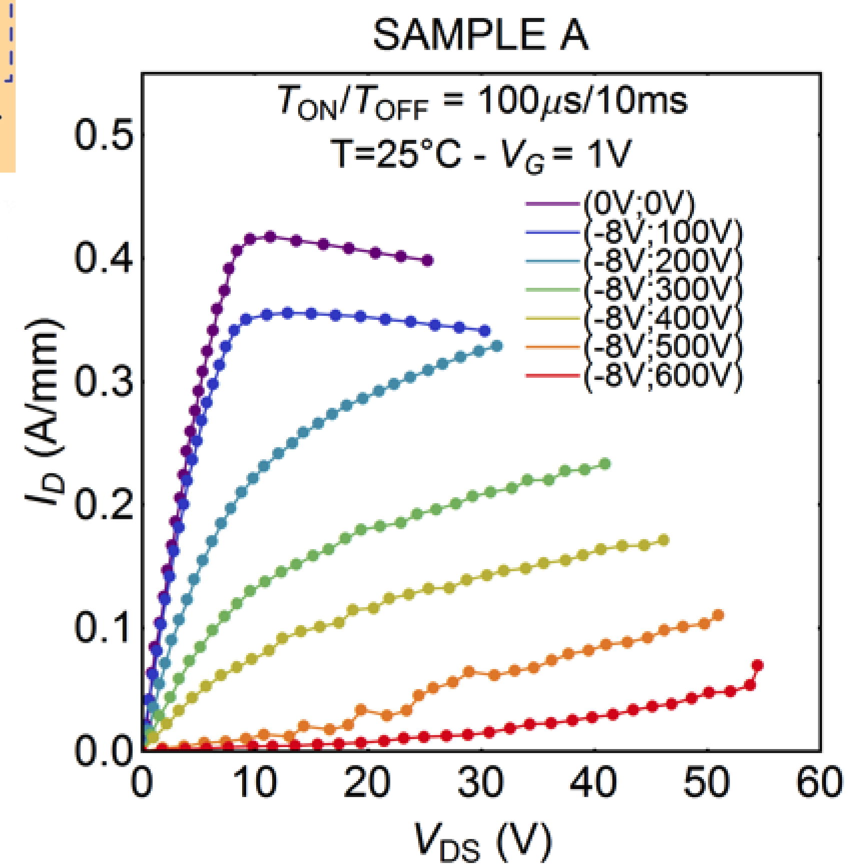


Double Pulse

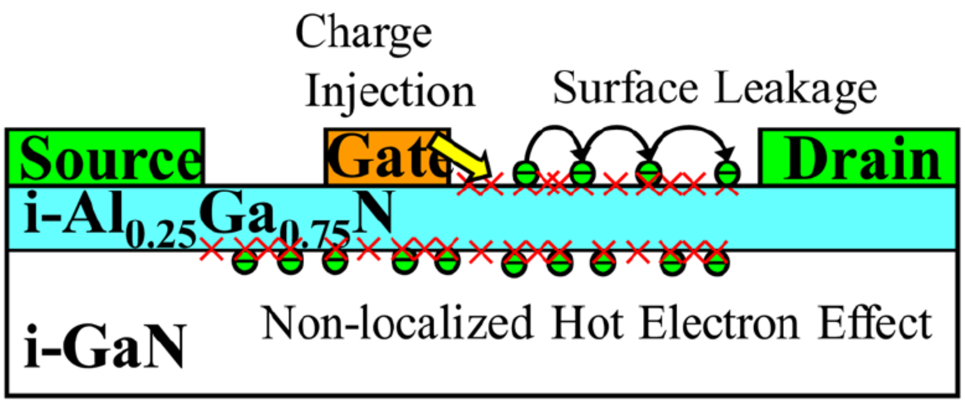
Investigate the influence of trapping phenomena on I_D-V_D and I_D-V_G dynamic characteristics.

Identify the I_{DS} current dispersion in terms of dynamic V_{TH} shift and dynamic g_m collapse





Trapping in the gate-drain access region

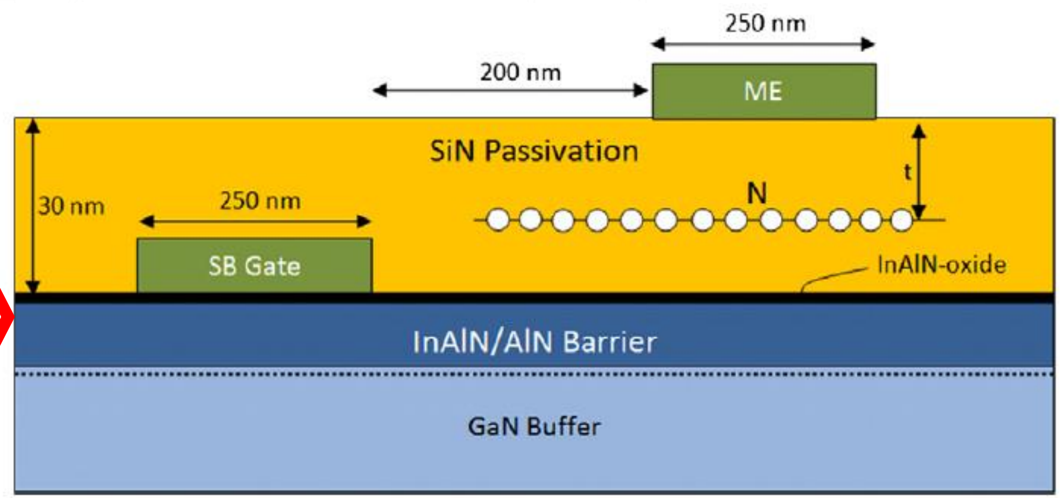


Trapping mechanisms:

- **Charge injection at surface**
- **Charge injection towards interface states**

Hu et al., JAP 111, 084504 (2012)

Electrons from the gate to passivation or interface states + hopping (Ostermaier, Microelectronics Reliability 52 (2012) 1812–1815)



Effects of trapping between gate and drain: Virtual Gate

- If there exists negative charge on the surface, the surface potential is made negative, depleting the channel of electrons and leading to extension of the gate depletion region

- The effect of surface negative charge is to act like a negatively biased metal gate

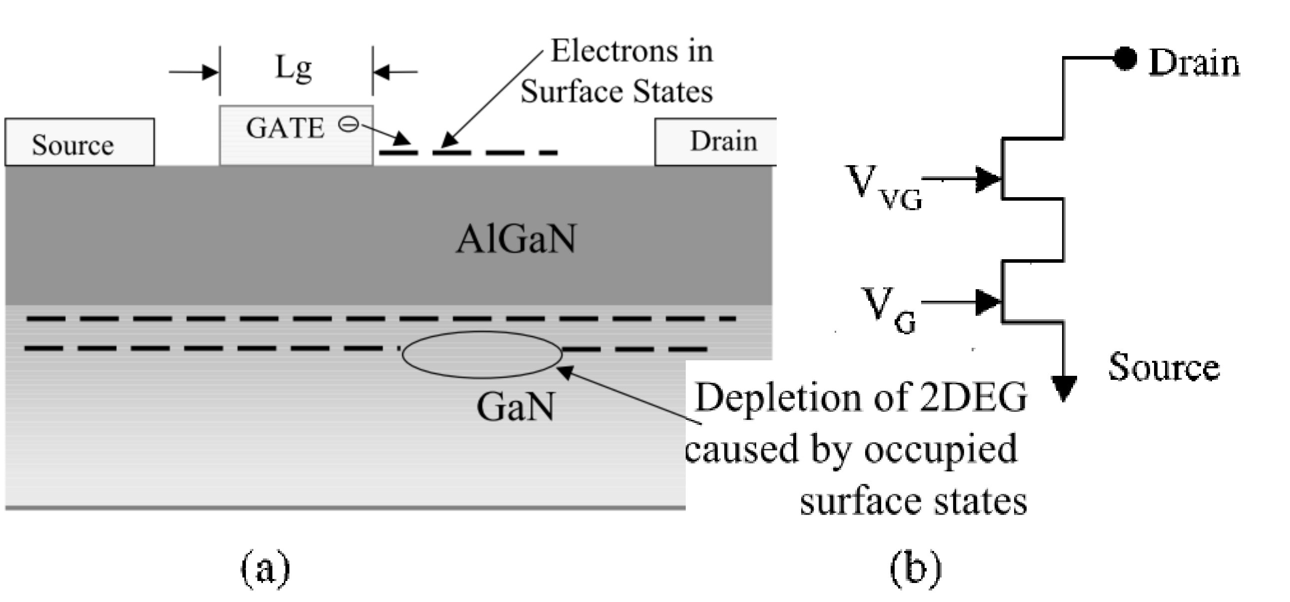
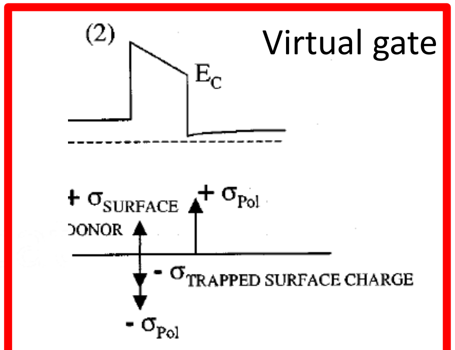
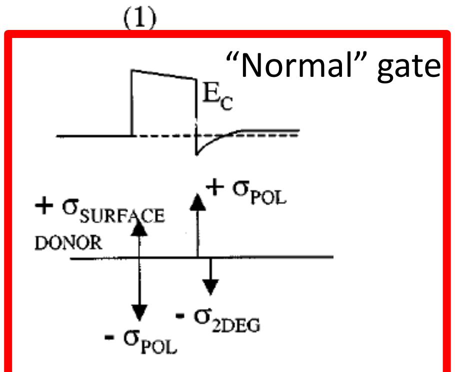


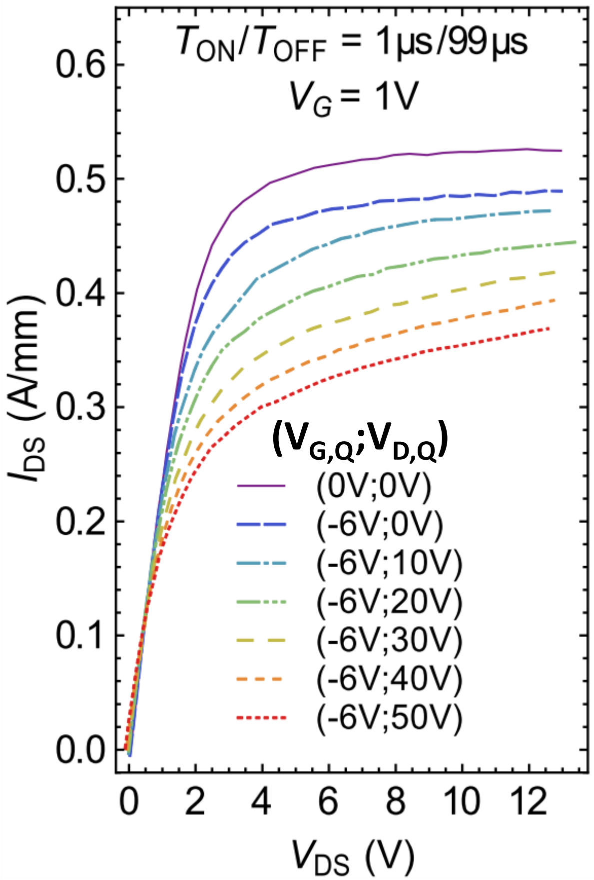
Fig. 3. Model of the device showing the location of the virtual gate and schematic representation of the device including the virtual gate.

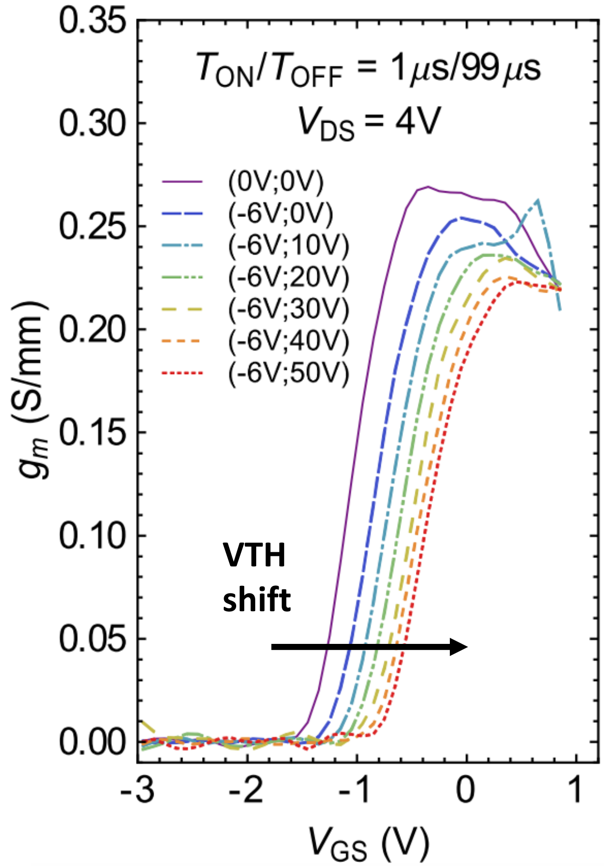




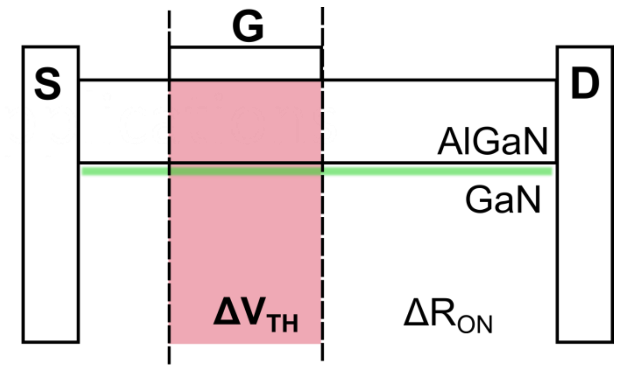
Vetury et al., IEEE-TED 48, 560, 2001

Current collapse → Trapping under the gate





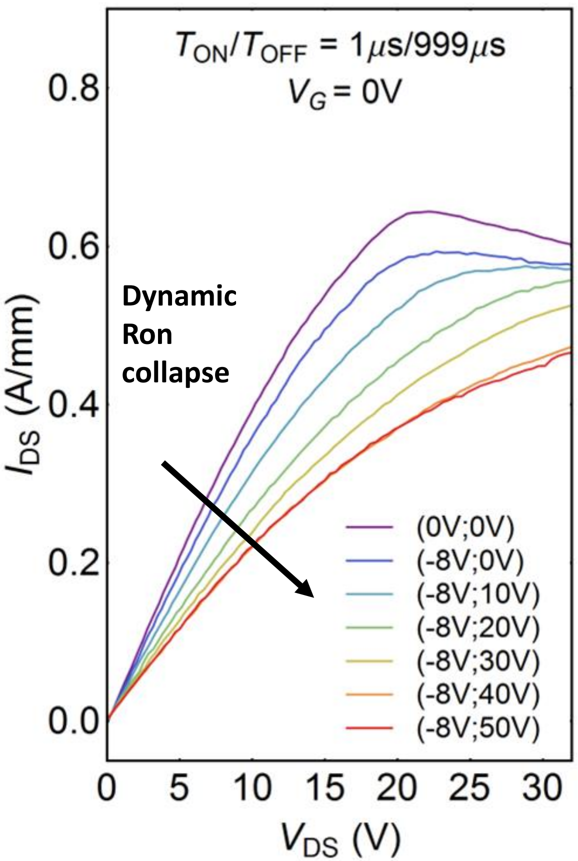
Current collapse mainly caused by **V_{TH} shift** can be ascribed to charge-trapping **below the gate region**.

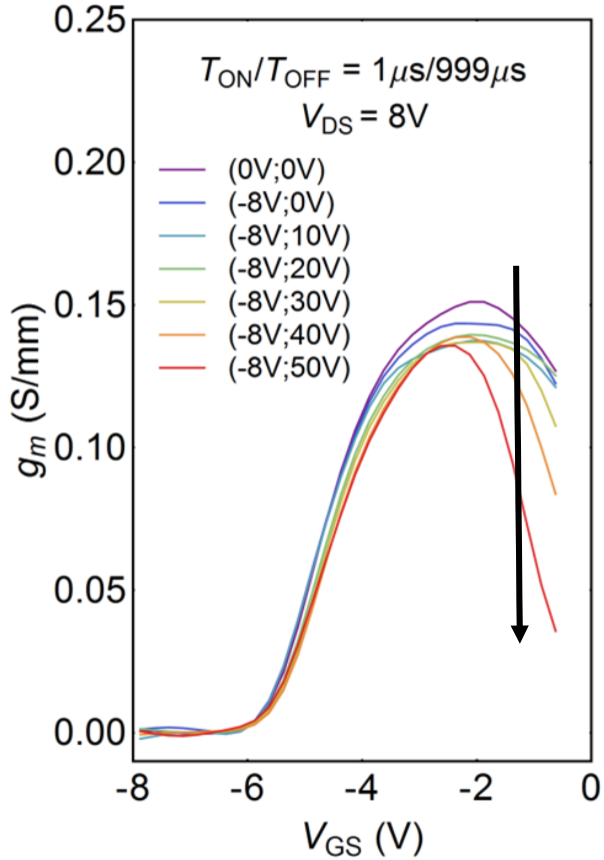


Bisi et al., IEEE TED 60, 3166 (2013)

Measurements are carried out starting from various quiescent bias points, in the off-state

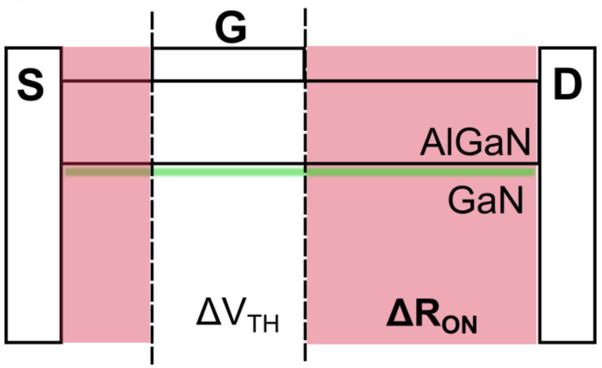
Current collapse → Trapping in the access region





Bisi et al., IEEE TED 60, 3166 (2013)

Current dispersion mainly caused by **dynamic R_{ON}** and **g_m transconductance collapse** can be ascribed to charge-trapping throughout the **extrinsic access regions**, either at the surface or within the epitaxial layers.



Measurements are carried out starting from various quiescent bias points, in the off-state

Double pulse → provide little informations

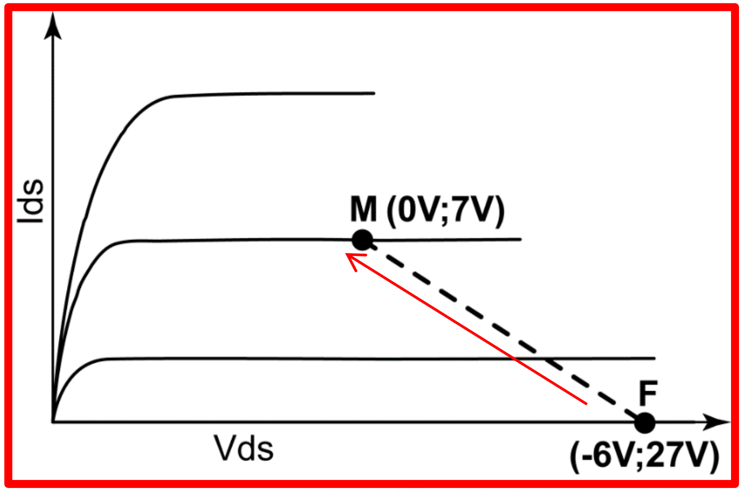
Double pulse measurements provide information about charge trapping and the presence of current collapse, however , it does not tell you much about the nature of the collapse:

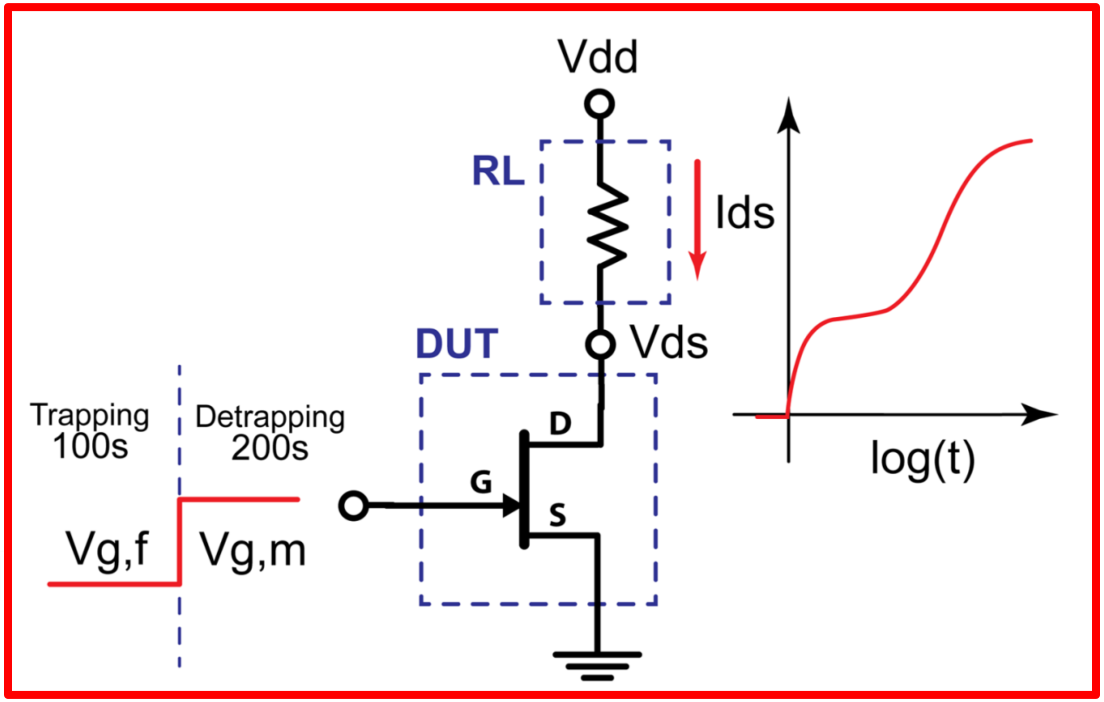
- Where are the traps? only little information
- Which are the traps properties (Ea and cross section)
- Which is the origin of traps (material, impurities, defects)

Can we do better?

YES with DLTS or I-DLTS

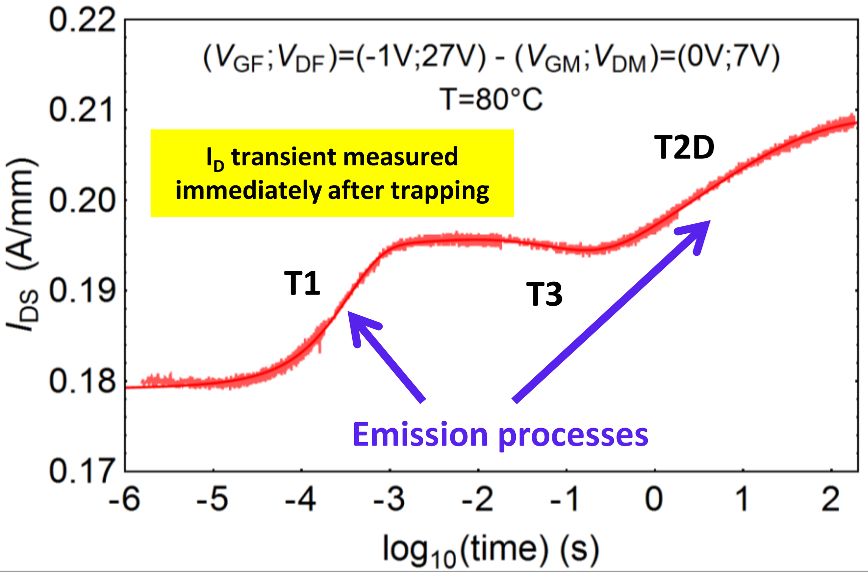
Characterizing traps: Drain Current Transient Technique

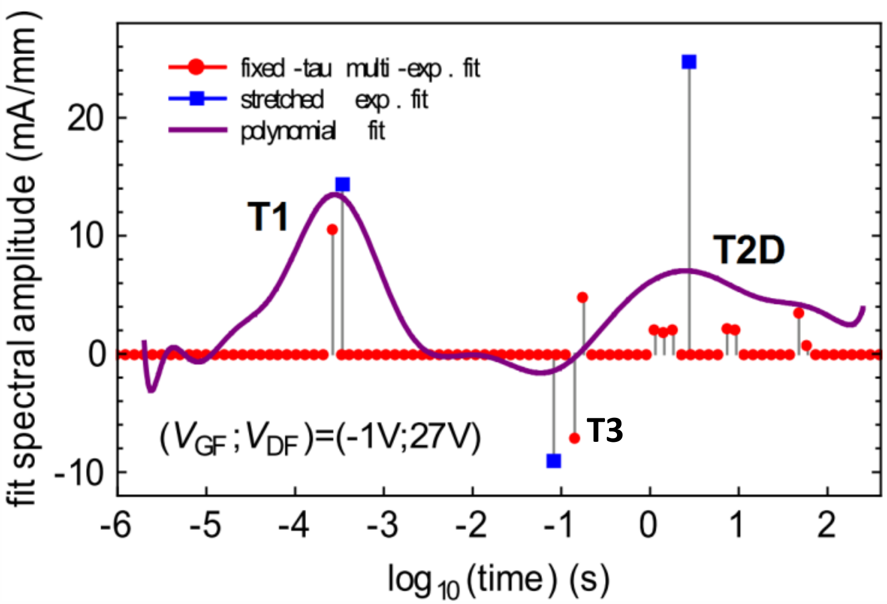




- Drain Current Transient analysis → kinetics of the (de)trapping processes
- The device is kept in a trapping condition (typically in the off-state) for a long time (e.g. 100 s) → when the HEMT is switched on, drain current shows an exponential increase, due to the release of trapped charge (time constant of the de-trapping process)
- The signatures of the deep-levels – activation energies and capture cross-sections – and their localization can be obtained by carrying out the measurements under different bias conditions and different temperatures

Characterizing traps: Drain Current Transient Technique





The thermal emission of trapped-carriers is governed by (nearly) exponential laws

Goal → To extrapolate the time constant of the de-trapping process!

- **Stretched multi-exponential**

$$I_{DS}(t) = I_{DS,\infty} - \sum_{i}^{N} A_i e^{-\left(\frac{t}{\tau_i}\right)^{\beta_i}}$$

- **Multi-exponential with fixed-τ-set**

$$I_{DS}(t) = I_{DS,\infty} - \sum_{i}^{100} A_i e^{-\frac{t}{fixed,\tau_i}}$$

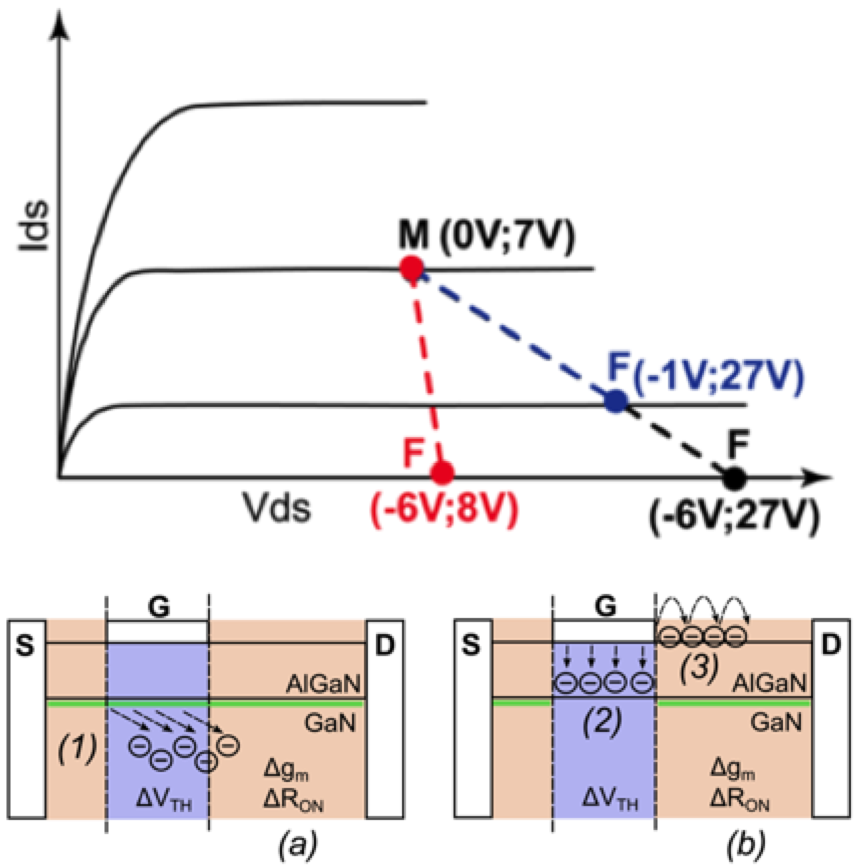
- **Peak of the transient derivative** (fitted by polynomial function)

D. Bisi et al, "DL characterization in GaN HEMTs", IEEE TED Oct. 2013

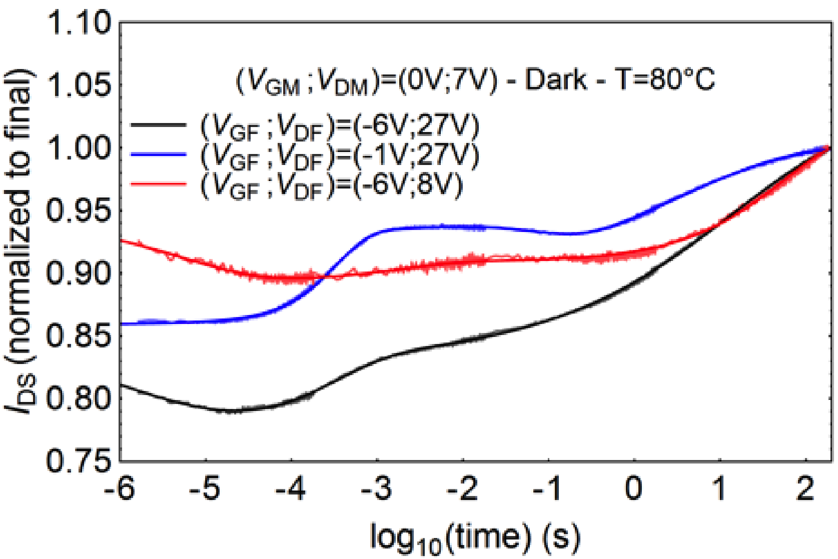
Characterizing traps: Drain Current Transient Technique

Properly selecting gate- and drain- voltage during the trapping phase promotes trapping phenomena in different device region:

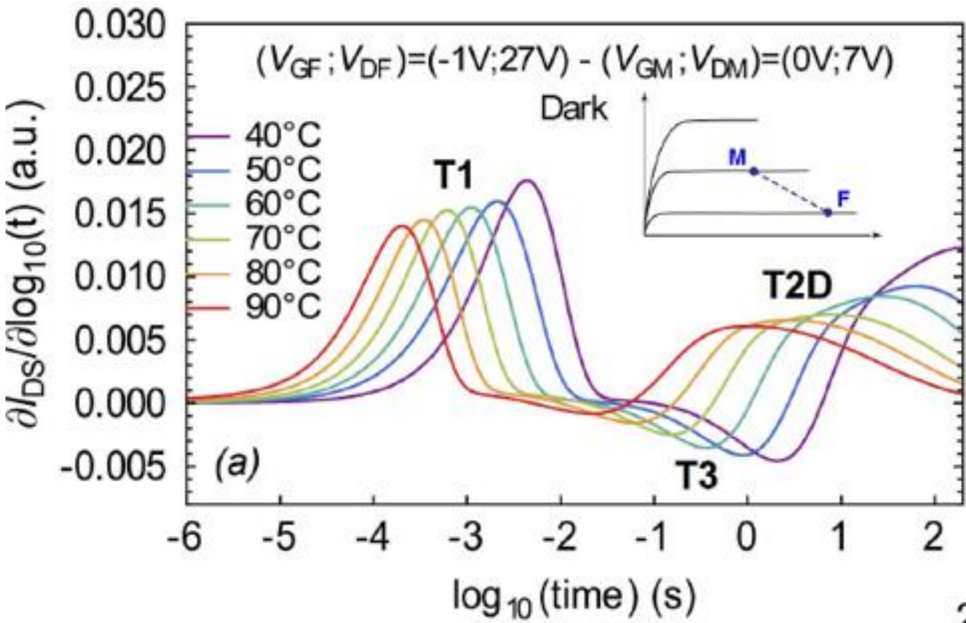
- Semi-on-state (high V_{DG} and relatively high I_{DS}) promote charge trapping into buffer region, likely caused by hot-electrons mechanisms.

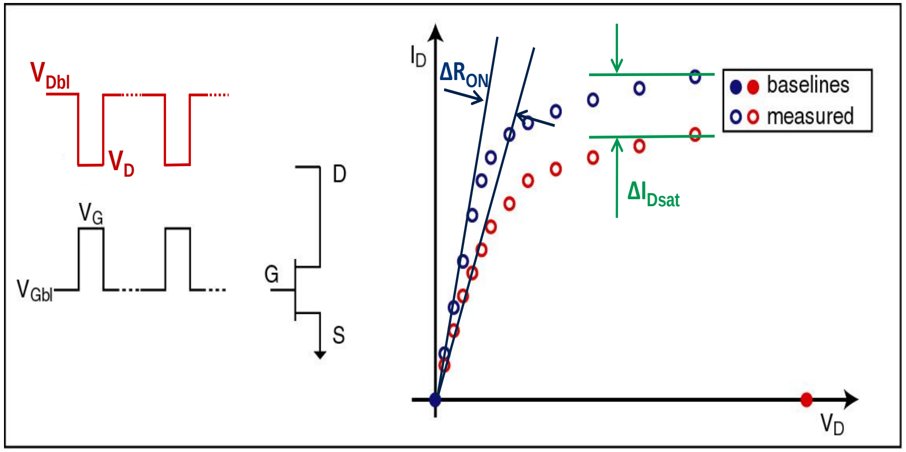


- Gate-reverse-bias promotes trapping below the gate region, where the free-carriers available for capturing are likely supplied by the gate-leakage current.



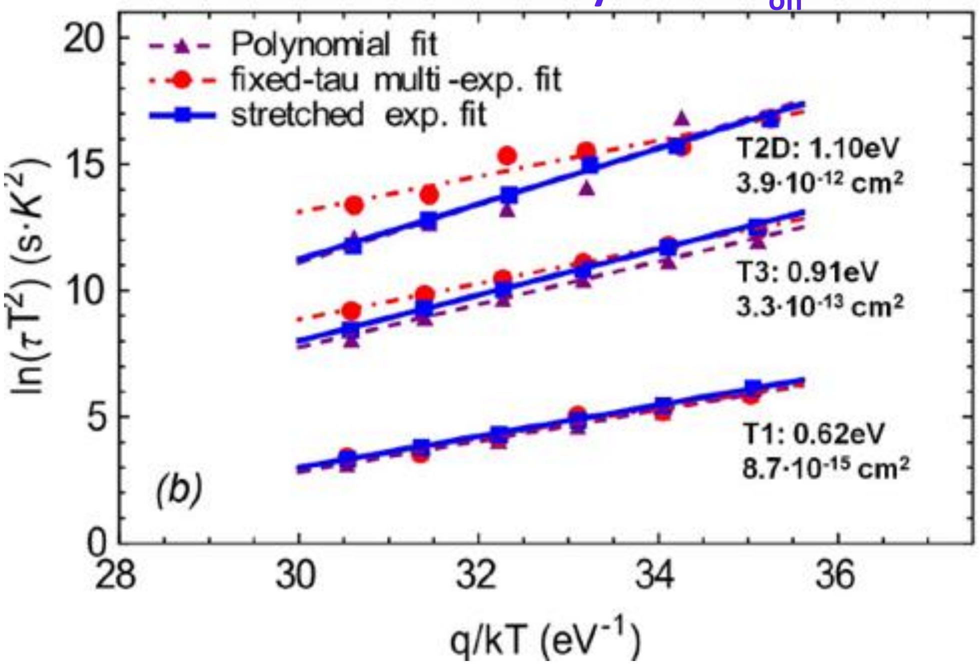
Characterizing traps: Drain Current Transient Technique





Deep levels responsible for trapping can be correlated with dynamic R_{on}

Thermal investigation can be used for the extrapolation of the Activation Energy and Cross Section of the deep levels responsible for trapping



D. Bisi et al, "DL characterization in GaN HEMTs", IEEE TED Oct. 2013

Database of DLs in GaN

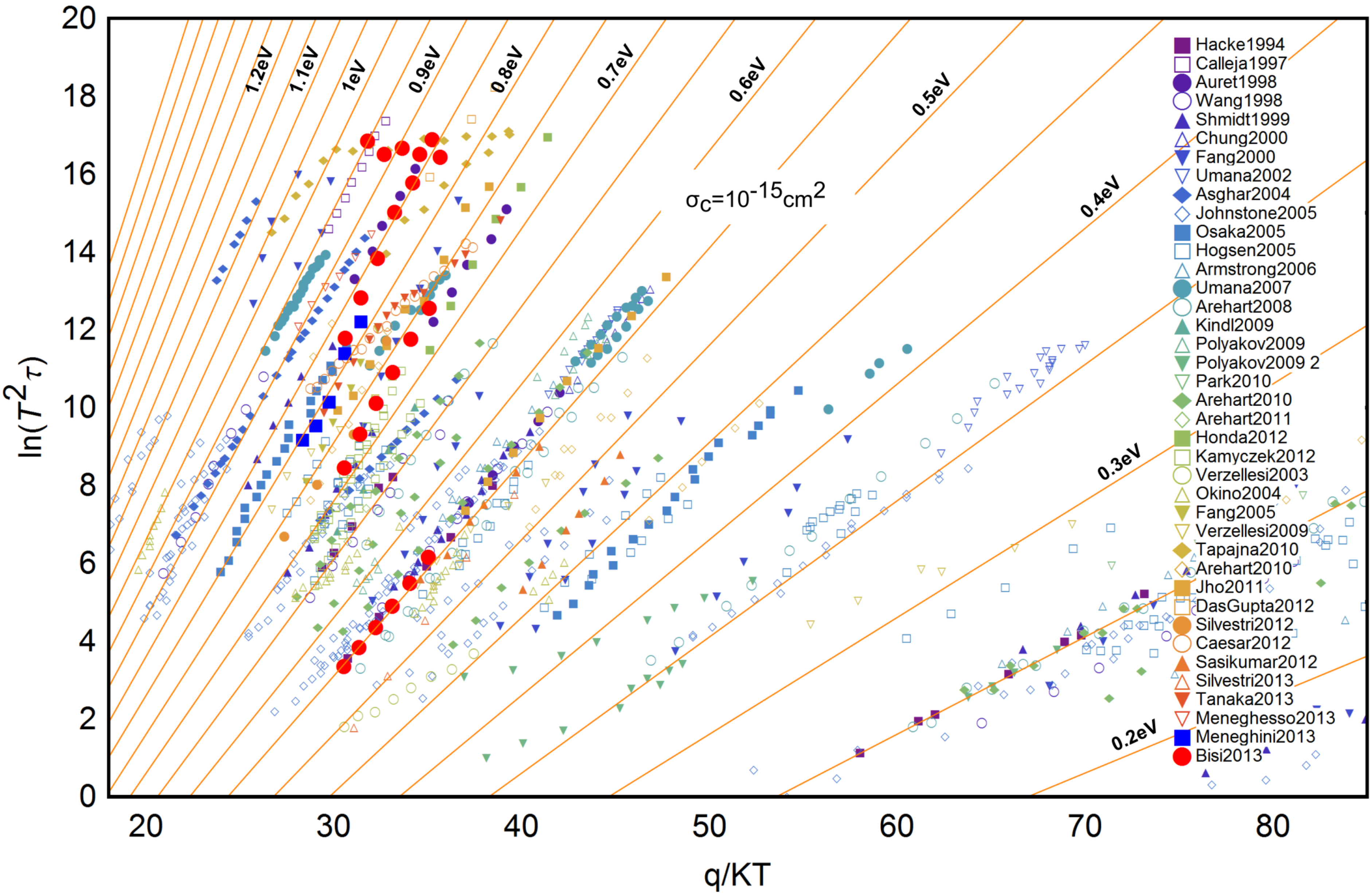
DL data from more than 80 papers on GaN material and devices

Reference papers	Analyzed samples	Deep level energy (eV)	Interpretations
Umana-Membreno [95], Soh [30], Park [83], Cho [36], Johnstone [89], Cho [37], Choi [62], Arehart [43], Cho [86], Chen [45]	Various GaN-based devices	EC - 0.09/0.27	Nitrogen vacancies
Chen [45]	n-GaN	EC - 0.12	Surface
Lee [77]	TMGa GaN	EC - 0.14	Carbon or hydrogen impurities
Polyakov [91]	p-GaN	EC - 0.15	Mg ionization
Gassoumi [72], Okino [39]	AlGaN/GaN HEMT	EC - 0.3/0.34	Possibly AlGaN surface
Heitz [71]	Fe doped GaN	EC - 0.34	Fe3+/2+
Umana-Membreno [95]	n-GaN	EC - 0.355	Mg impurities
Soh [30]	Si doped GaN	EC - 0.37/0.4	Si dopant
Caesar [18], Tapajna [17], Lee [77]	Various GaN-based devices	EC - 0.44/0.49	C/O/H impurities, possibly in nitrogen substitutional position
Cho [37], Cho [36], Umana-Membreno [75], Stuchlikova [46], Ashraf [61], Arehart [43], Chung [34], Chen [45], Fang [35]	Various GaN-based devices	EC - 0.5/0.62	Nitrogen antisites
Polyakov [51]	Fe doped GaN	EC - 0.5	Fe dopant
Cardwell [97]	AlGaN/GaN HEMT	EC - 0.57	influenced by Fe dopant
Chen [47]	n+p GaN diode	EC - 0.59	Si dopant
Hacke [32], Hierro [66]	Mg doped p-type GaN	EC - 0.6/0.62	Mg-H complex formation
Stuchlikova [46]	AlGaN/GaN HFET	EC - 0.6/0.64	VGa + Oxigen complex
Jhonstone [89]	n-type GaN	EC - 0.613	Nitrogen vacancies
Okino [39]	AlGaN/GaN MIS-HEMT	EC - 0.68	Surface
Silvestri [96]	Fe-doped AlGaN/GaN HEMT	EC – 0.72	Fe dopant
Asghar [68]	GaN pn diode	EC - 0.76	Nitrogen interstitials
Polyakov [51], Calleja [57]	Fe-doped or U.I.D. GaN	EV + 0.85, 0.94	Gallium vacancy
Fang [35]	n-type GaN on sapphire	EC - 0.89	Nitrogen interstitials
Asghar [68]	GaN pn diode	EC - 0.96	Gallium vacancy or N interstitials
…uret [33], Fang [49], Fang [50]	Various GaN-based devices	EC - 0.95/1.02	Threading dislocations
Stuchlikova [46]	AlGaN/GaN HFET	EC - 1.118	VGa + Oxigen complex
…], Arehart [44], Arehart [9], Hierro [66]	Various GaN-based devices	EC - 1.28/1.35	Carbon interstitial defect
Sasikumar [5]	AlGaN/GaN HEMT on SiC	EC - 2.3	Surface
Zhang [81]	c/m plane GaN	EC - 2.47/2.49	VGa + Hydrogen complex
Aggerstam [74]	Fe doped GaN	EV + 2.5/3	Fe dopant
Arehart [43], Arehart [44], Hierro [66]	Various GaN-based devices	EC - 2.6/2.64	VGa or VGa-H or VGa-2H
Arehart [56]	AlGaN (Al 30%)	EC - 3.11	Cation vacancy
Sasikumar [94], Arehart [43], Hierro [66]	Various GaN-based devices	EC - 3.2/3.22	Residual Mg acceptor
Zhang [81], Arehart [43], Sasikumar [5], Arehart [44], Henry [93]	Various GaN-based devices	EC - 3.24/3.31	CN substitutional
Sasikumar [5], Arehart [9]	AlGaN/GaN HEMT	EC - 3.7/3.76	Mg or C substitutional in AlGaN
Arehart [56]	AlGaN (Al 30%)	EC - 3.93	Mg impurities

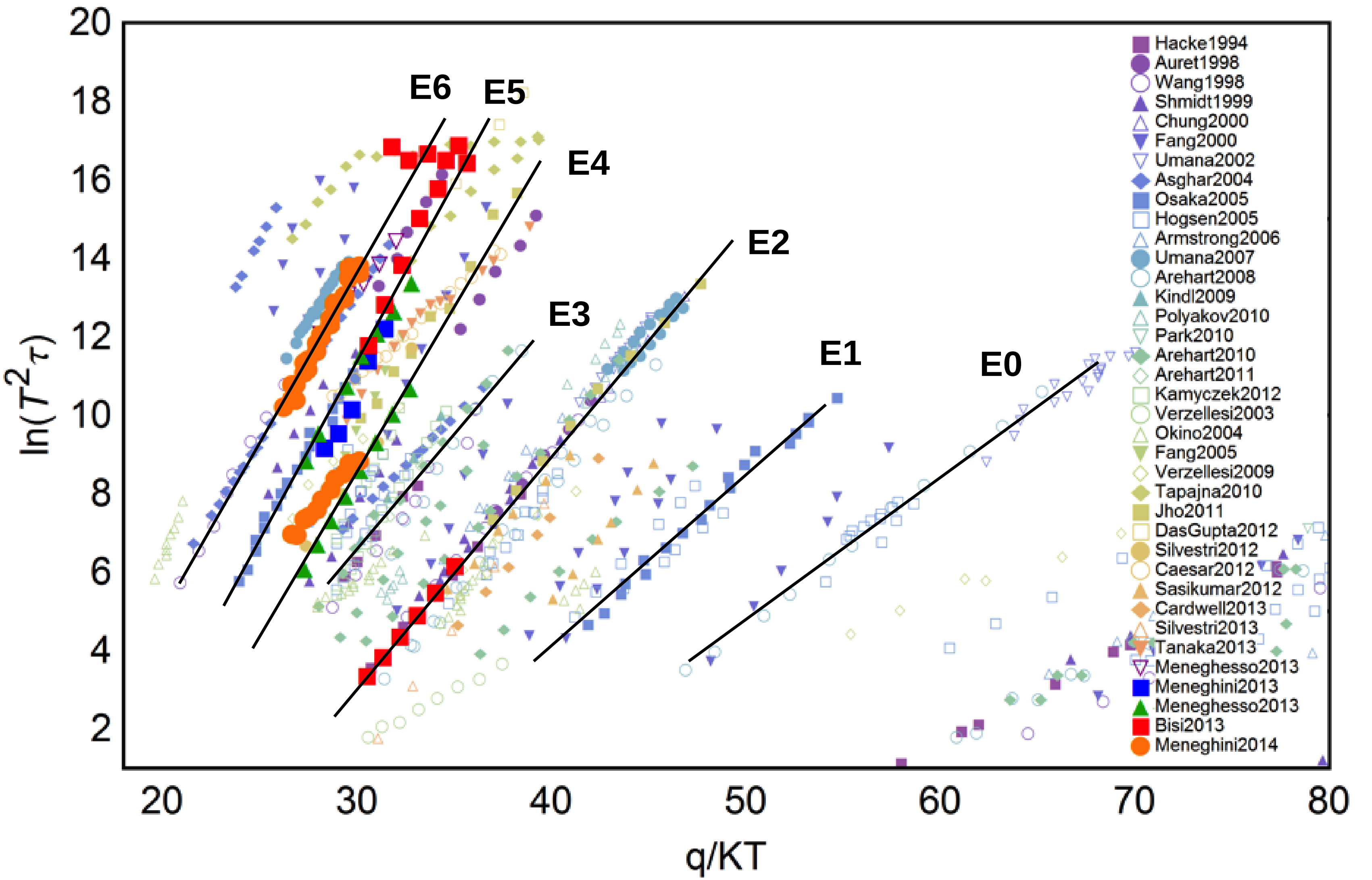
TABLE I: DATABASE OF THE DEEP LEVELS IN GAN- AND ALGAN-BASED LAYERS AND DEVICES

The whole database is described in D. Bisi et al, “DL characterization in GaN HEMTs”, IEEE TED, Oct. 2013

Database of deep levels in GaN



Database of deep levels in GaN



D. Bisi et al, "DL characterization in GaN HEMTs", IEEE TED Oct. 2013

Deep levels in GaN

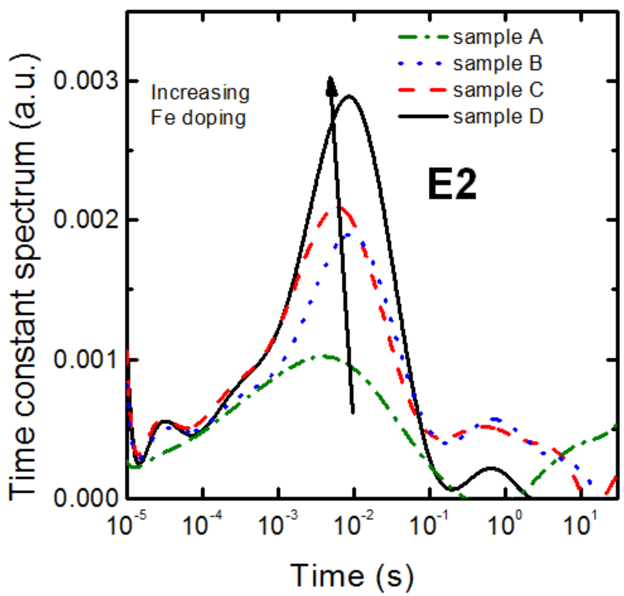
	E_A (E_C-)	Capture cross-section	***possible*** origins
E0	0.28 eV	1×10^{-17} cm^2	• Carbon in Gallium-substitutionals. • (open-core) dislocations. • Nitrogen-vacancies.
E1	0.37 eV	1×10^{-16} cm^2	
E2	0.63 eV	1×10^{-14} cm^2	• GaN point-defects (clustering along dislocations) Promoted by Iron-doping.
E3	0.62 eV	9×10^{-17} cm^2	• GaN point-defects.
E4	0.85 eV	4×10^{-14} cm^2	• Carbon interstitials. • (full-core) dislocations. • Gallium-antisites or interstitials. • AlGaN-related defects. • Radiation-induced defects.
E5	1.1 eV	10^{-12} cm^2	
E6	0.96 eV	5×10^{-15} cm^2	

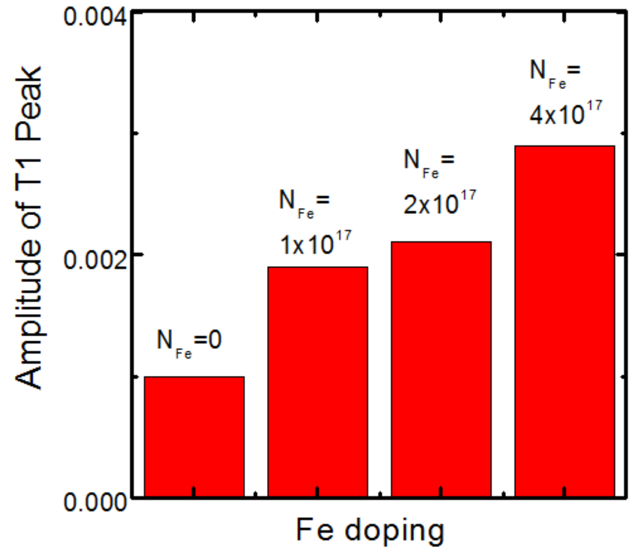
Key readings:

- D. Johnstone, *Proc. SPIE* 6473 (2007)
- C. G. Van de Walle *et al.* , *J. Appl. Phys.* 95 3851 (2004)
- A. F. Wright *et al*, *Appl. Phys. Lett.* 73 (1998)
- F. D. Auret *et al*, *Appl. Phys. Lett.* 73 , 3745 (1998)

Trapping processes related to compensating atoms→Iron

The Iron-doping promotes current collapse → deep-level **E_C-0.63eV / 10^{14}cm^2**, labelled as "E2".





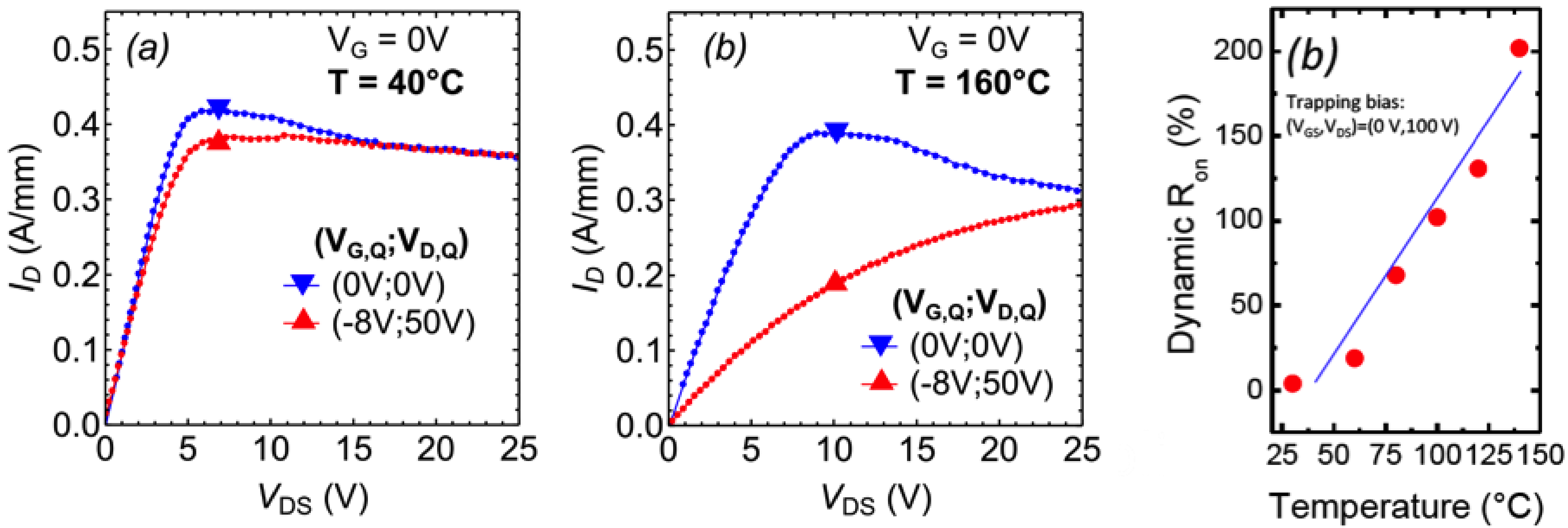
M. Meneghini *et al.*, "Role of buffer doping and pre-existing trap states in the current collapse and degradation of AlGaN/GaN HEMTs," *IEEE International Reliability Physics Symposium 2014*

E2 is actually not related to the Fe-level, but – more likely – to a defect whose concentration increases with Fe-doping

From the literature:

- E2 has been detected in GaN-bulk layers grown by means of different techniques, without the intentional introduction of foreign, dopant species.
- Iron in GaN should introduce the deep-acceptor-levels E_V+2.5eV and/or E_V+3eV

Trapping at high temperature

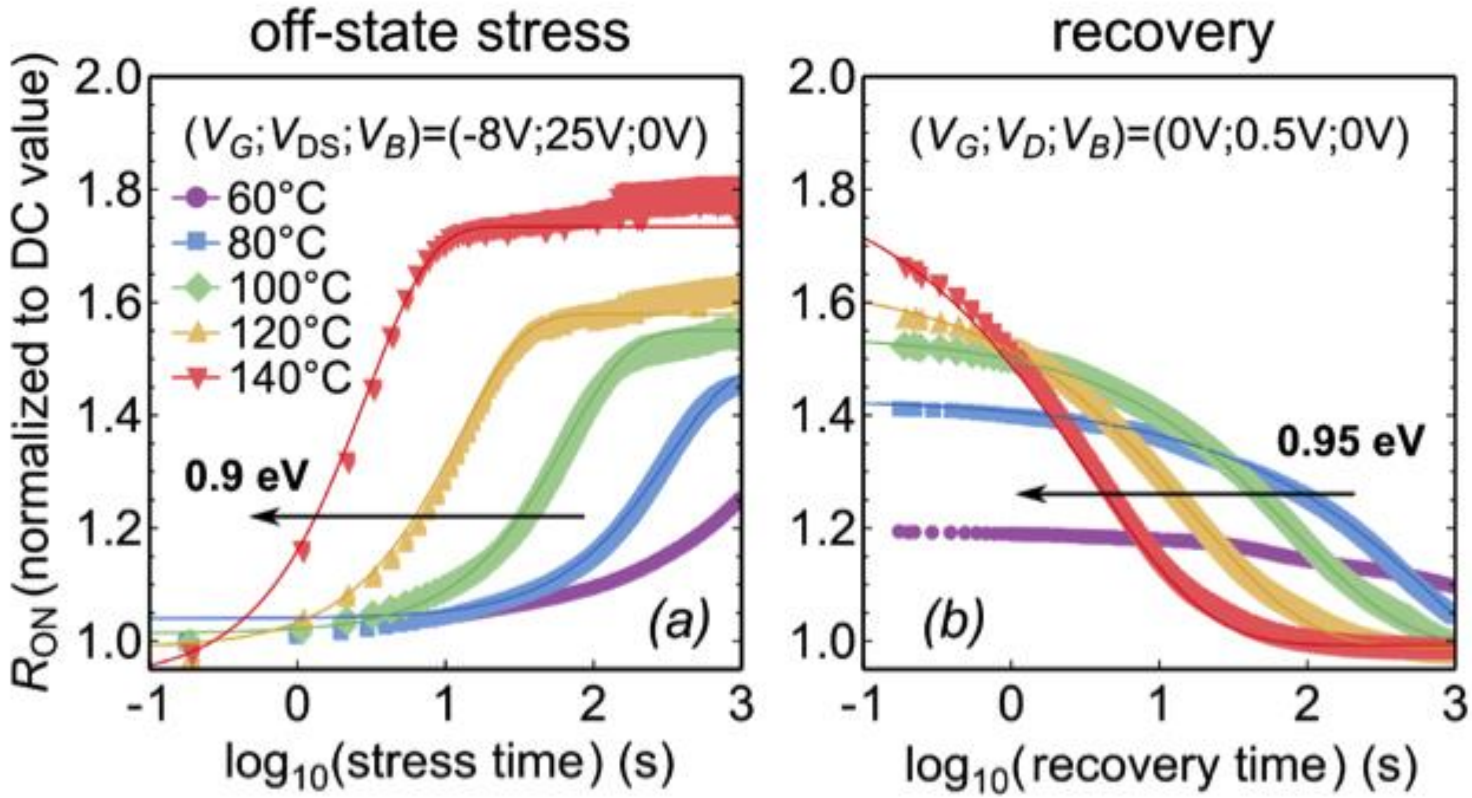


The trapping at different temperature has been evaluated:

- DUT has been tested at relatively low temperature and no significant dynamic Ron was observed;
- Dynamic Ron increases with temperature (25-140 ° C)
- This effects seems not consistent since it is known that the trapping in semiconductors at high T is decreased.

ON Semiconductor

I-DLTS at High Temperature



- **Trapping phenomena require long time (up to hrs);**
- **Trapping time lowers at high Temperature**
  - **Dynamic Ron (and trapping rate) increase with T**
- **Detrapping also require long time**
- **Detrapping is thermally-activated with Ea=0.95 eV**

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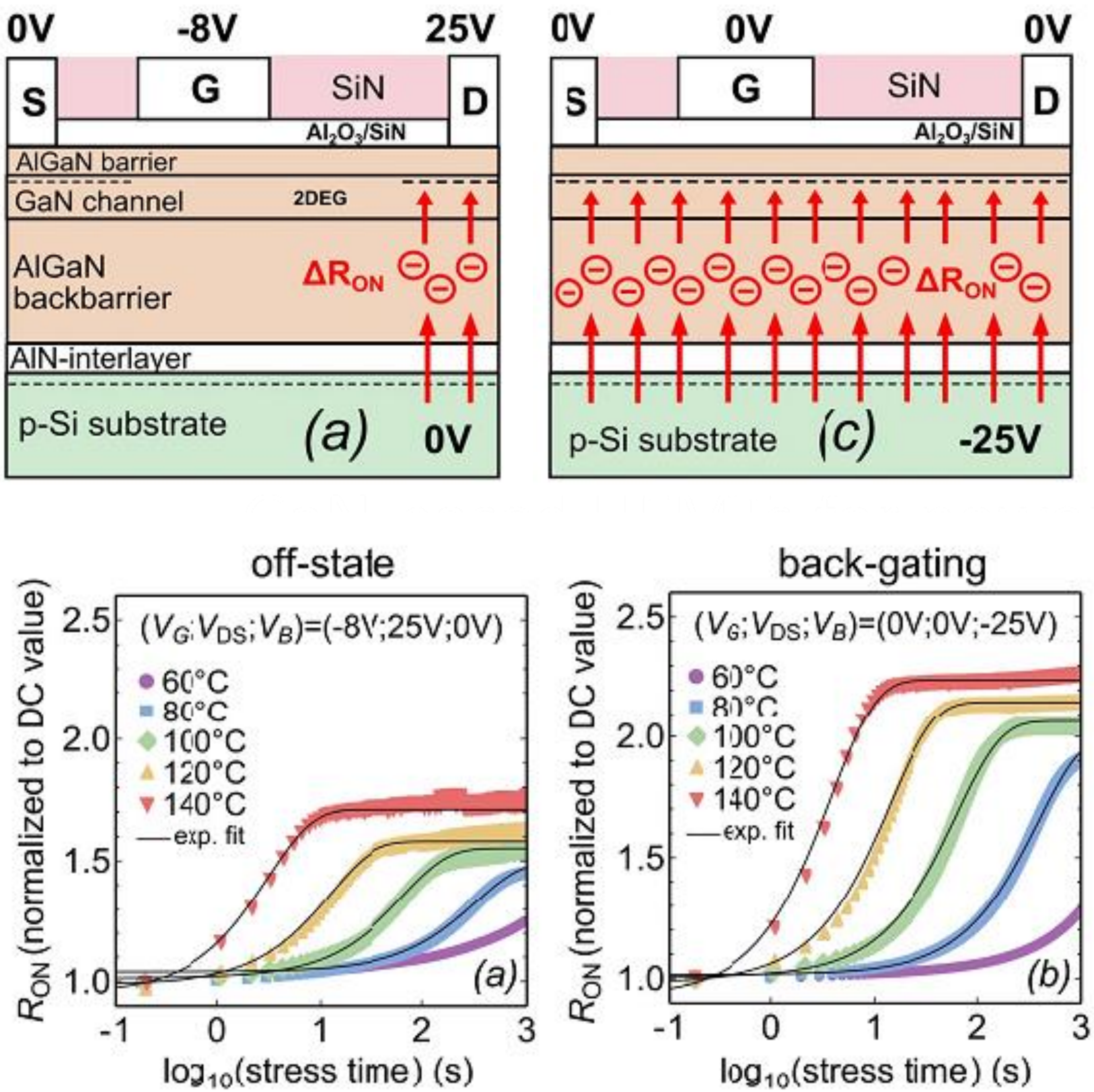
Back-side pulsing



- Trapping in power GaN devices is not trivial;
- It can be explained with a barrier for trapping;
- Traps are located in the buffer

Back-gate helped to localize traps

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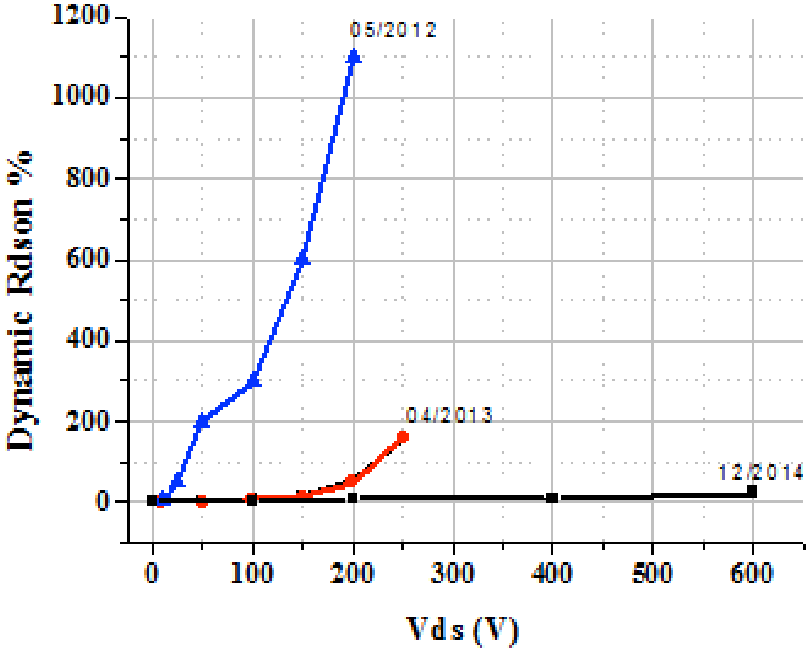
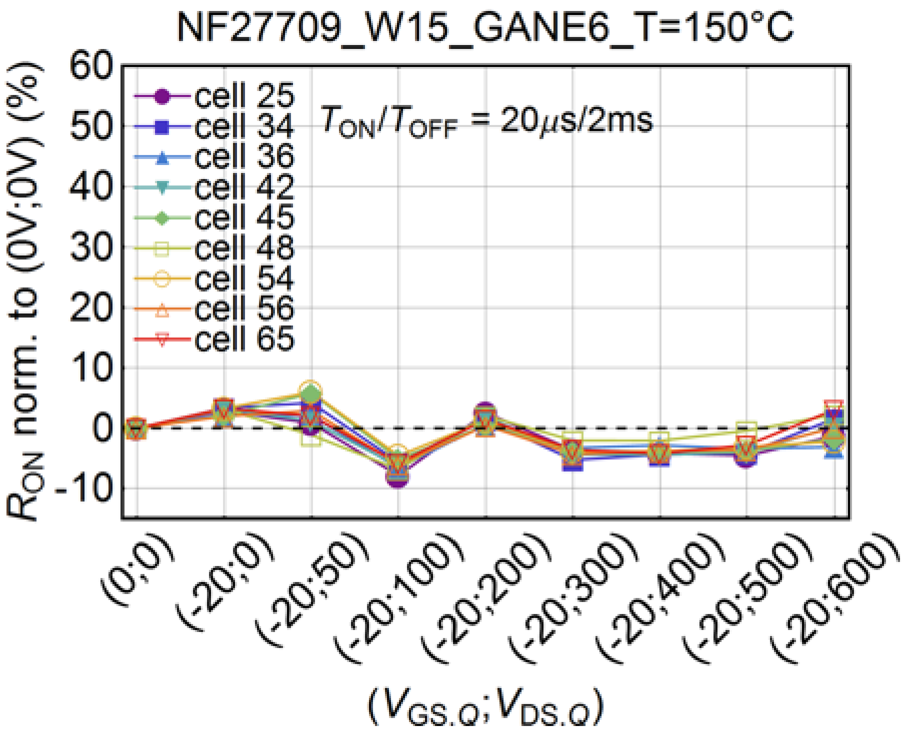
Dynamic R_{DSon} evolution

2012, 2014



2016



Large progress has been made in the last year by means of process and material development.

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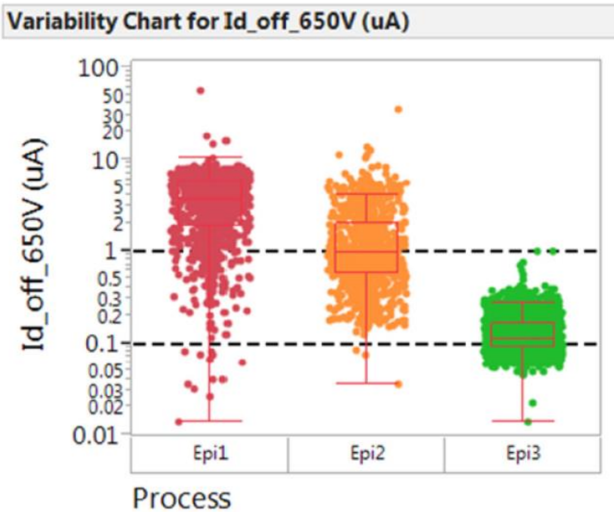
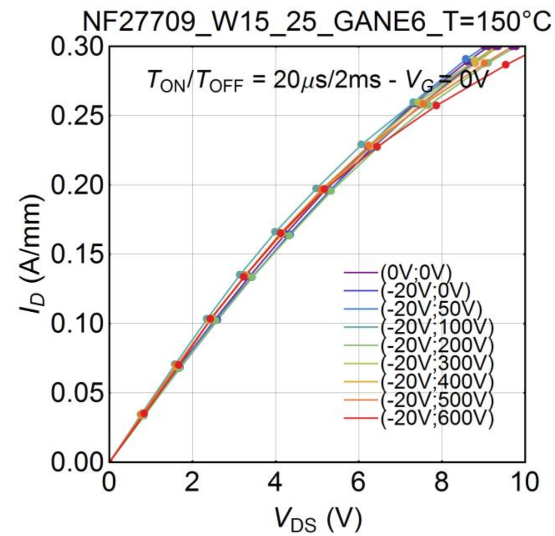
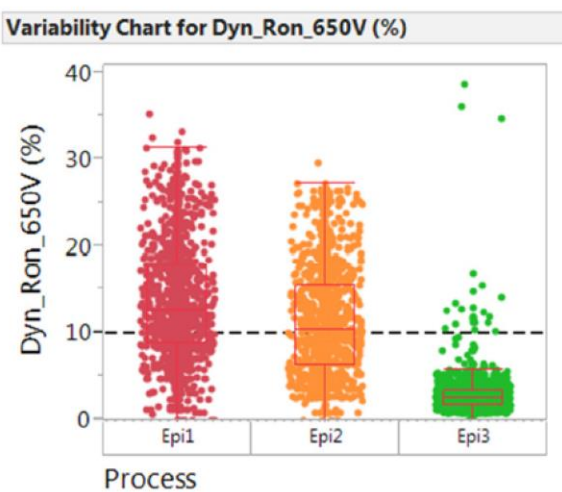
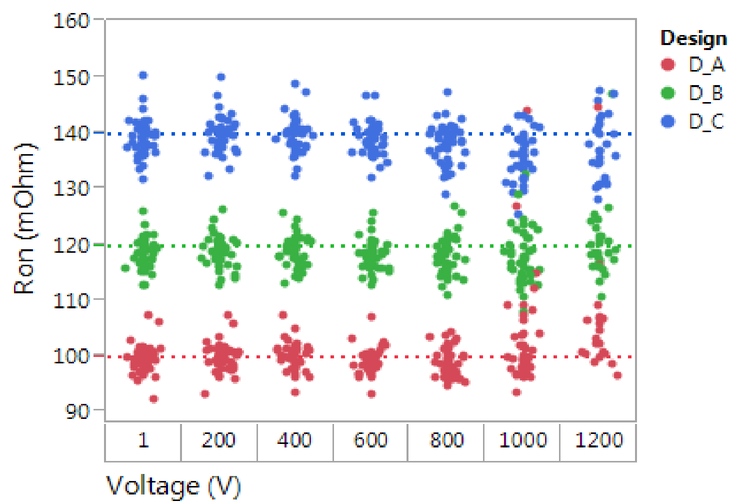
Fully dyn Ron free devices



Epitaxy optimization allow the processing of dynamic R_{DSon} free devices up to 1.2 kV







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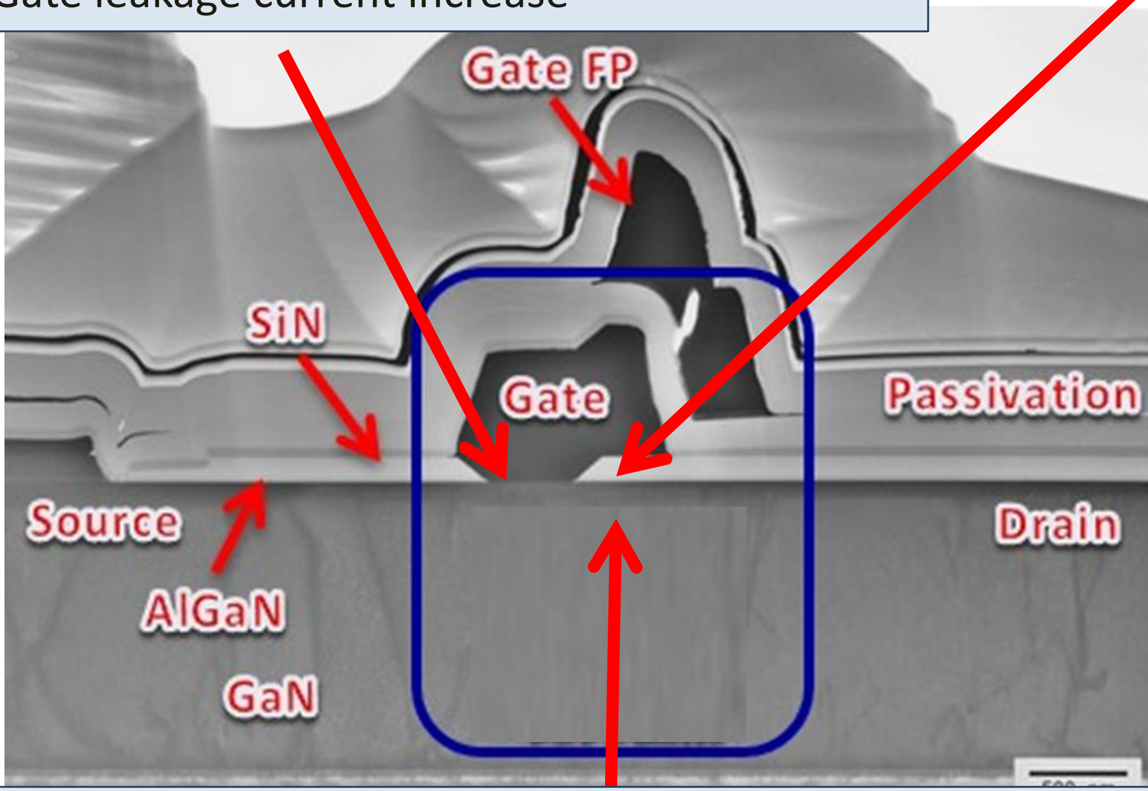
Outline

- Introduction on GaN-based HEMTs
- Breakdown mechanisms at high drain bias
- Parasitic (trapping) mechanisms → recoverable degradation
  - Current/Ron collapse
  - Methods for analyzing defects in GaN-HEMTs
  - A database for deep levels in GaN
- Permanent degradation mechanisms
  - Degradation in off-state → Schottky-gate
  - Degradation under FW bias → p-GaN gate
  - Degradation under FW bias → MIS gate
- Conclusions

Degradation mechanisms for GaN-HEMTs

Schottky contact degradation (high T, on-state)
4) Thermally activated interdiffusion
Gate leakage current increase

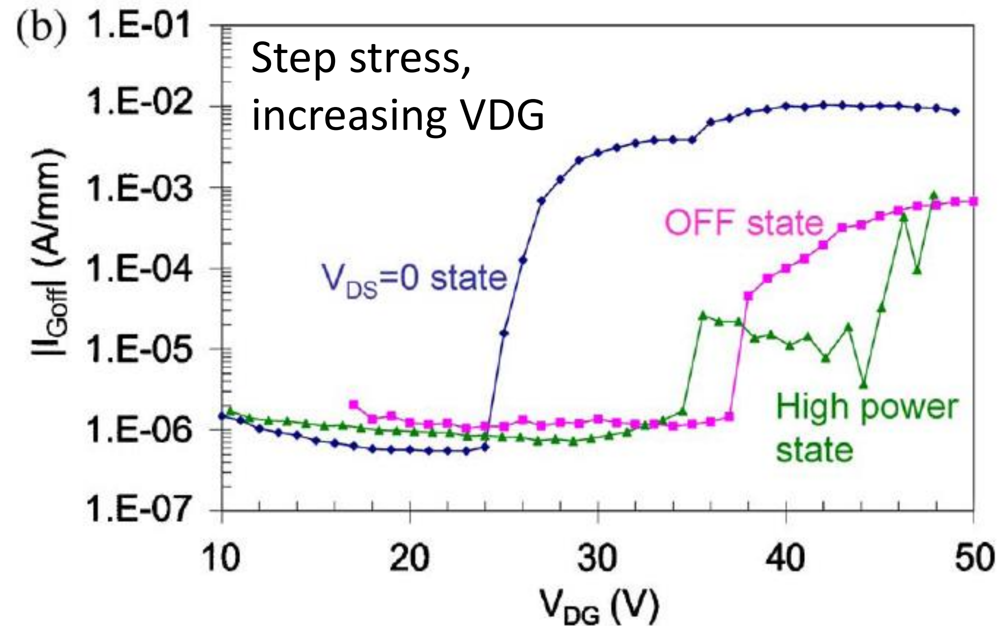
Reverse bias or off-state degradation
1.1) Converse piezoelectric effect
Deep levels generation
1.2) Time dependent breakdown (point defects percolation)
1.3) Electrochemical surface degradation (GaN oxidation)
GaO dissolution, oxygen indiffusion
1.4) Groove formation, surface pitting
Increase of gate leakage current, decrease of drain current, increased current collapse



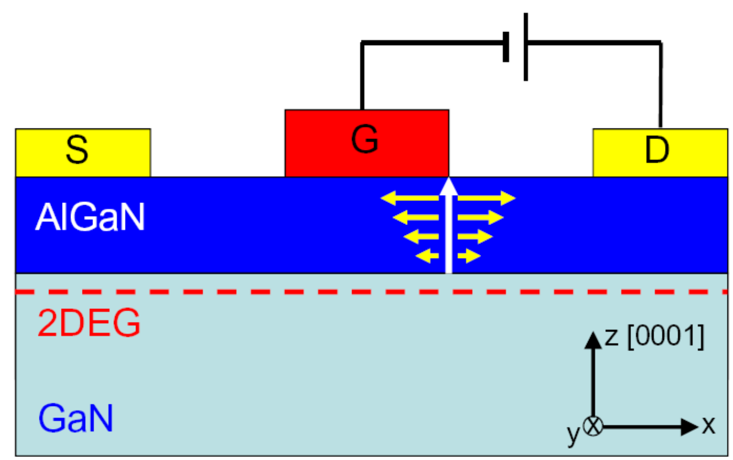
On-state and semi-on state degradation
2) VTH drift: due to impurities or trapping; 3) Hot electron effects: Charge trapping in the SiN, dehydrogenation of point defects and deep levels activation; 1.4) Groove formation, surface pitting, defects formation : electrochemical GaN dissolution? converse piezoelectric effect?
Transconductance degradation; drain current decrease; threshold voltage shifts

HEMTs may degrade when submitted to reverse-bias stress

Joh et al. suggested that – in a step-stress experiment - there is a "critical (gate-drain) voltage" beyond which the device starts degrading, showing a permanent increase in gate leakage current



Degradation was ascribed to converse piezoelectric effect → the mechanical strain produced by this electric field adds on top of the tensile strain due to lattice mismatch (increase in the elastic energy in the AlGaN). If this elastic energy exceeds a critical value, crystallographic defects are formed



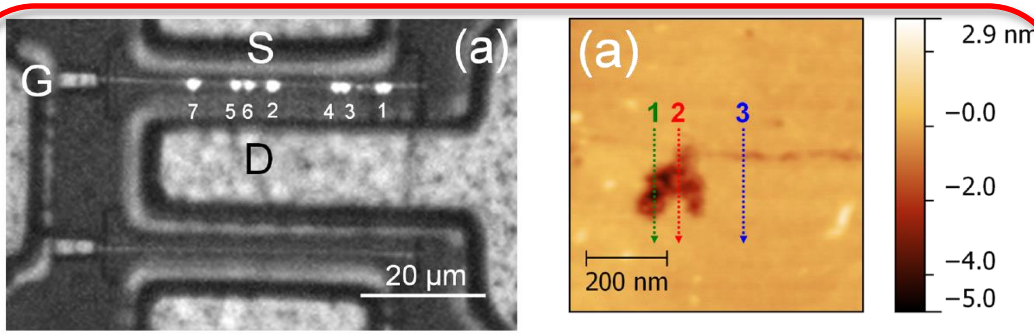
Joh et al., EDL 29, 287, 2008

EL as a tool for analyzing the degradation process

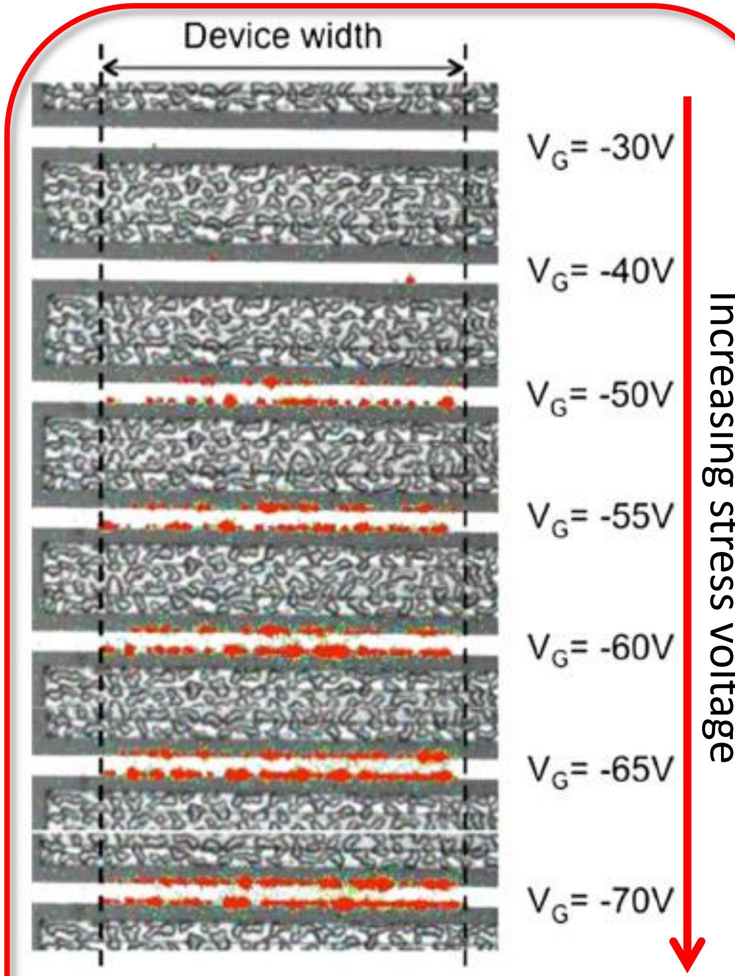
Stress induces the generation of leaky paths under the gate → Generation of lattice defects

Leakage paths can be identified by electroluminescence microscopy →

A direct relation between EL hot spots, surface pits, and gate current leakage was demonstrated

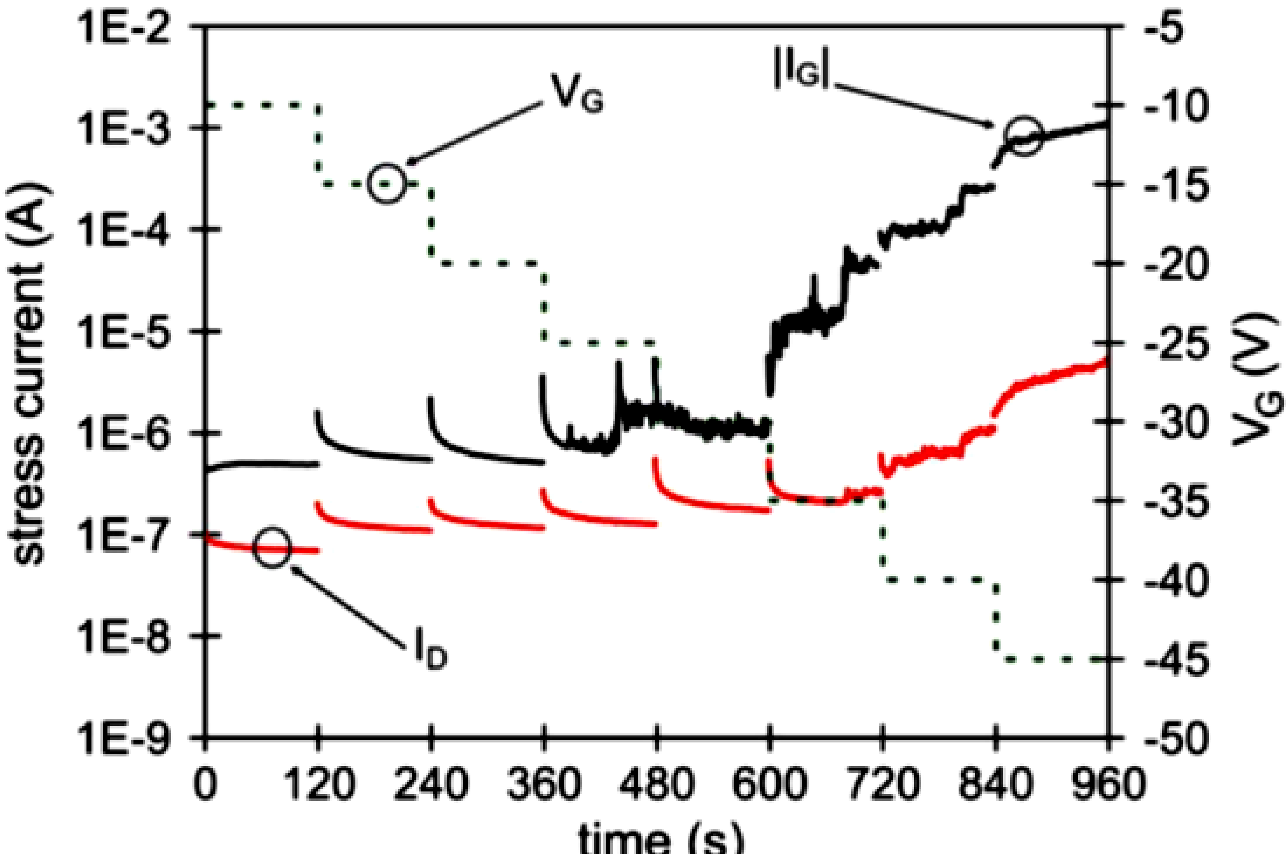


Montes Bajo et al., Appl. Phys. Lett. 101, 033508 (2012)



EL investigation:
Zanoni et al., EDL 30, 429, 2009

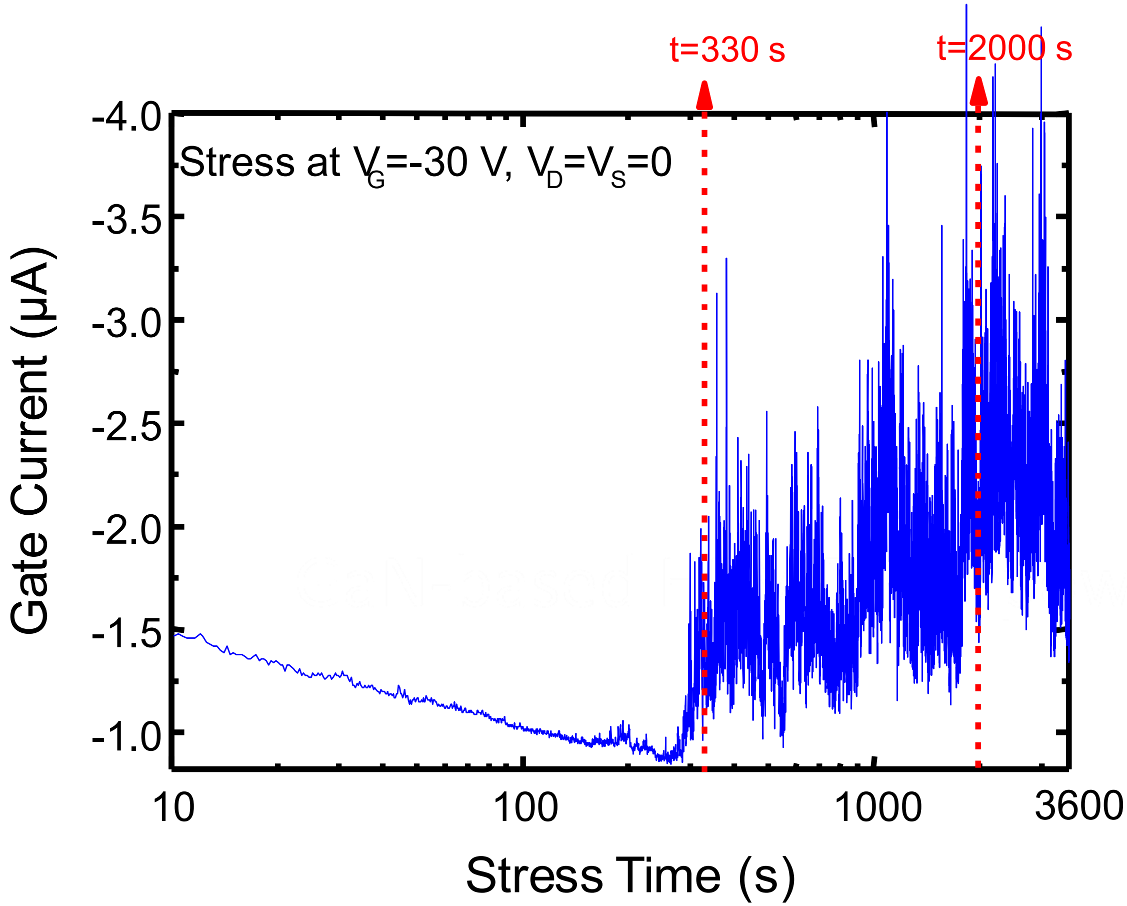
Gate-edge degradation and sudden increase of Ig



Reverse-bias step-stress experiment on a 200 nm AlN/GaN-on-Silicon double-heterostructure HEMT for Ka-band applications. V_{DS} = 0 V, 5 V /step, 120 s duration.

G. Meneghesso *et al.*, "First reliability demonstration of sub-200-nm AlN/GaN-on-silicon double-heterostructure HEMTs for Ka-band applications," *IEEE Trans. Device Mater. Reliab.*, vol. 13, no. 4, pp. 480–488, 2013.

Constant-Voltage Stress Tests: time dependent failure



Three phases:
1. gate leakage current is reduced, as a consequence of electron trapping

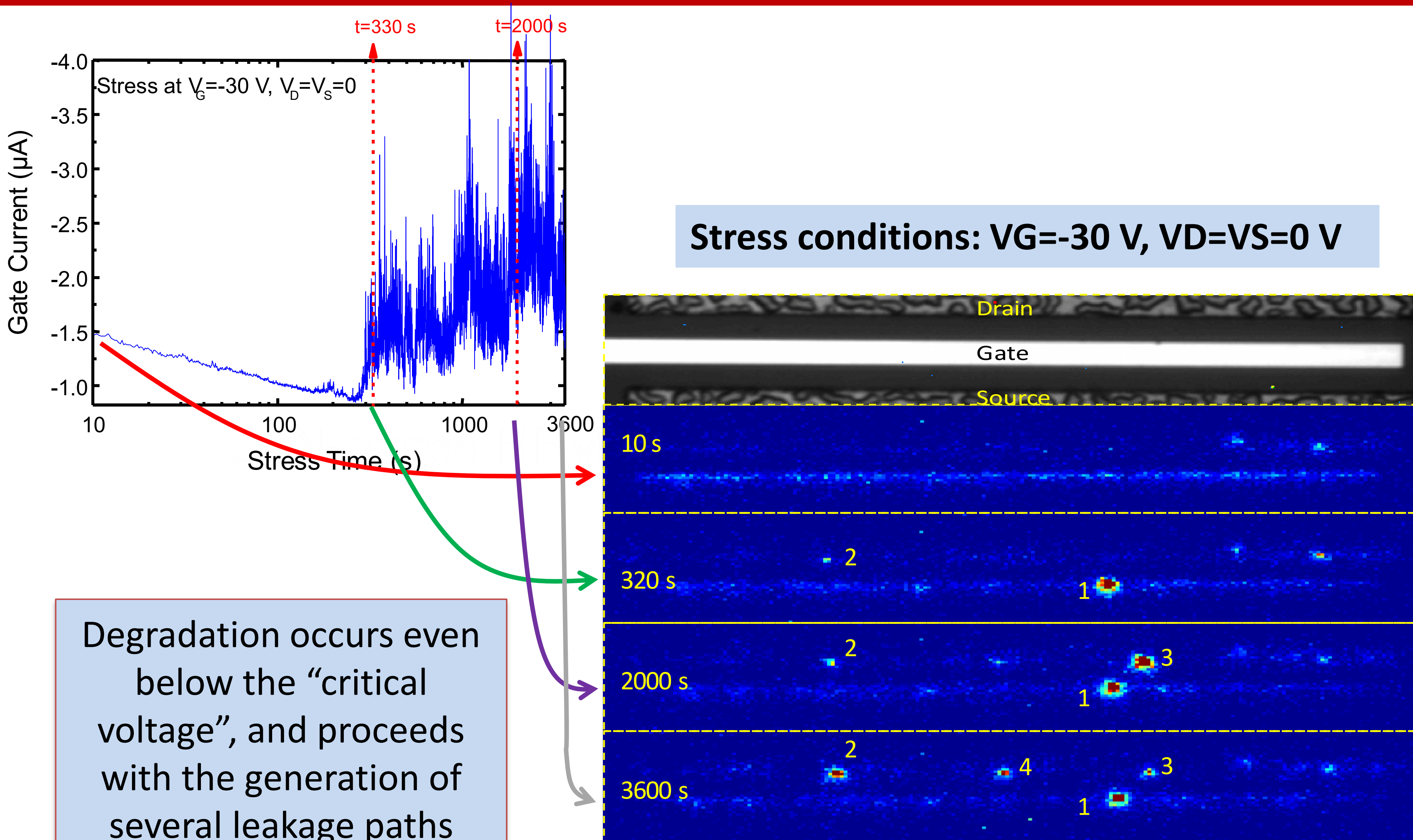
2. leakage current becomes «noisy»

3. leakage current «jumps», remarkably increasing before «hard breakdown»

STRESS CARRIED OUT AT 30 V

M. Meneghini et al., Appl. Phys. Lett. 100, 033505 (2012)

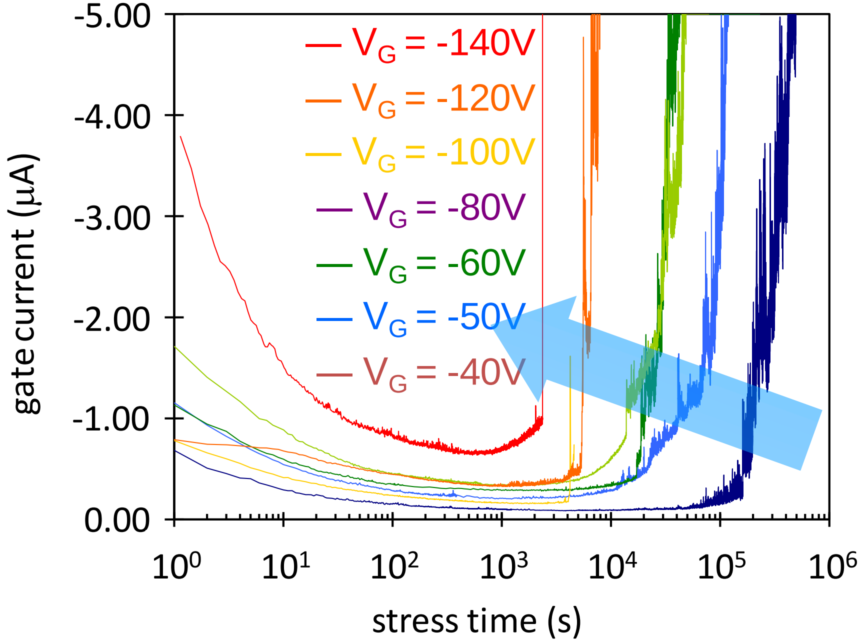
Electroluminescence signal during stress



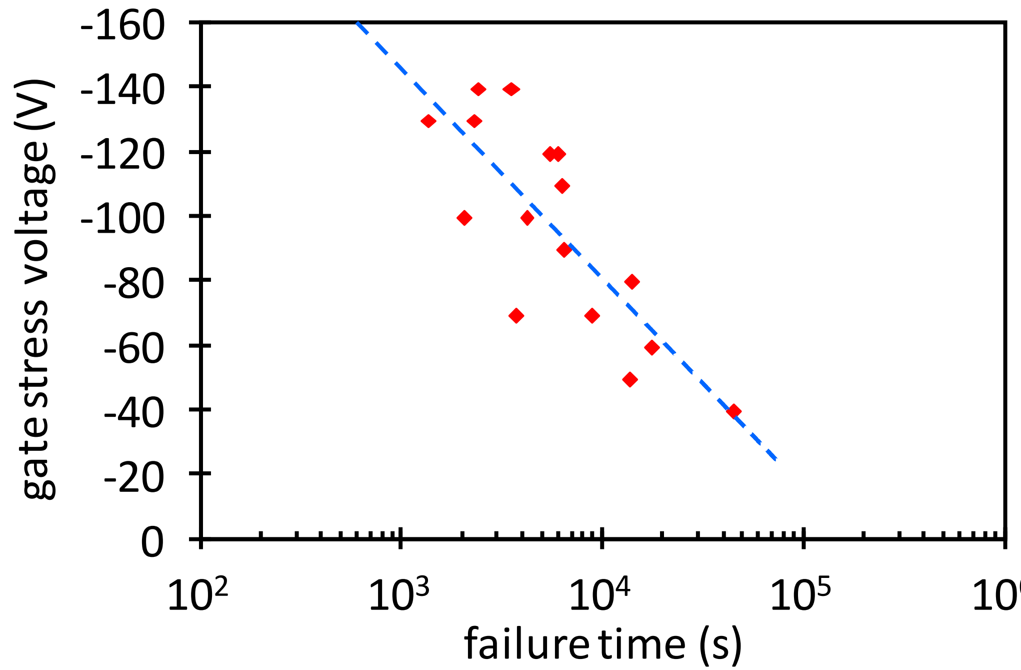
Stress conditions: VG=-30 V, VD=VS=0 V

Degradation occurs even below the "critical voltage", and proceeds with the generation of several leakage paths

Dependence of time to breakdown on stress voltage



•Stress tests carried out at different (negative) voltage levels show that degradation kinetics are strongly accelerated at high electric fields



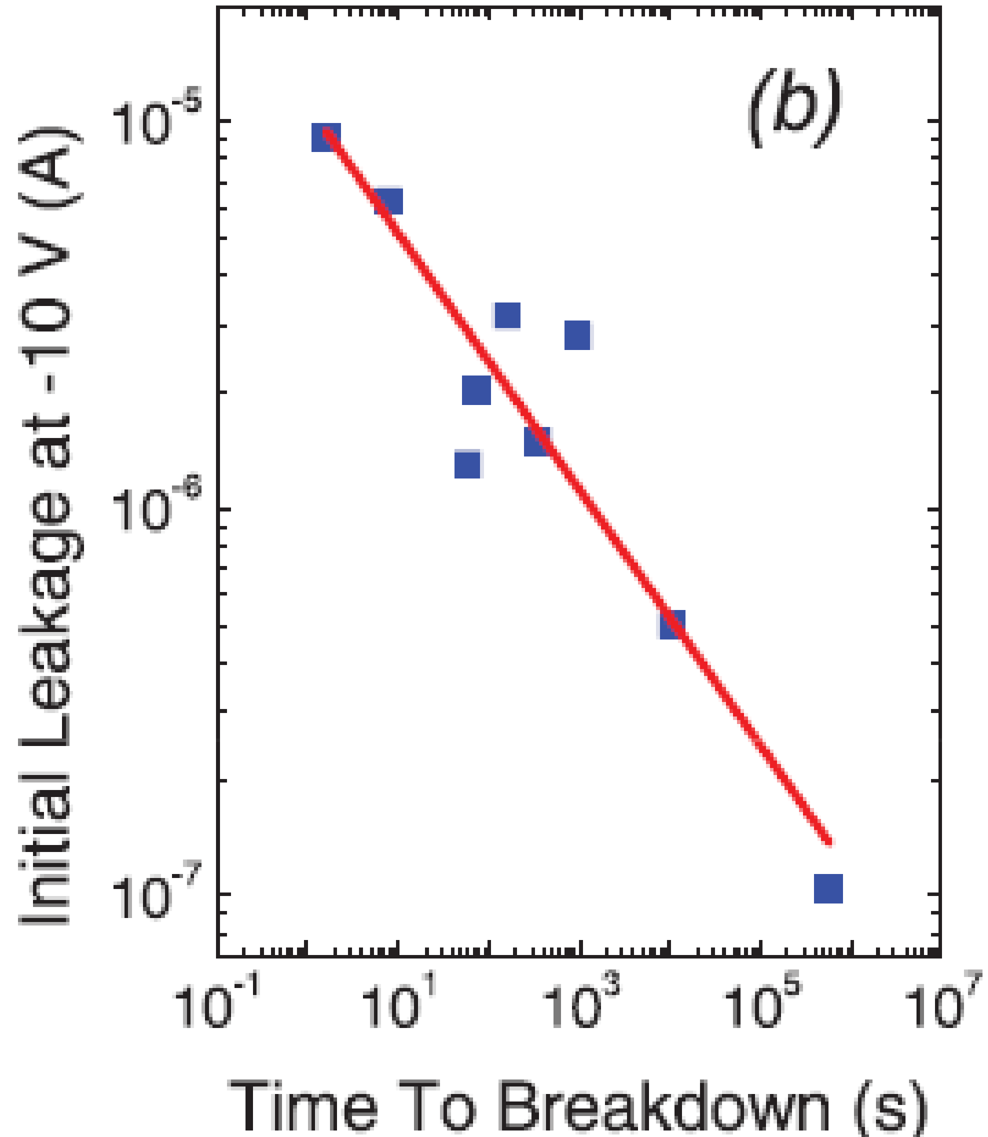
•Time to Breakdown strongly depends on the applied electric field (degradation even below the "critical voltage")

M. Meneghini et al., Appl. Phys. Lett. 100, 033505 (2012)

Dependence of time to breakdown on initial leakage

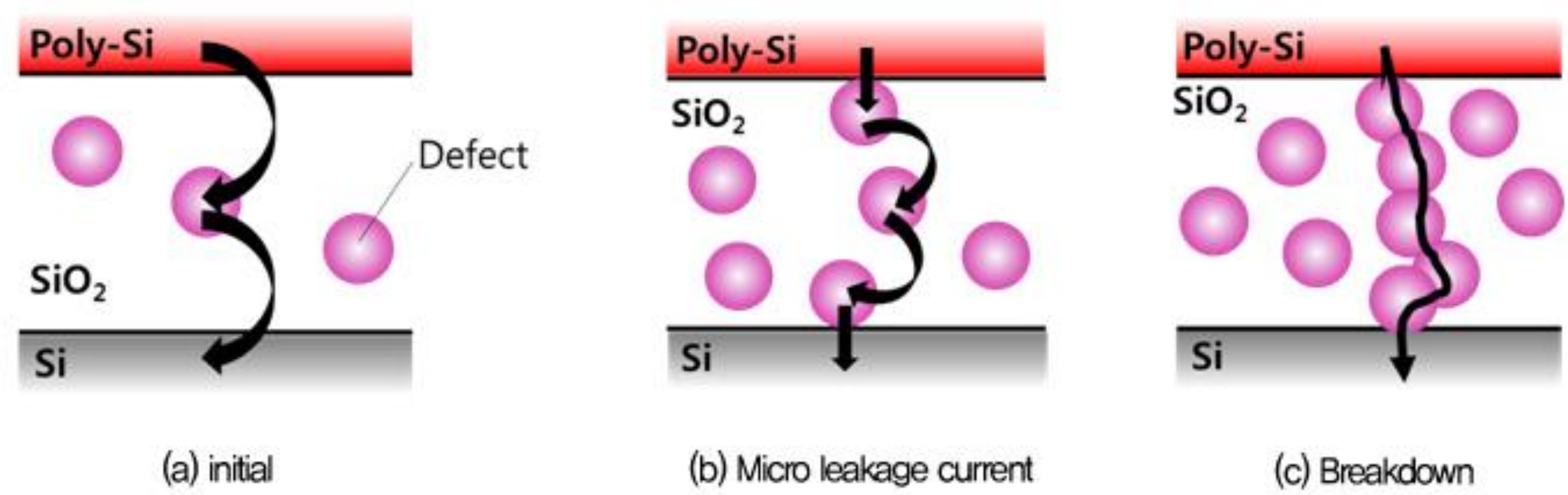
•Time to Breakdown measured at V_G = -30 V $V_D = V_S$ = 0 V

M. Meneghini et al., Appl. Phys. Lett. 100, 033505 (2012)



Percolation theory:

Electric field + leakage induce random defects within the blocking layer (insulator). When a conductive chain of defects is formed (percolation path) lekage current sharply increases.

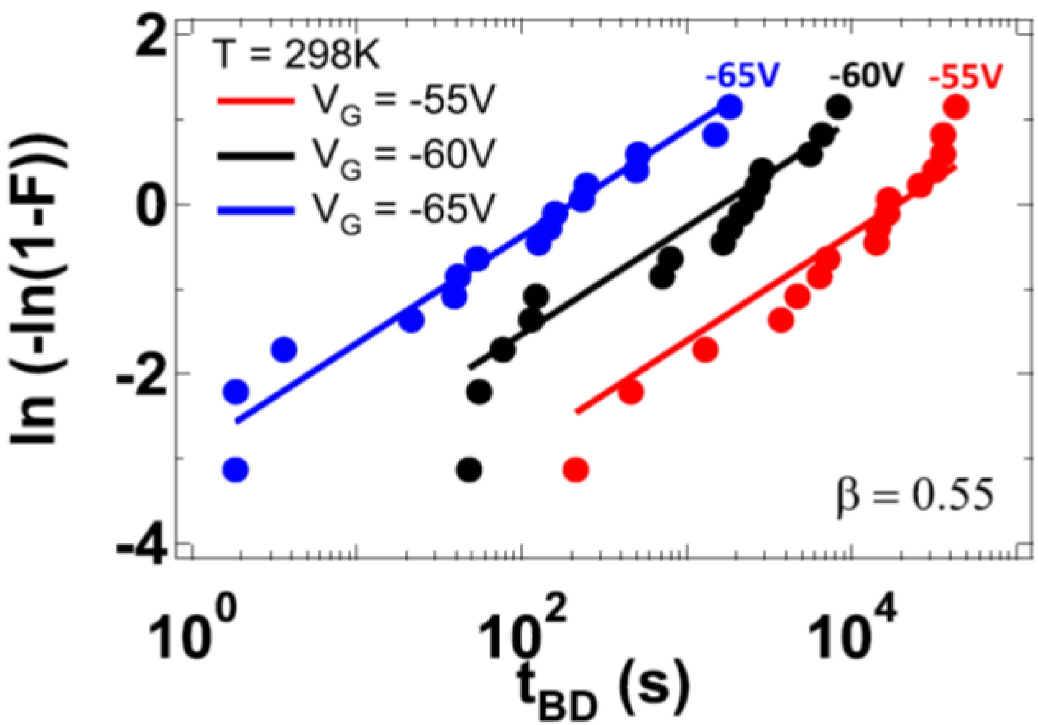


Weibull distribution of time to breakdown

cumulative probability function:

$$\int_{-\infty}^{t} f(y)dy = F(t) = 1 - exp\left[-\left(\frac{t-\gamma}{\eta}\right)^{\beta}\right]$$

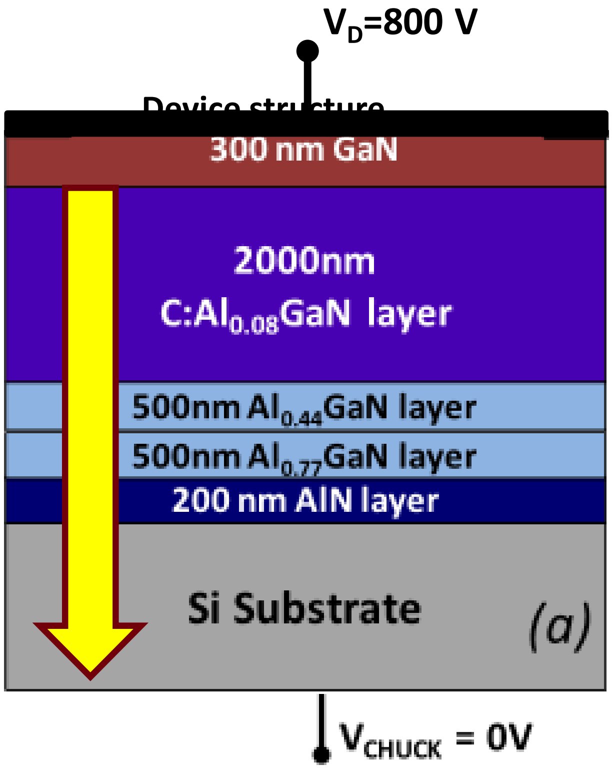
$$ln[-ln(1-F(t))] = \beta ln(t) - \beta ln(\eta)$$



The parameter β is related to the number of defects forming the percolation path. $\beta = m\,N$ where m is the trap generation rate and N is the number of defects needed to form the defects needed to form the percolation path.

The low β value (0.55) possibly depends on the reduced number of defects which is sufficient to create a conductive percolation path within the AlGaN.

Intrinsic failure: GaN TDB, the ultimate limit?

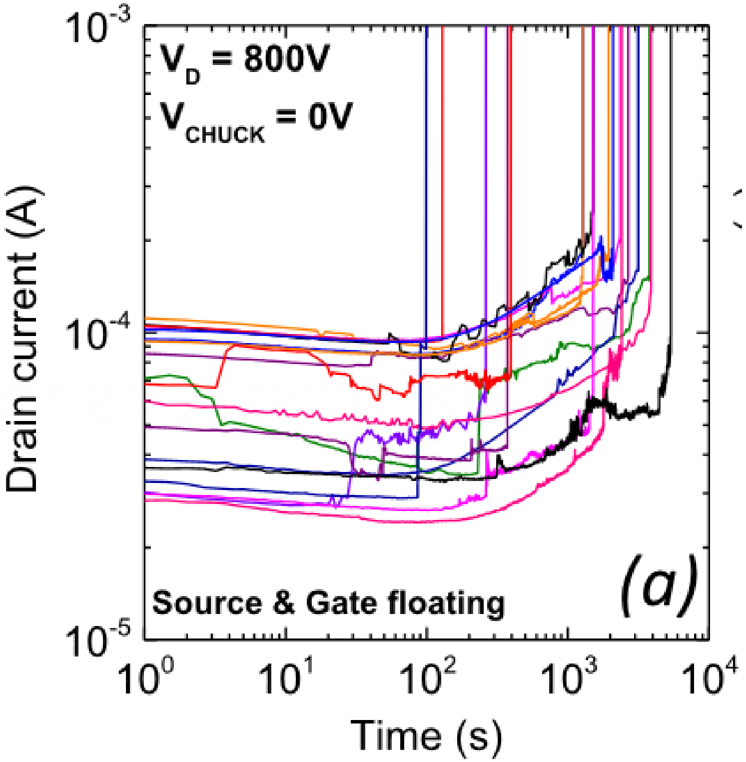


$E_{C,GaN}$=3.3 MV/cm → what happens during a long-term stress close to E_C?

2-terminal stress experiment (drain-to-substrate) induces a time-dependent failure

Semi-insulating GaN behaving as a dielectric

Constant voltage stress



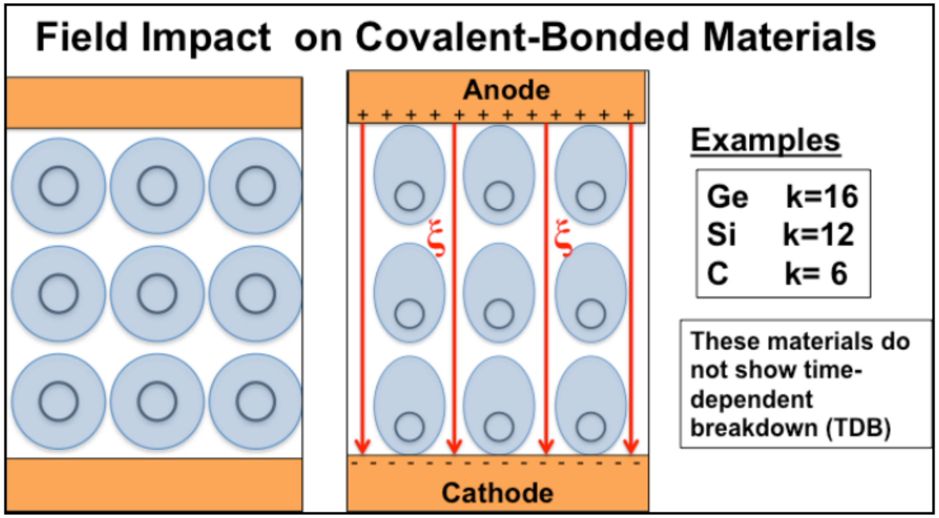
Here dielectrics are not involved, GaN itself is showing TBD

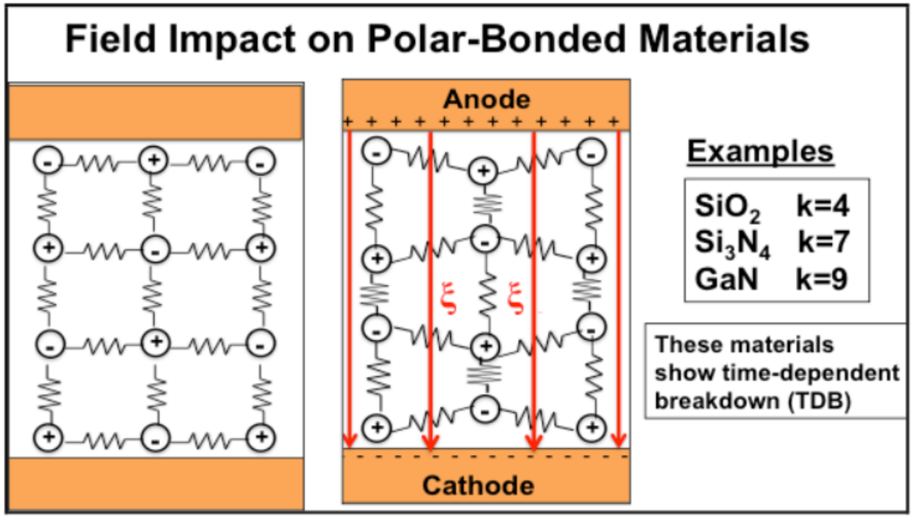
IEEE TED 64 (9) 3616 (2017) IEEE TED 65 (7) 2765 (2018)

Intrinsic failure: GaN TDB, the ultimate limit?

Why does GaN show TBD (and silicon does not?) →

Joe Mc Pherson, IEEE-IRPS 2018



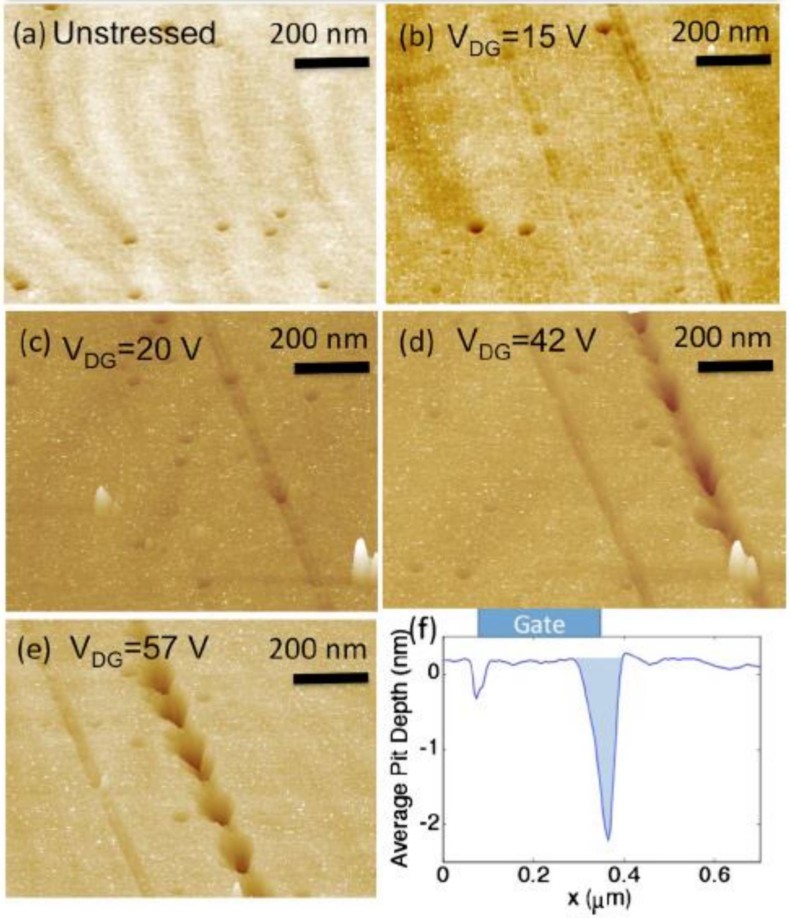


Covalent-bonded materials → polarization induces **shift in the electron cloud about each atom's nucleus** (rather easy, time constant in the order of femto-seconds, no lattice distortion)

Polar-bonded materials → field induces a strong **increase in strain energy**, with time constant in the order of pico-seconds → Change in Gibbs potential, lattice becomes less stable (TBD is a stress-relief mechanism)

AFM analysis → Generation of grooves/pits under the gate

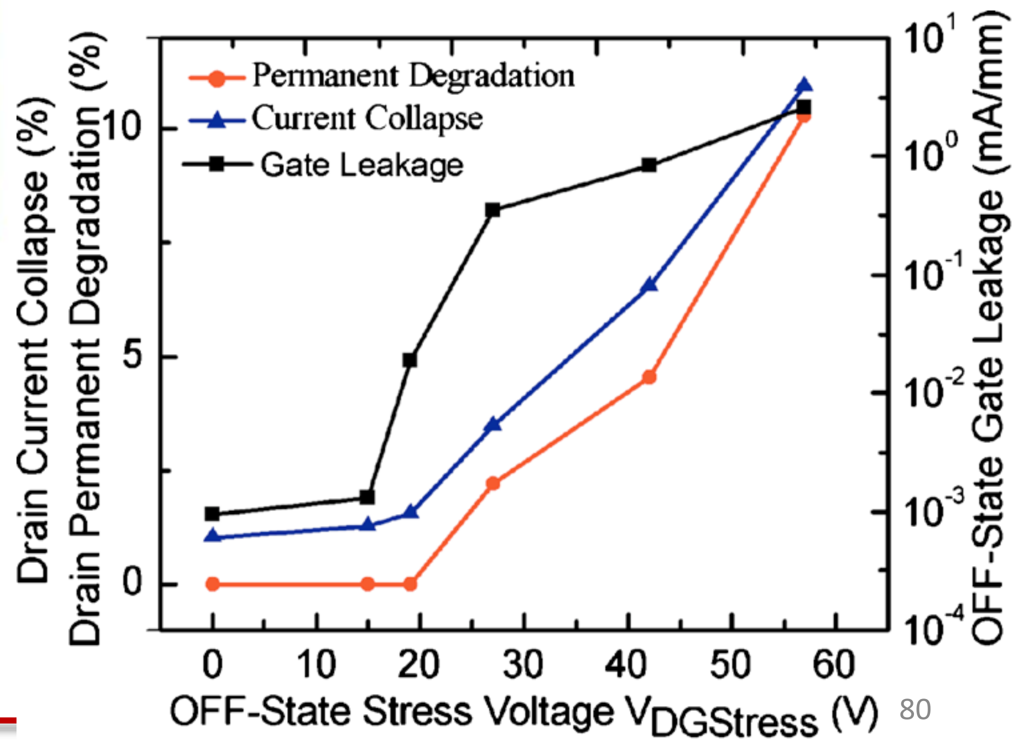
Stress at 150 °C,up to V_{DG}=50 V



Three-steps process:

1. **a groove forms in the GaN cap layer due to field-induced oxidation or electrochemical etching**
2. pit formation and growth
3. subsequent crack formation

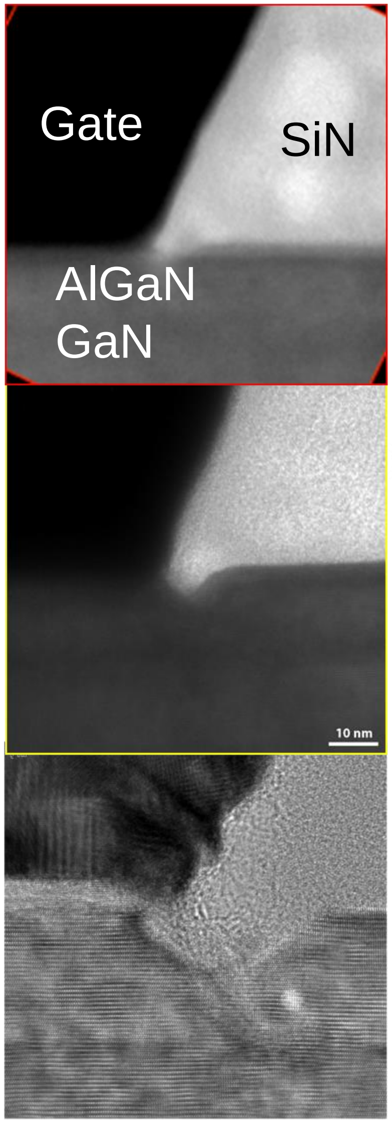
Mechanism thermally enhanced,
but requiring an electric field to occur



Makaram et al. (MIT), Appl. Phys. Lett. 96, 233509 (2010)

Structural Degradation in GaN HEMTs

Cross-section



1. Below and around V_{crit}:

Fast groove formation in GaN cap

2. Beyond V_{crit}:

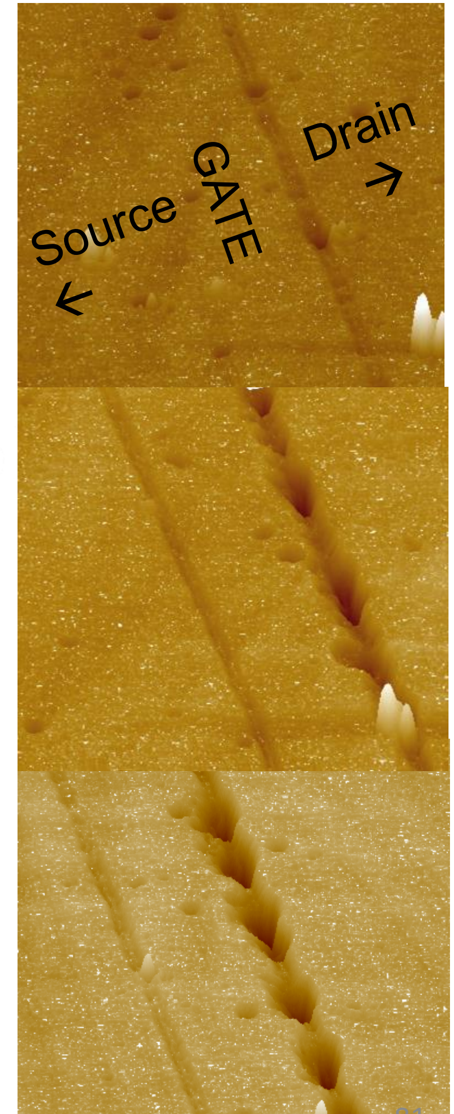
Pit formation in AlGaN barrier

3. Pit growth (to AlGaN/GaN interface) and merge

Joh, ROCS 2010

Makaram, APL 2010

Plan-view



Oxidation of the surface

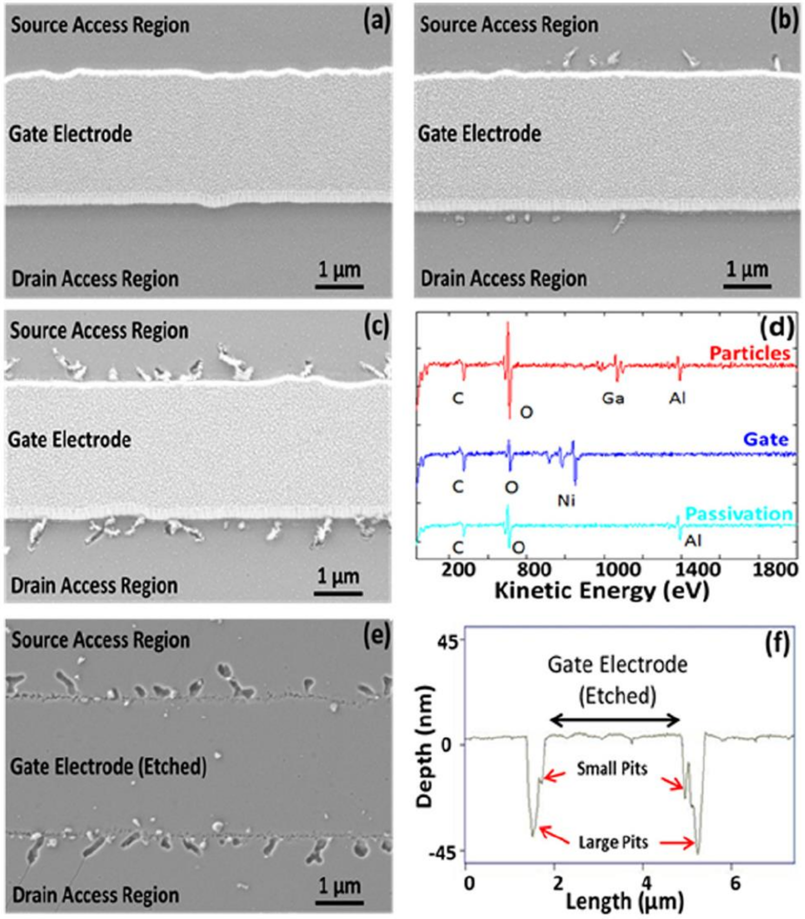


FIG. 1. (Color online) Top-view SEM images of an AlGaN/GaN HEMT stressed at $V_{ds} = 0$ V and $V_{gs} = -40$ V for 60 s (a), 600 s (b), and 6000 s (c). (d) Auger electron spectra results for three different regions of the transistor surface. Panel (e) shows the surface morphology of the device (c) after removal of the gate, and panel (f) shows an AFM depth profile across the gate electrode of the same device.

Gao et al., Appl. Phys. Lett. 99, 223506 (2011)

- Oxide particles were found to form along the gate edge of stressed devices (-40 V)
- When the gate electrode is removed, pits are seen to have formed underneath each particle
- Reverse-bias degradation can be due to the chemical oxidation of the nitride semiconductor surface
- GaN is decomposed to Ga^{3+} and nitrogen gas. The Ga^{3+} then reacts with oxygen ions or oxyanions to form Ga_2O_3. The supply of oxygen ions and oxyanions is therefore key for this reaction to happen

Redox in the off-state degradation of AlGaN/GaN HEMTs

Redox in the off-state degradation of AlGaN/GaN HEMTs

The surface electrochemical reactions

- ***Oxidation*** of $Al_xGa_{1-x}N$ (or GaN)

  $2Al_xGa_{1-x}N + 6\mathbf{h^+} = 2xAl^{3+} + 2(1-x)Ga^{3+} + N_2\uparrow$

  $2xAl^{3+} + 2(1-x)Ga^{3+} + 6\mathbf{OH^-} = xAl_2O_3 + (1-x)Ga_2O_3 + 3H_2O$

- ***Balance*** of H^+ and OH^-

  $H^+ + OH^- = H_2O$

- ***Reduction*** of hydrogen

  $2H^+ + 2\mathbf{e^-} = H_2\uparrow$

F. Gao et al., IEEE Trans. El. Dev. 61 (2) 2014 437-444

Complete balanced electrochemical reaction:

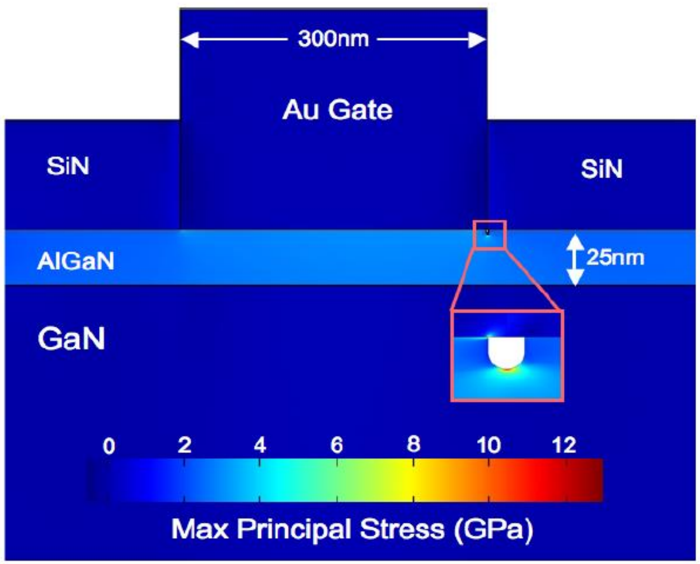
$$2Al_xGa_{1-x}N + 6h^+ + 6e^- + 3H_2O = xAl_2O_3 + (1-x)Ga_2O_3 + N_2\uparrow + 3H_2\uparrow$$

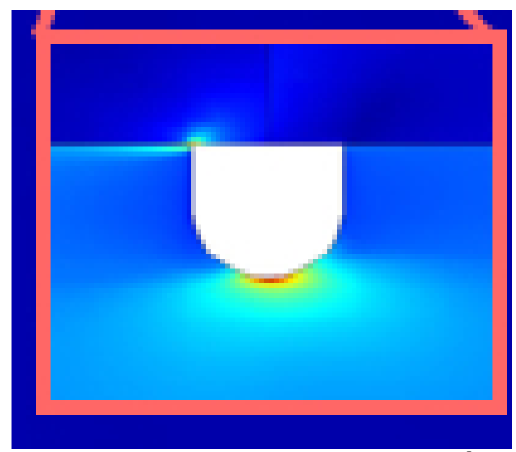
Multiphysics modeling of converse piezoelectric effect

Simulations : 0.3 μm gate HEMT 30% 25 nm AlGaN, 1.6 μm gate-drain spacing
junction temperature 400°C, peak E ~11.5 MV/cm stress 4.6 GPa

INTRINSIC DEVICE (NO PIT) : failure due to converse piezoelectric effect
is unlikely (piezoelectric contribution to stress 0.5 GPa, thermal 0.6 GPa)

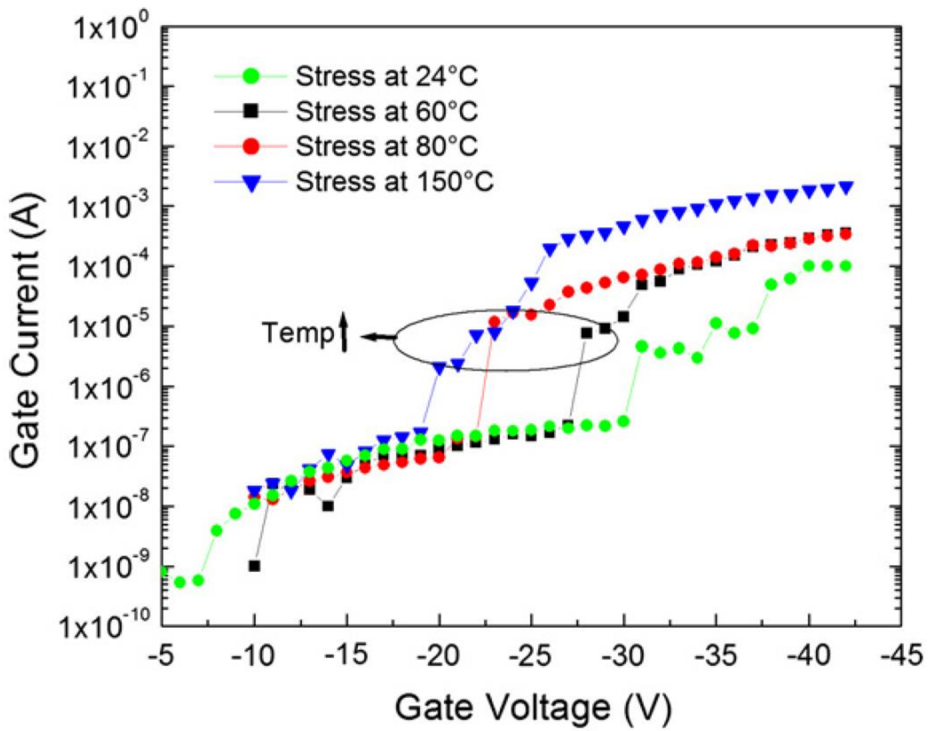
DAMAGED DEVICE (AFTER PIT FORMATION) : once a pit is formed
the strain under pit (2nm x 3nm) is much higher (13 GPa) and increases
if a crack is formed (35 GPa if crack transversed the AlGaN)

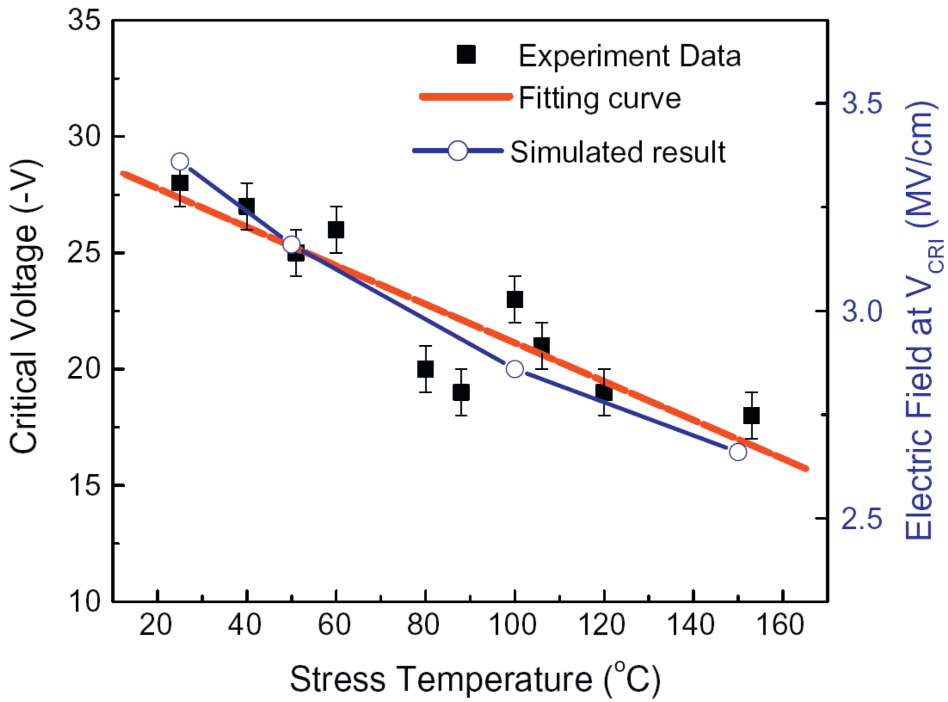




2011 Ancona et al. SISPAD

Critical voltage decreasing with temperature

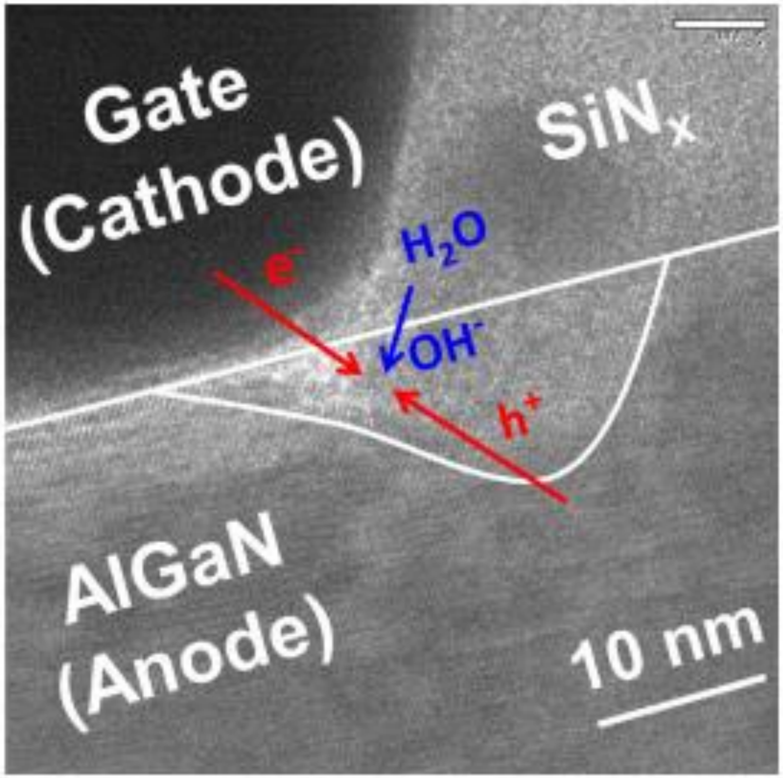




Both the critical voltage and the electric field value required to induce the abrupt increase of leakage decrease with temperature. Failure is attributed to GaO dissociation and NiO formation.

Douglas et al. Microel. Reliab. 52 (2012) 23-28

Oxidation of the surface



The gate-SiN-$Al_xGa_{1-x}N$ region at the gate edge forms an electrochemical cell which causes anodic oxidation of the $Al_xGa_{1-x}N$ layer

The reaction starts at the GaN cap surface and then proceeds into the AlGaN barrier during the electrical stress

$$2\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{N} + 3\mathrm{H_2O} = \mathrm{xAl_2O_3} + (1-x)\mathrm{Ga_2O_3} + \mathrm{N_2}\uparrow + 3\mathrm{H_2}\uparrow$$

Gao et al., IEEE TED 61, 437 (2014)

GaN-based HEMTs for power applications

Repeatability of experiments

- After the initial discovery of time-dependent breakdown effects in GaN by D. Marcon and coauthors [A], this failure mode has been observed several times [B], [C], [D],[E].

- (Defective) GaN behaves like an "imperfect insulator" under extreme electric field conditions

- Time-dependent breakdown failure modes in GaN-on-Si power HEMTs for switching applications have been observed in: vertical drain-to-substrate breakdown [F], breakdown of GaN HEMTs in off-state [G], [H], and forward-bias time-dependent leakage increase of p-gate of e-mode GaN HEMTs [I].

- Time dependent breakdown was also observed in reverse-biased InGaN/GaN LEDs [L].

[A] D. Marcon *et al.*, *Phys. Status Solidi Curr. Top. Solid State Phys.*, vol. 6, no. SUPPL. 2, pp. 1–5, 2009. [B] M. Meneghini *et al.*, *Appl. Phys. Lett.*, vol. 100, no. 3, pp. 4–7, 2012. [C] D. Marcon *et al.*, *IEEE IEDM*, pp. 472–475, 2010. [D] M. Meneghini *et al.*, *CS MANTECH Conf.*, no. iv, 2012. [E] M. Meneghini *et al.*, *IEEE IEDM*, pp. 469–472, 2011. [F] M. Borga *et al.*, *IEEE Trans. Electron Dev.*, vol. 64, no. 9, pp. 3616–3621, 2017. [G] M. Meneghini *et al.*, *IEEE Trans. El. Dev.* vol. 62, no. 1, pp. 1–6, 2015. [H] J. Hu *et al.*, IEEE El. Dev. Lett. vol. 38, no. 3, pp. 371–374, 2017. [I] I. Rossetto *et al.*, IEEE Trans. El. Dev. 62 (8), pp. 35–38, 2016. [L] C. De Santi, M. Meneghini, M. Buffolo, G. Meneghesso, and E. Zanoni, *IEEE Electron Device Lett.*, vol. 37, no. 5, pp. 611–614, 2016.

Two different mechanisms: TDDB vs surface pitting

- Time-dependent breakdown due to formation of percolation path → Gate leakage current increase (without drain current decrease and pitting)

- Surface pitting (possibly due to a combination of electrochemical surface oxidation and converse piezoelectric effect → Drain current decrease

- Pitting requires an oxidizing ambient, is accelerated by power and temperature
 Pitting is not always found after reverse bias experiments in off-state

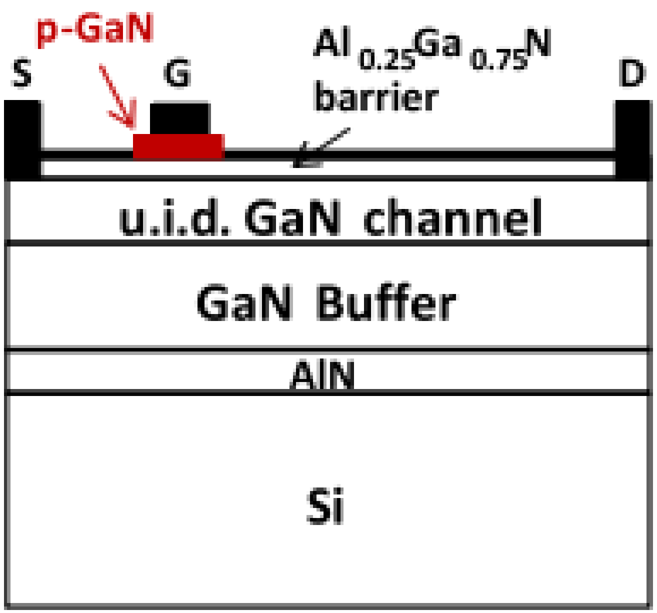
- Percolation model is in agreement with data showing that degradation of gate leakage current and subthreshold voltage swing, observed after step-stress tests in off-state, can be completely recovered by 10 min. annealing at 450°C in nitrogen. Thermal annealing also recovers small-signal rf characteristics of devices.

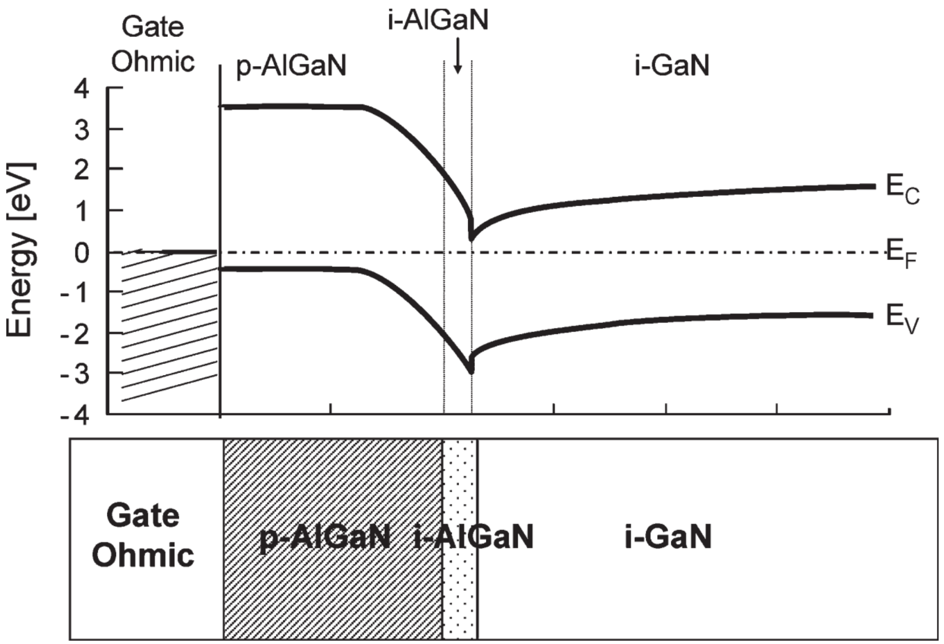
- This rules out both metal-semiconductor interdiffusion and electrochemical Ga oxidation as possible failure mechanisms since they can not obviously reversed by a high temperature treatment.

B.-J. Kim *et al.*, “Recovery in dc and rf performance of off-state step-stressed AlGaN/GaN high electron mobility transistors with thermal annealing,” *Appl. Phys. Lett.*, vol. 106, no. 15, pp. 271–274, 2015.

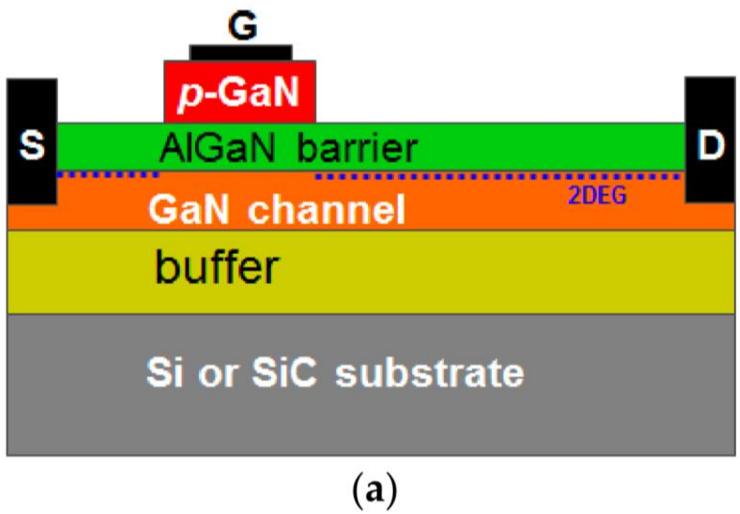
Today the most popular normally off device

GaN-HEMTs: Degradation of the p-GaN gate stack

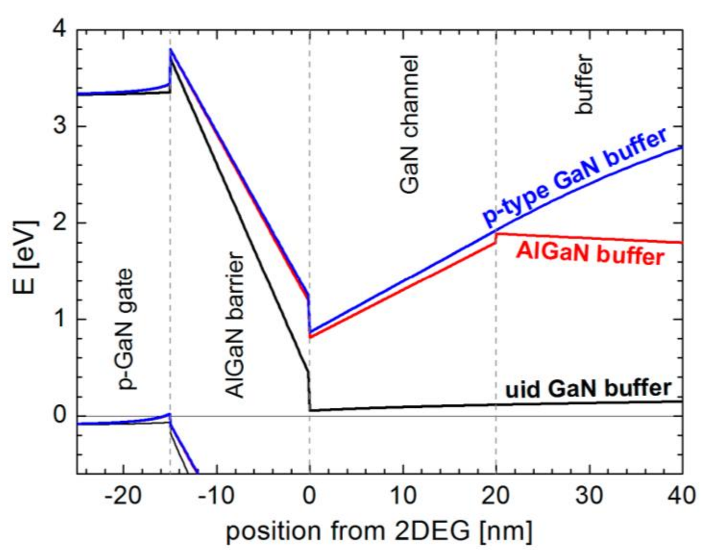




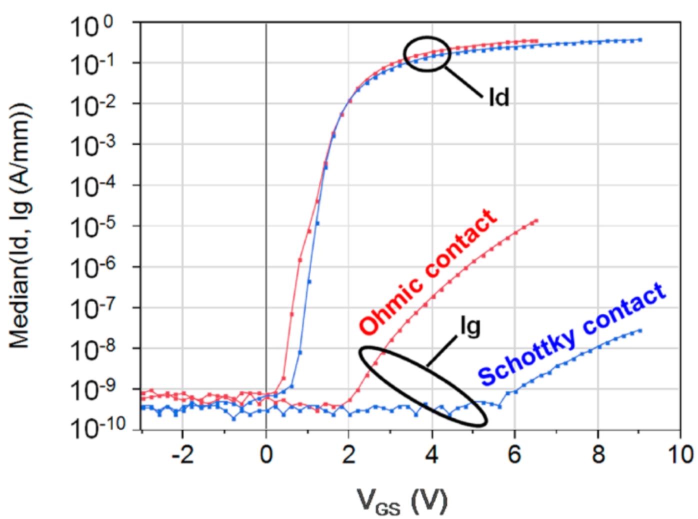
HEMTs with p-GaN gate: structure, advantages



(a)

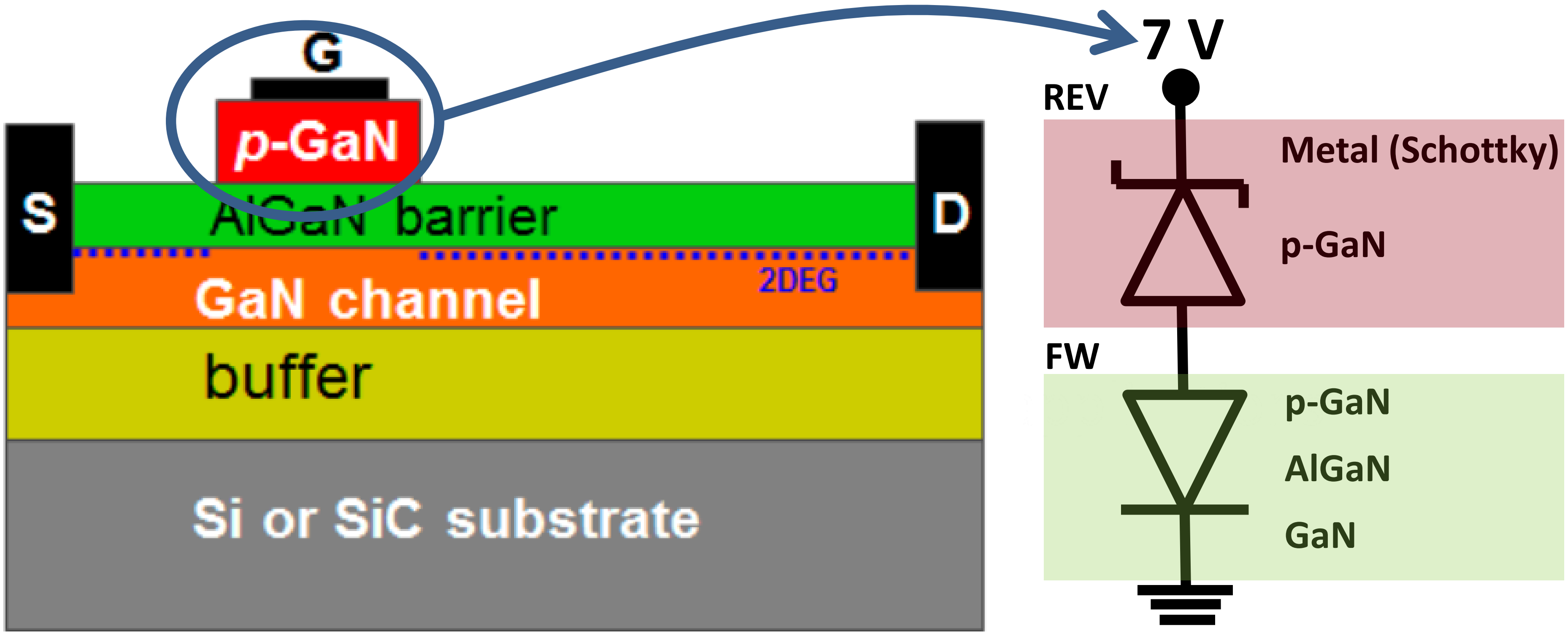


- A p-GaN layer can be used to reach normally-off operation
- A **backbarrier** can further lift the conduction band near the channel, thus further increasing V_{th}
- A Schottky-type contact further reduces gate leakage (robustness?)



Meneghini, Energies **2017**, *10*, 153

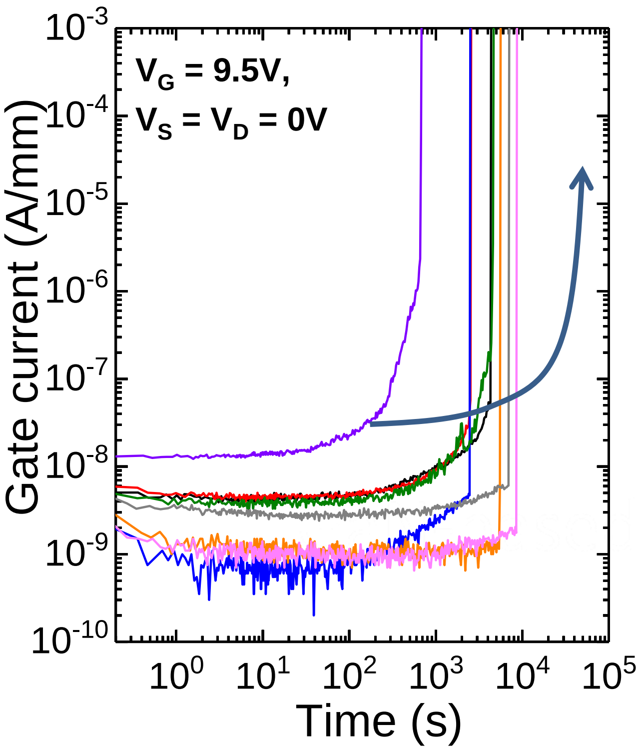
Degradation of the p-GaN gate



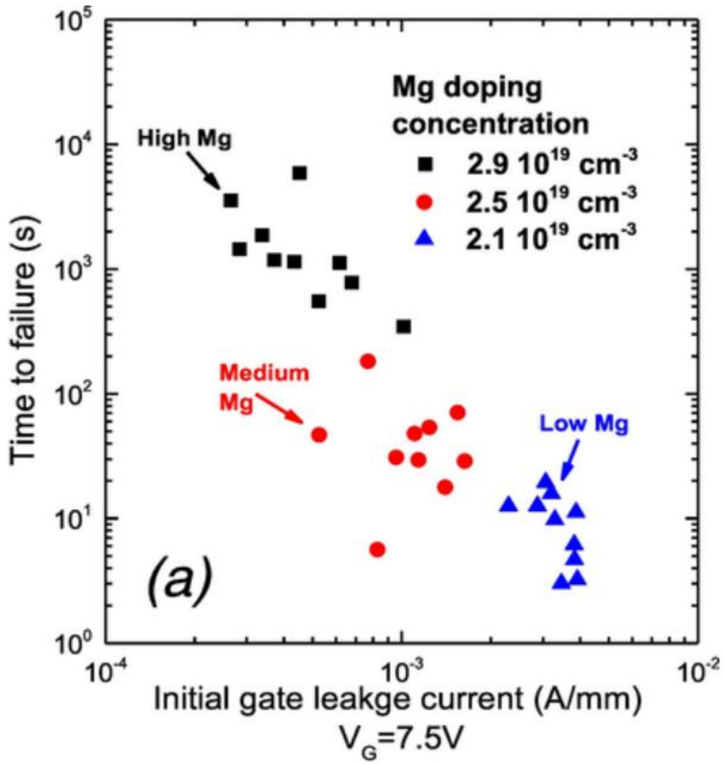
UNIPD & imec, IRPS 2017 and ESREF 2017
UNIPD & FBH, Energies 2017

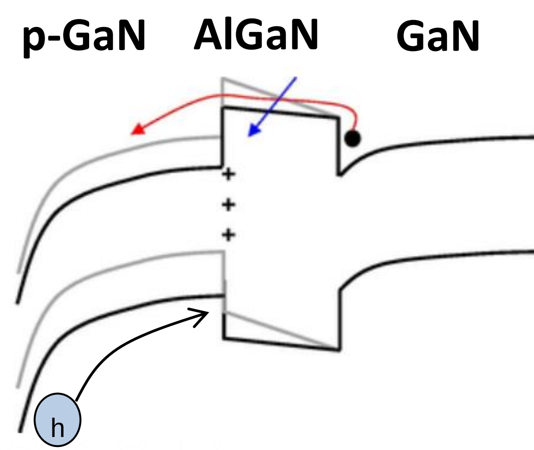
Degradation of the p-GaN gate

Constant voltage stress



TTF correlated with Ig





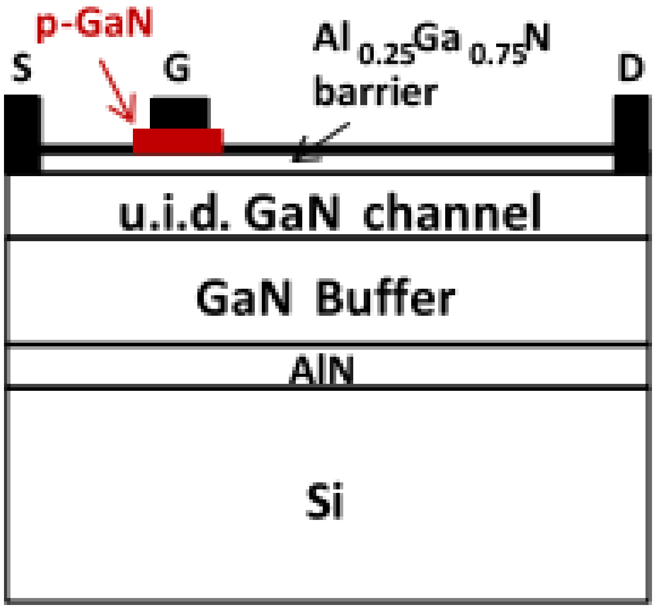
- dc stress → Accumulation of positive charges at the p-GaN/AlGaN interface promotes an increase in leakage current → **This explains why TTF is strongly depends on gate leakage**
- **Low magnesium is weaker,** since it has a lower leakage current
- Optimizing barrier improves TTF (Stoffels, IRPS2017)

See also:
Ťapajna, IEEE-EDL vol. 37, no. 4, 2016
Stoffels, IRPS 2017
Tallarico, IEEE-TED 38, 99, 2018

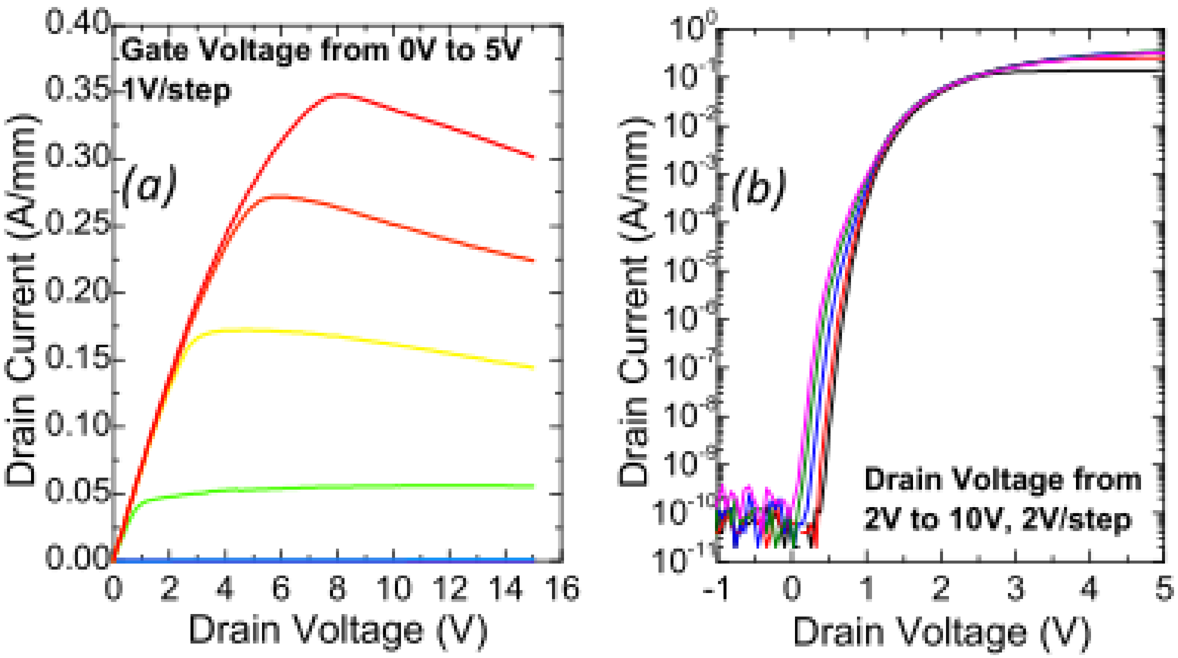
UNIPD & imec, IRPS 2017 and ESREF 2017

PowerBase

Degradation of the p-GaN gate

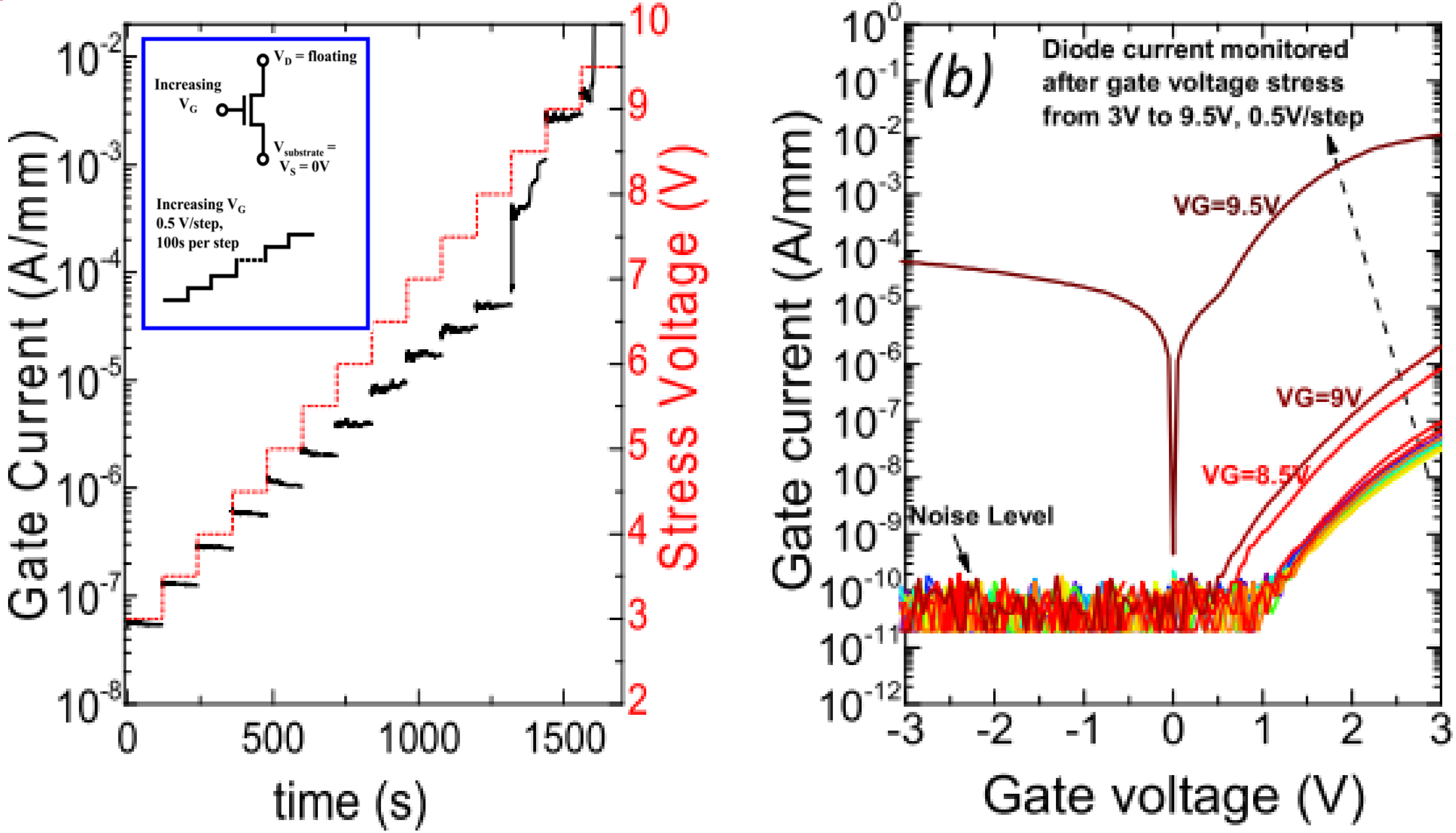


Normally-off transistors with p-GaN gate are exposed to high gate bias (>6 V) → Is the p-GaN/i-AlGaN junction stable at positive gate bias?



Rossetto et al., IEEE TED 63, 2334 (2016)

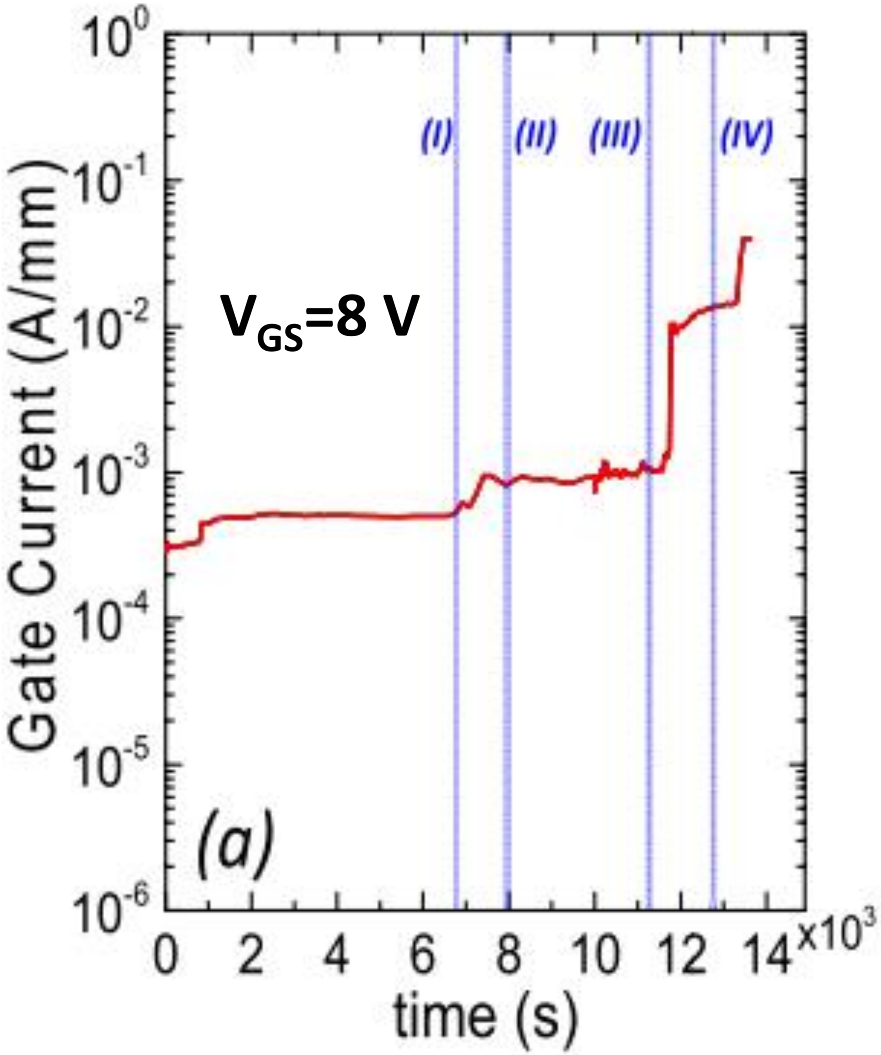
Step-stress (positive gate bias, source grounded)

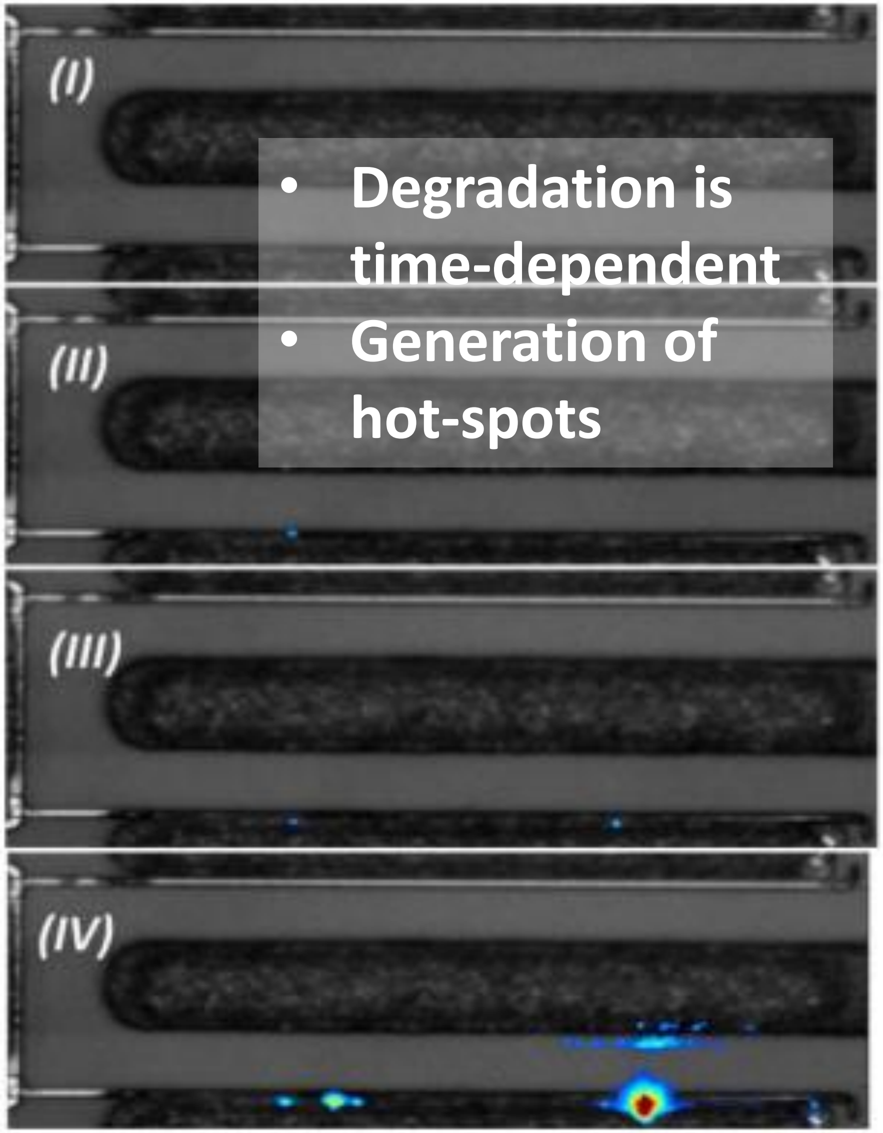


A step-stress test results in the failure of the gate junction → What is the physical origin? AlGaN? p-GaN? Dielectrics?

Rossetto et al., IEEE TED 63, 2334 (2016)

A time-dependent mechanism…

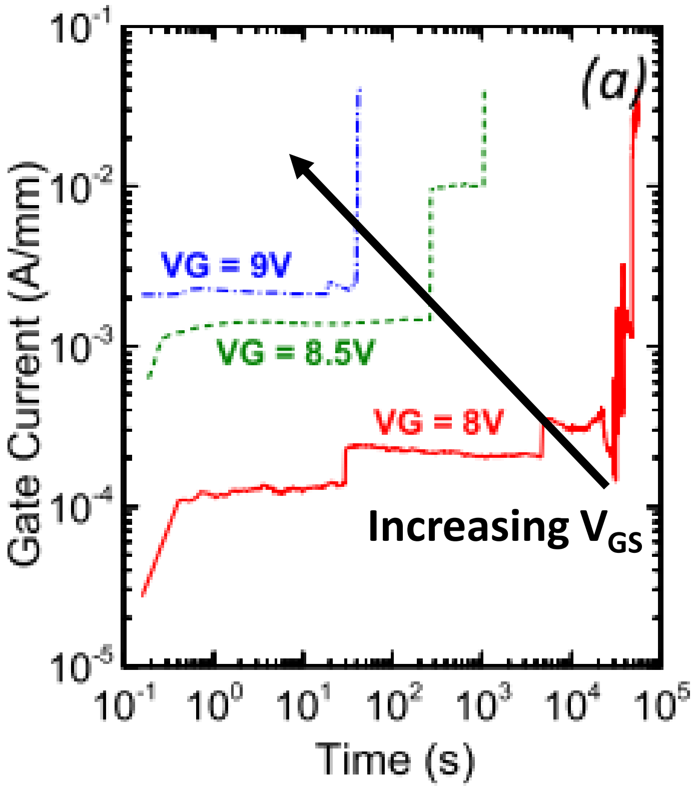


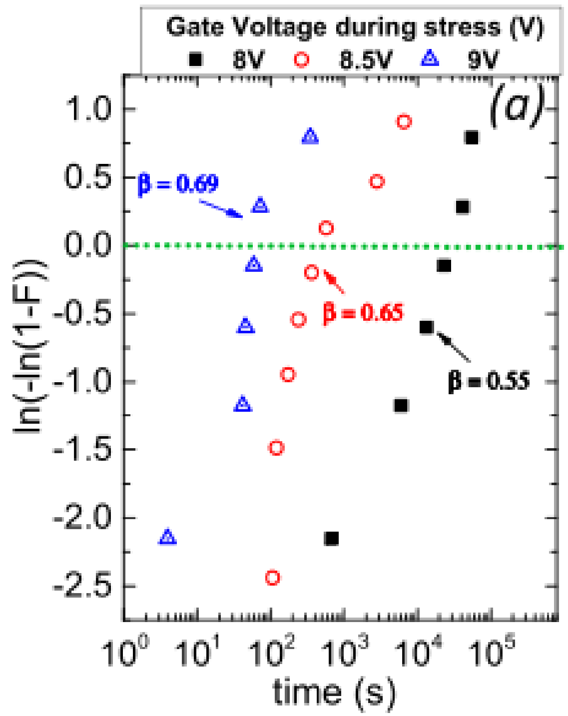


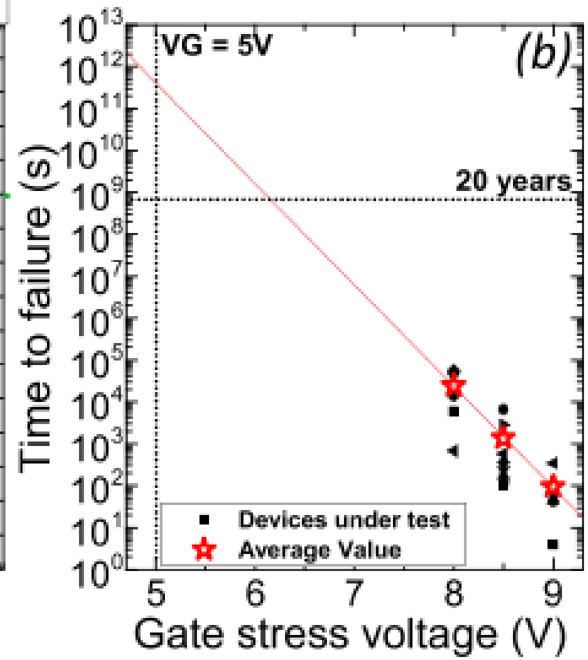
- Degradation is time-dependent
- Generation of hot-spots

Rossetto et al., IEEE TED 63, 2334 (2016)

Gate stability in p-GaN HEMTs: dependence on voltage



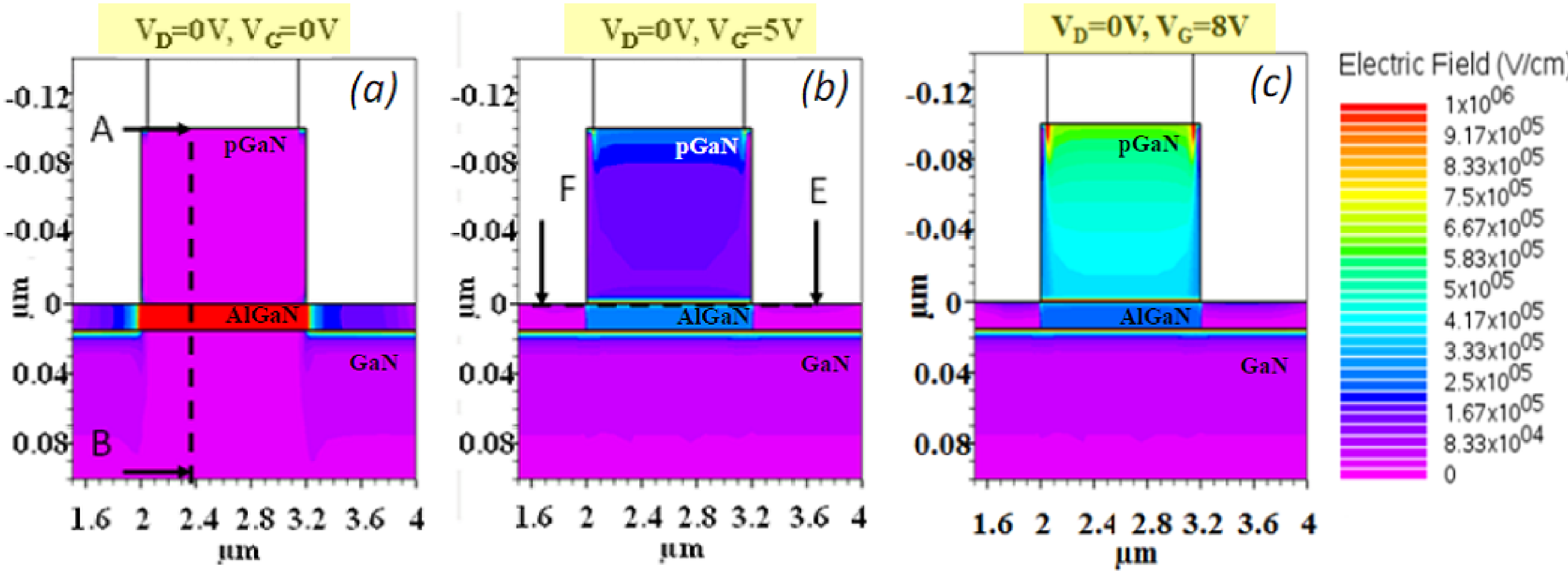




- TTF follows a Weibull distribution, with a shape factor β of 0.55–0.7, suggesting an extrinsic breakdown mechanism
- 20 years lifetime extrapolated for V_{GS}=5 V

Rossetto et al., IEEE TED 63, 2334 (2016)

Physical origin of the degradation

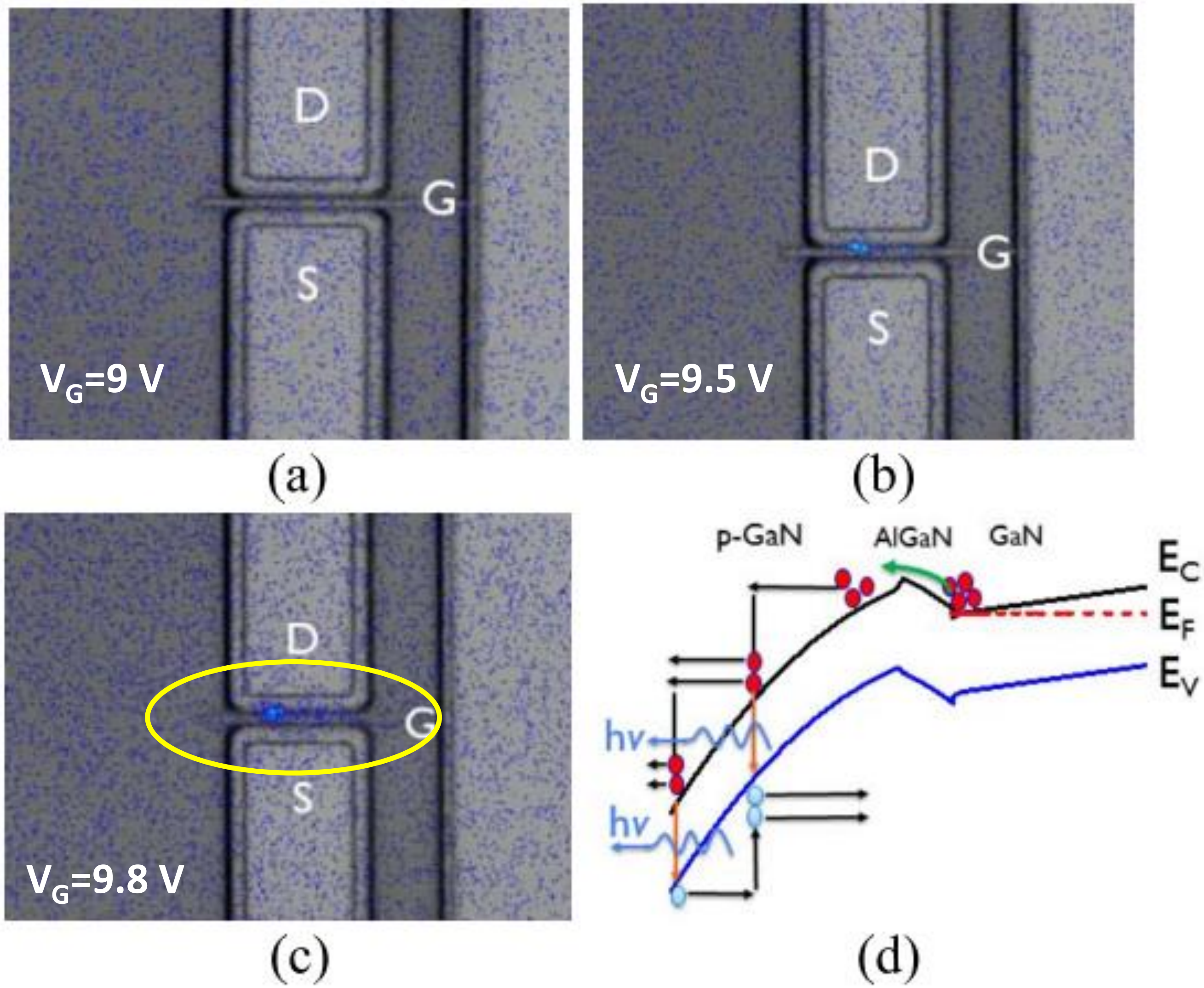


At high gate bias:

- Electric field in the AlGaN decreases → Not a source of degradation
- Electric field in the p-GaN increases → Possibly leading to the degradation (close to the surface, Schottky vs Ohmic contact…)

Rossetto et al., IEEE TED 63, 2334 (2016)

Avalanche effects



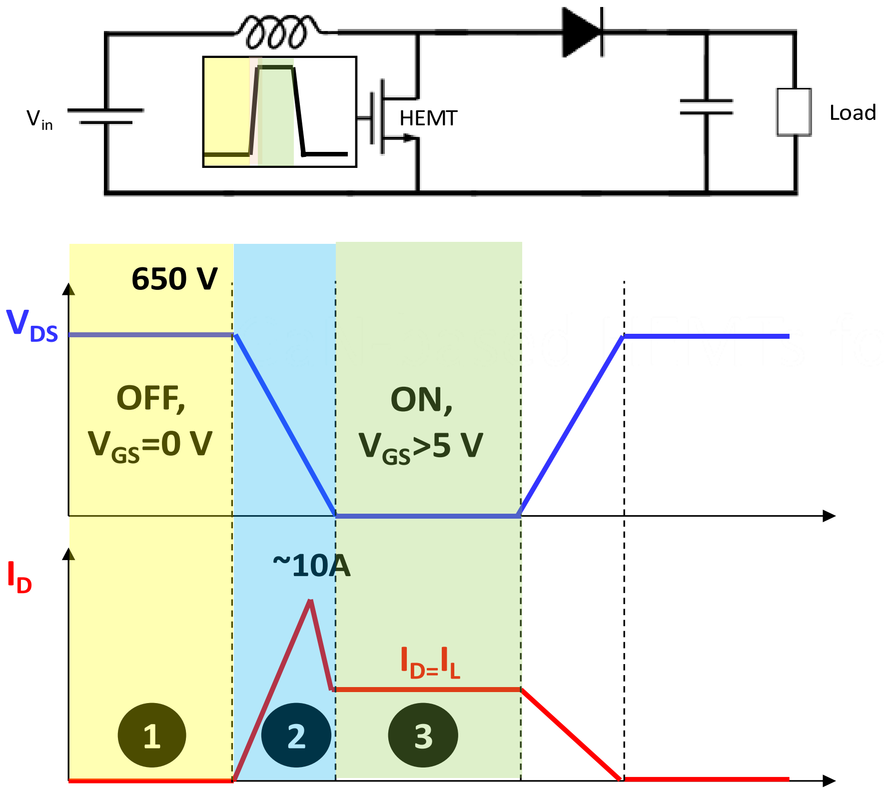
Avalanche effects may play a role in HEMTs with p-GaN gate

Electrons are injected from the channel over the AlGaN barrier, and are accelerated by the electric field in the p-GaN

This may accelerate device degradation

Wu et al., IEEE EDL 36, 1001 (2015)

What are the most stressful regimes?



1. Off-state, high lateral and vertical field (dielectric failure, GaN TBD)

2. Hard-switching, hot electrons and self-heating

3. ON-state, positive gate, p-GaN or gate dielectric degradation

Meneghini et al., Energies 2017, 10, 153

Power HEMTs: dc breakdown voltage

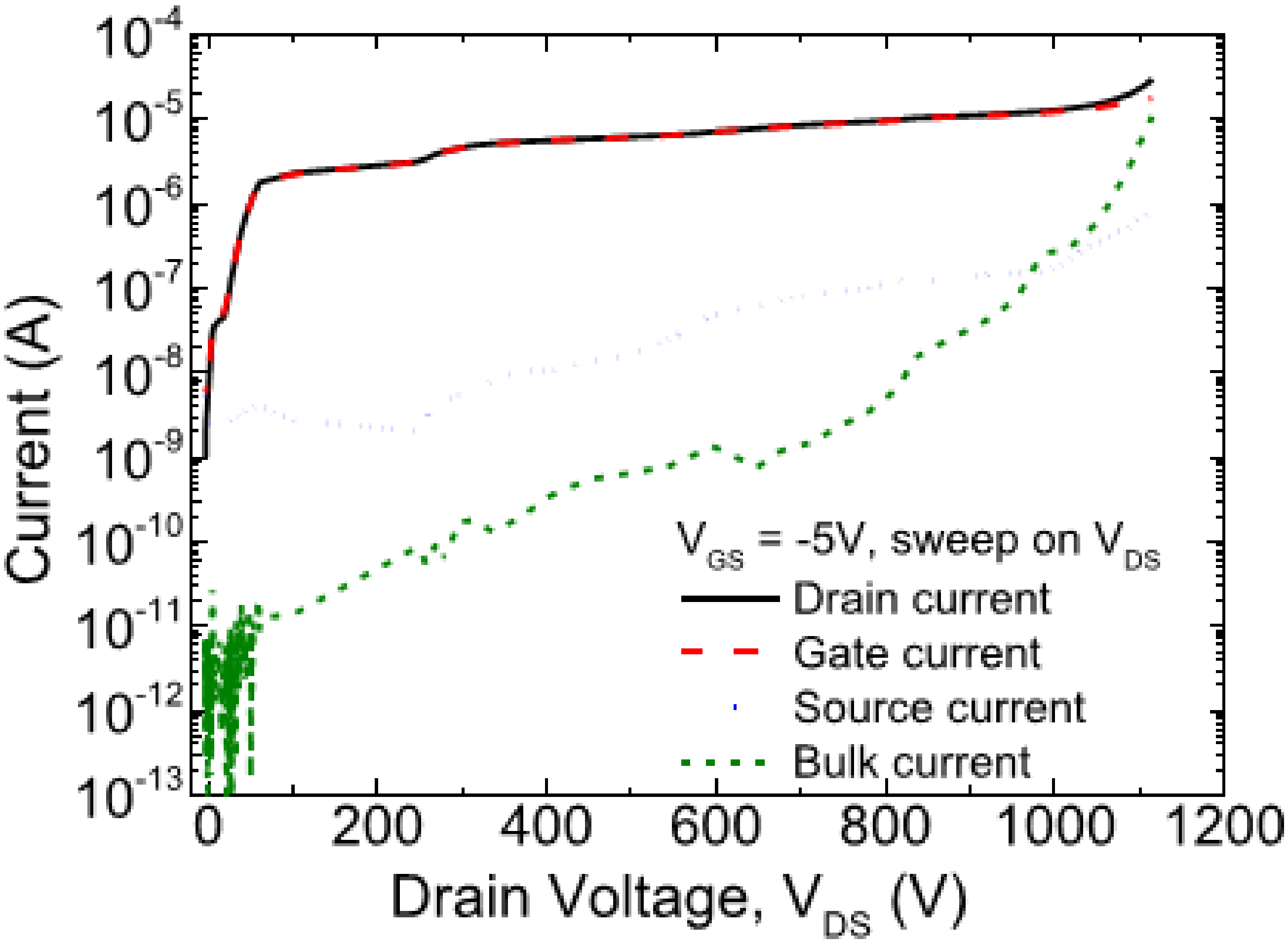


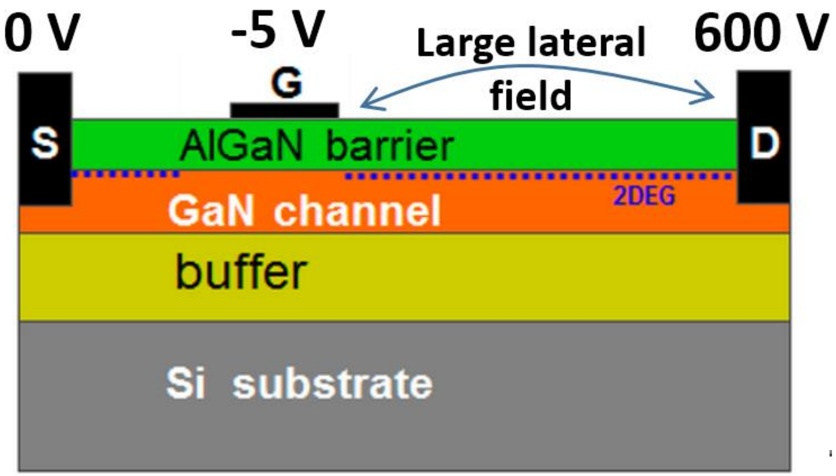
Fig. 1. Current–voltage I_D–V_{DS} curves measured with $V_{GS} = -5$ V on one of the analyzed devices. The individual contributions of drain (I_D), gate (I_G), source (I_S), and bulk (I_B) current are shown.

Meneghini et al., IEEE TED 62, 2594 (2015)

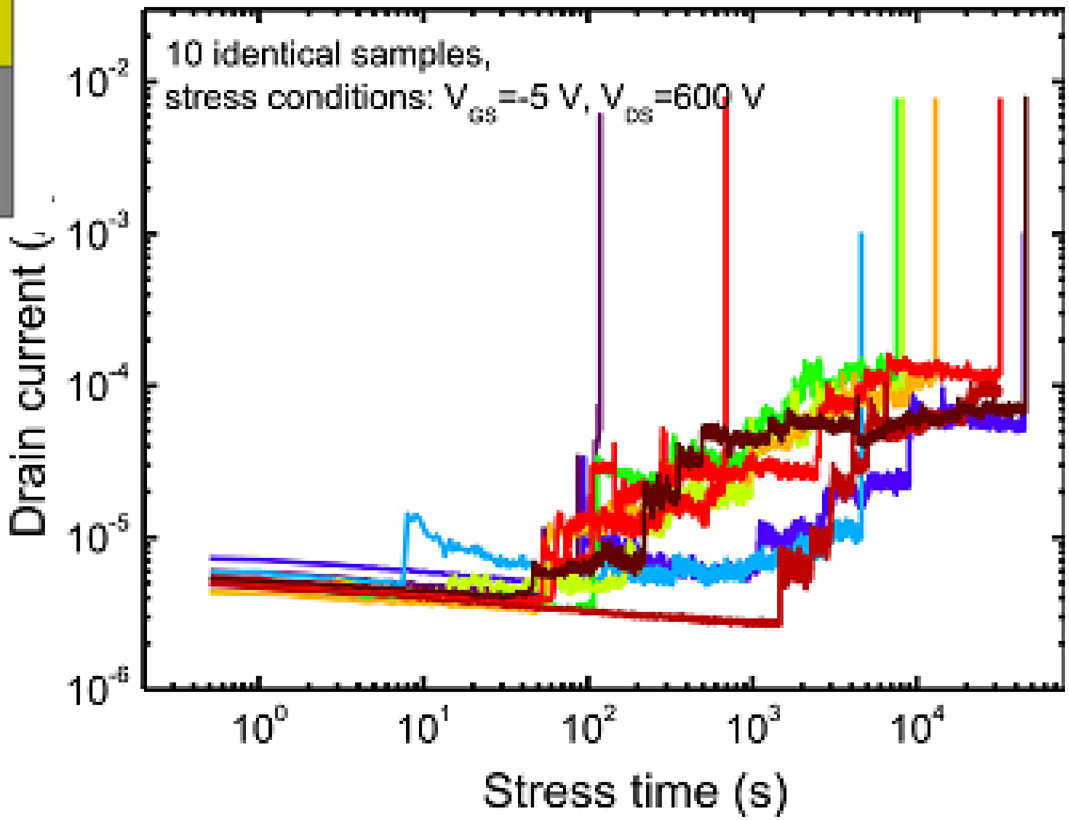
The samples have a breakdown voltage of V_{BD}~1100 V (evaluated at 3×10^{-5} A) with the drain leakage in OFF-state dominated by the reverse current of the gate Schottky junction

A significant contribution of buffer leakage becomes visible only for drain voltages higher than 800 V

Off-state: Lateral (extrinsic) failures → Dielectric-related



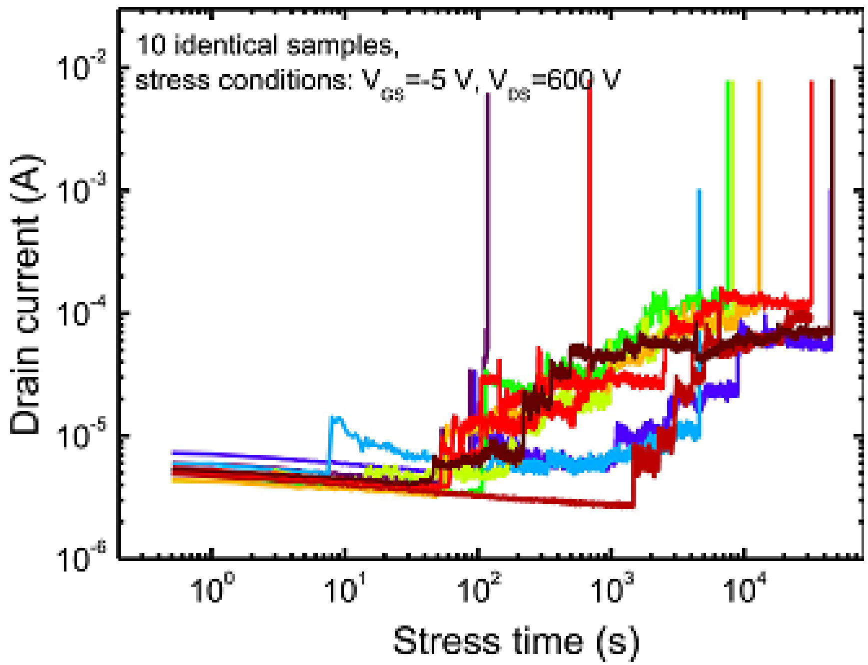
OFF-state stress induces time-dependent breakdown

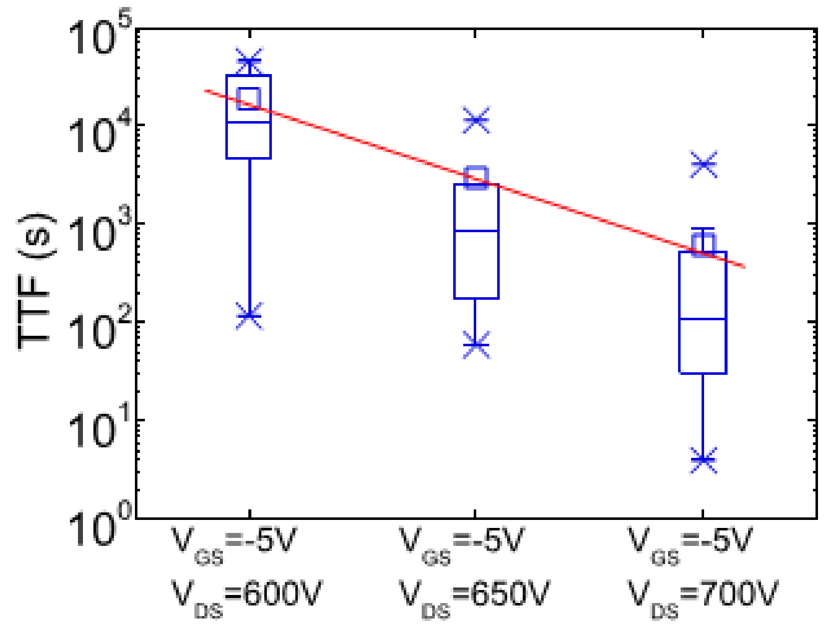


Which is the failure location '

AlGaN ?
GaN ?
dielectric ?

Time-dependent breakdown during constant voltage stress



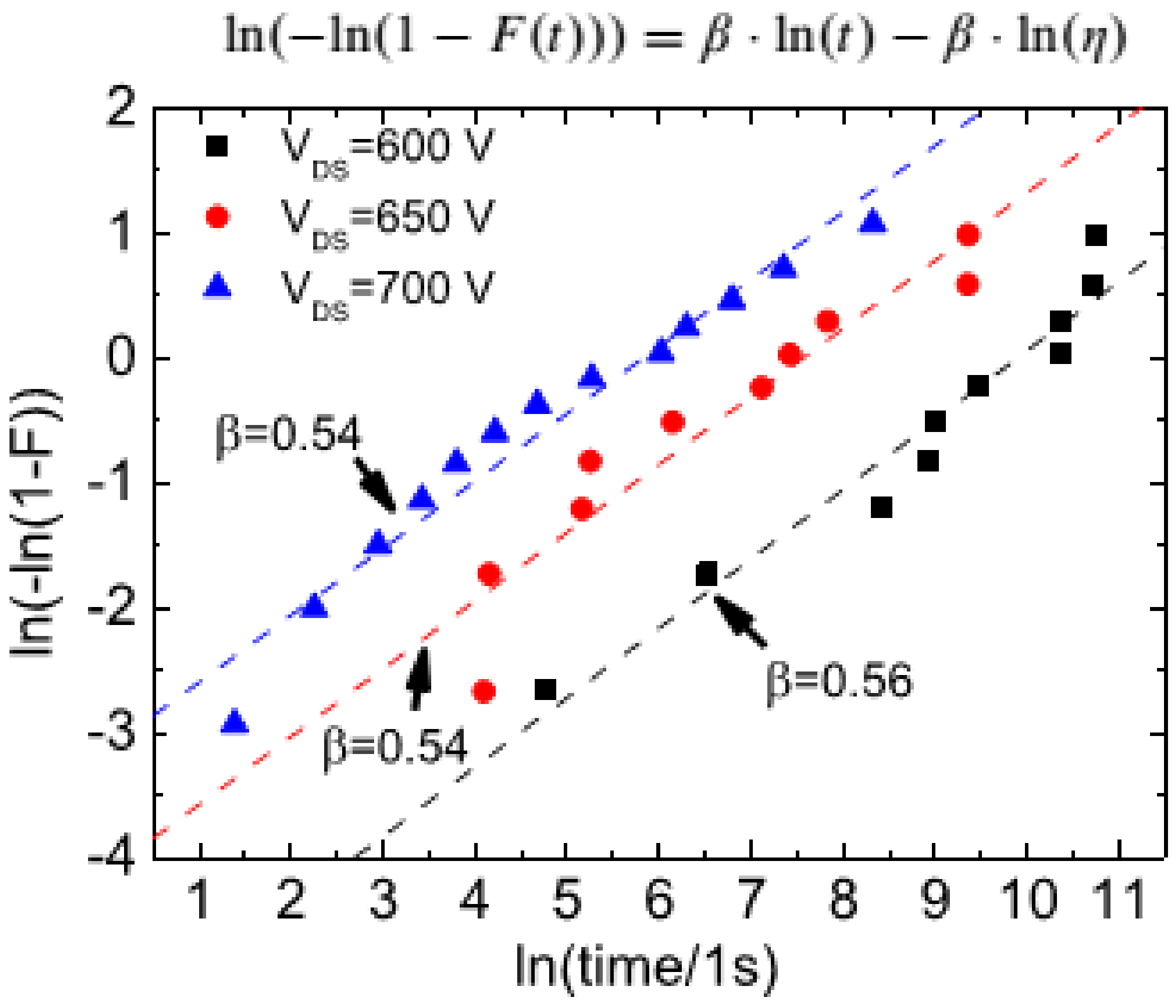


- Time-dependent degradation process at a voltage significantly lower than the breakdown voltage estimated by dc measurements (1100 V)

- TTF is exponentially dependent on stress voltage VDS

Meneghini et al., IEEE TED 62, 2594 (2015)

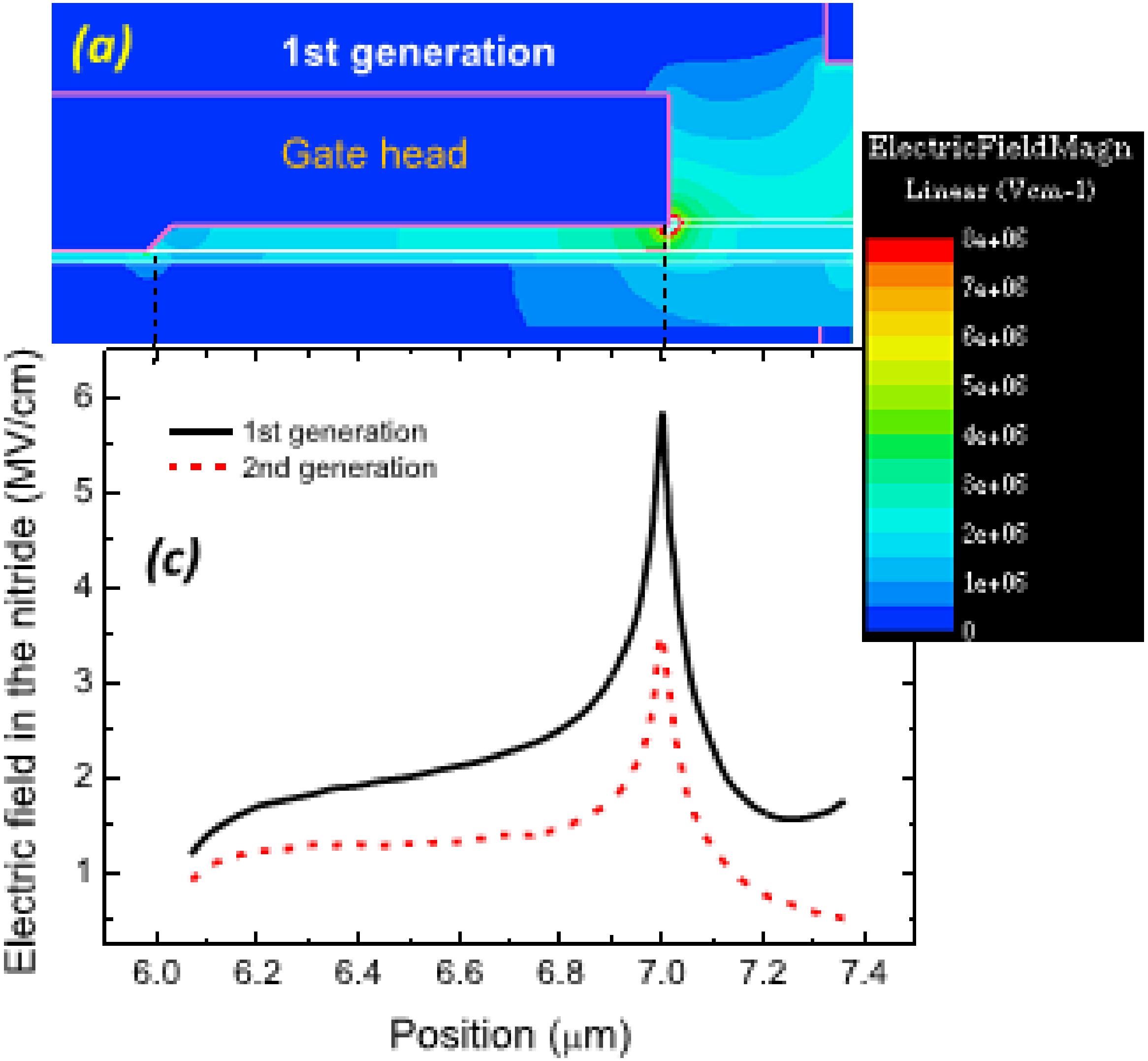
Weibull-distributed breakdown in OFF-state



- TTF is Weibull distributed (dielectrics? extrinsic failure?)

Meneghini et al., IEEE TED 62, 2594 (2015)

2D simulations under off-state conditions (V_{DS}=500 V)

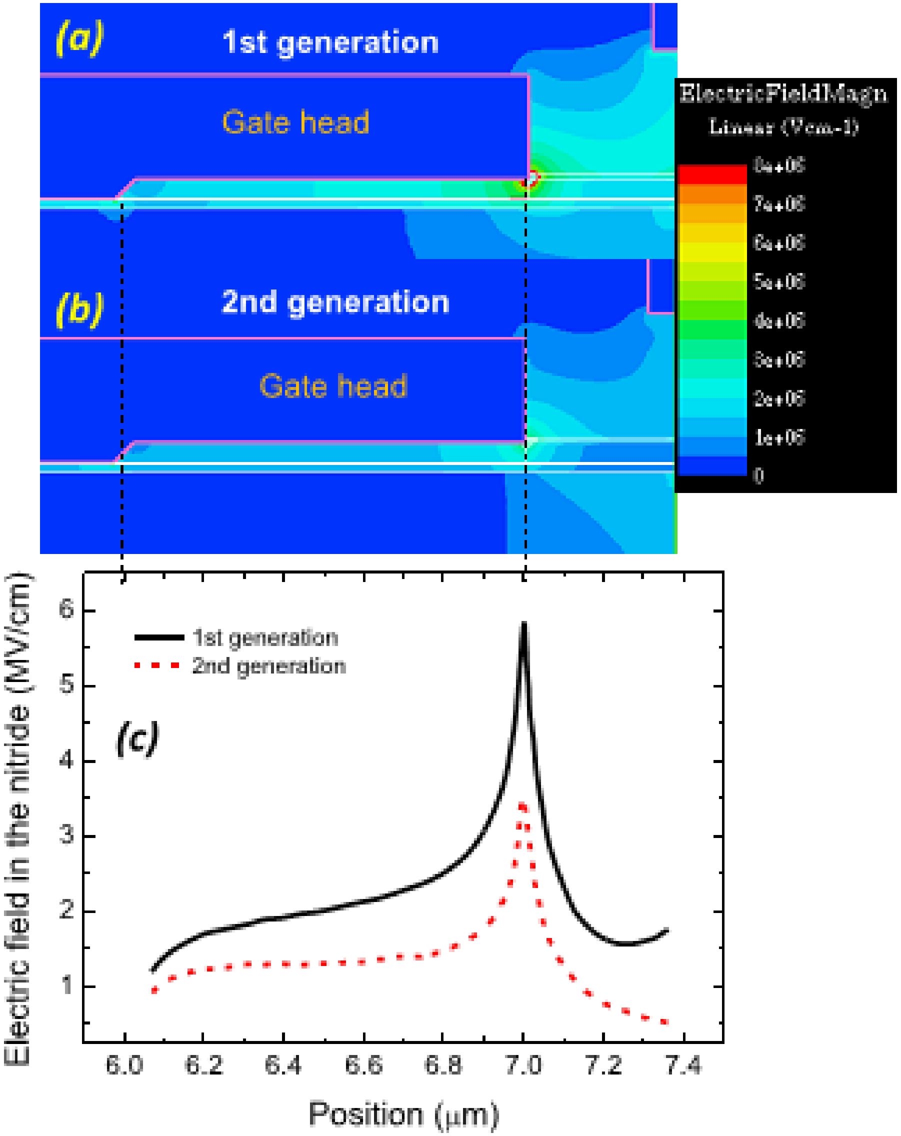


Meneghini et al., IEEE TED 62, 2594 (2015)

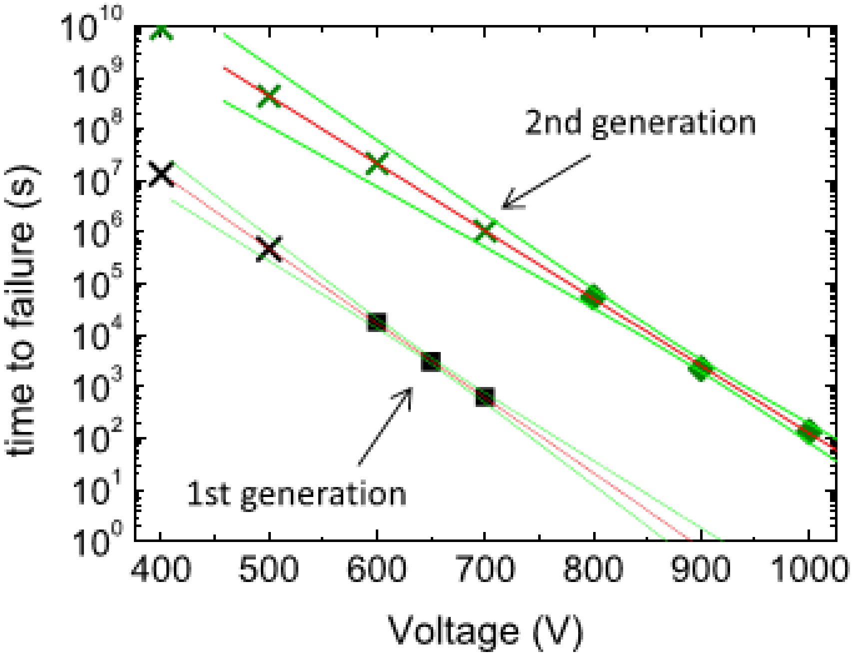
The electric field in the nitride reaches its maximum in proximity of the edge of the gate overhang, on the drain side; the peak field is 6 MV/cm, and is therefore comparable with the breakdown strength of SiN (~6 MV/cm)

On the other hand,
under the same conditions the electric field in the AlGaN layer
was found to be lower than 3 MV/cm (i.e., lower than the breakdown field of AlGaN)

2D simulations: GEN1 Vs GEN2

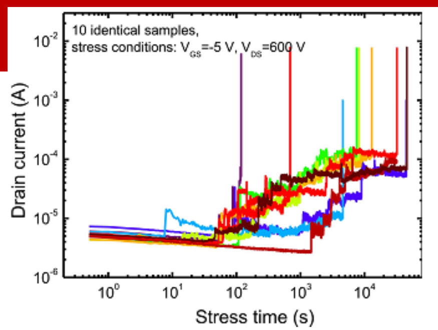


Significant decrease in the electric field in Gen-2 devices, leading to increased lifetime

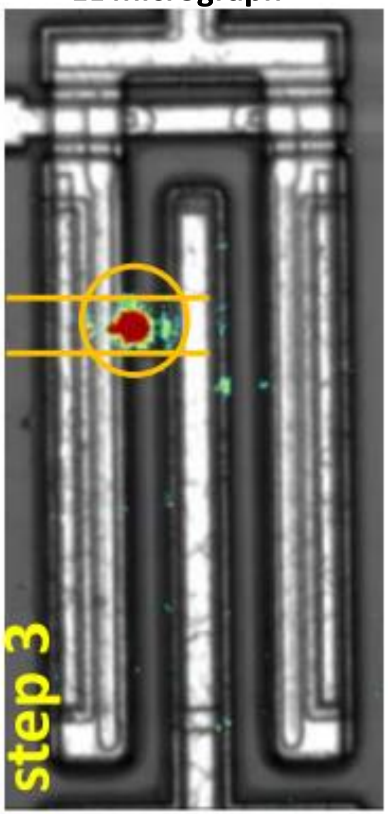


Meneghini et al., IEEE TED 62, 2594 (2015)

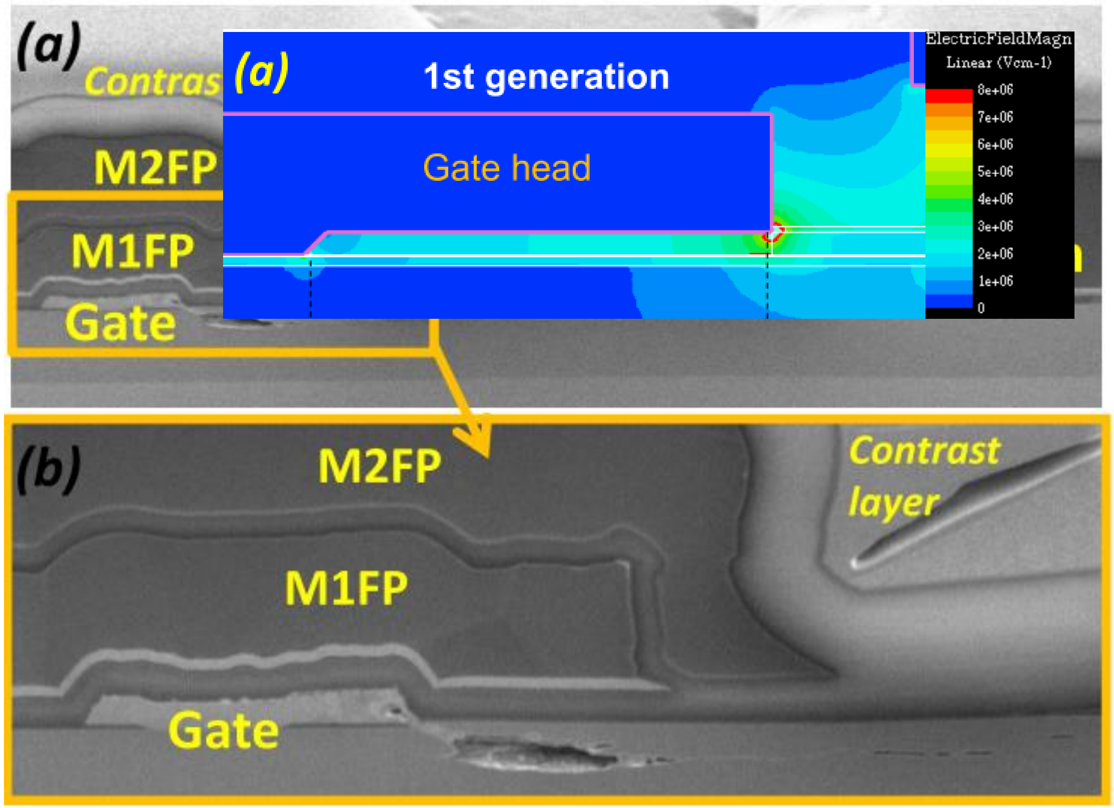
Extrinsic failures → Dielectric-related



EL micrograph



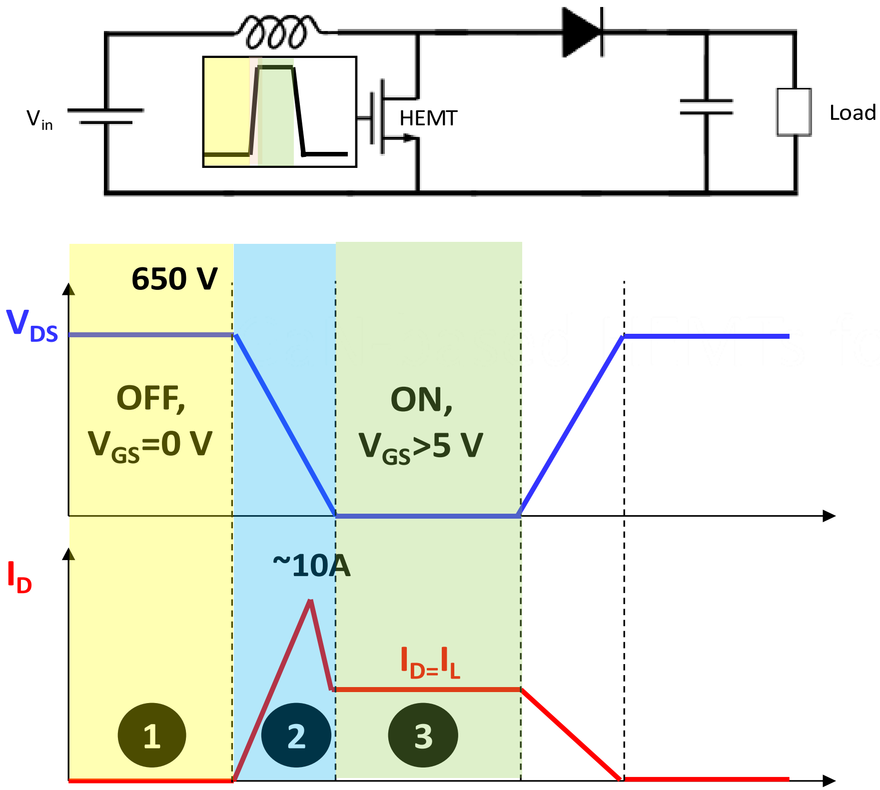
x-section



FIB x-section indicates the presence of a weak spot under the gate edge (on the drain side) → **dielectric failure**

UNIPD & NXP, Rossetto et al., IEEE-TED 64, 73 (2017)

What are the most stressful regimes?



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2. Hard-switching, hot electrons and self-heating

3. ON-state, positive gate, p-GaN or gate dielectric degradation

Meneghini et al., Energies 2017, 10, 153

How to test devices in hard switching?

Previous publications on the topic

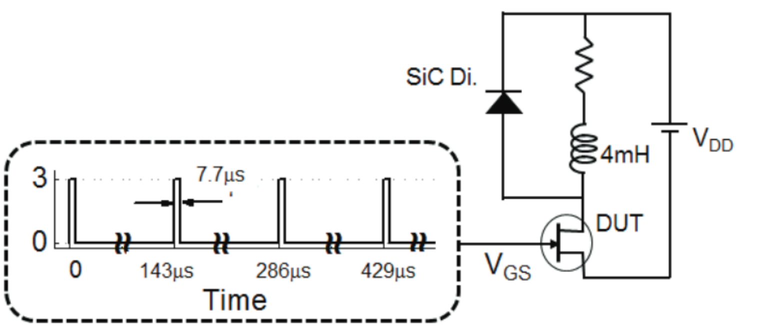
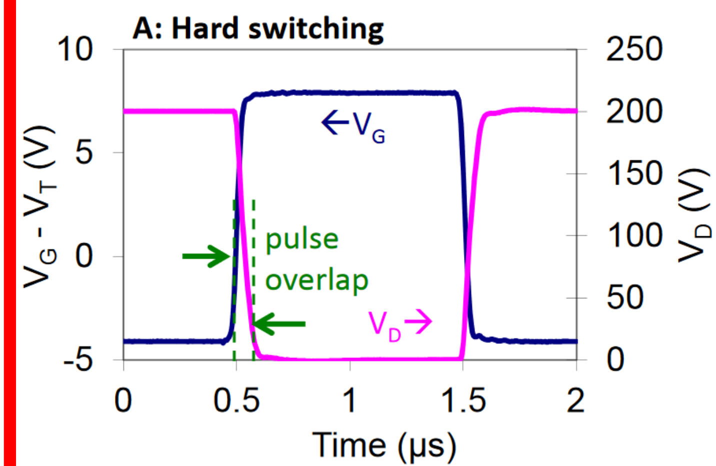


Fig. 10: Electric circuit for dynamic high temperature operation life (D-HTOL) test. DUT is the devices tested

K. Tanaka et al., IEEE-IRPS 2017



J. Joh et al., IEEE-IRPS 2014

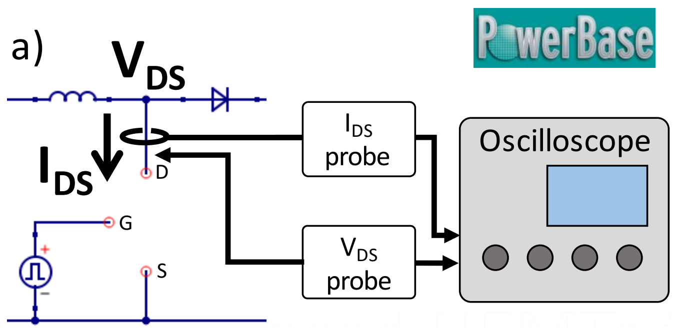
I. Rossetto et al., IEEE-TED 64, 3734 (2017)

Works on packaged parts
(e.g. 10 A switching current)

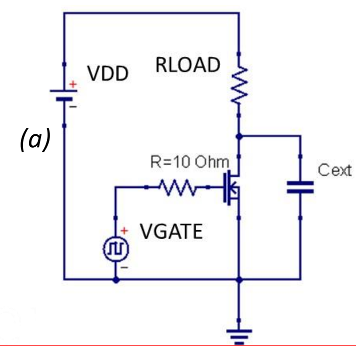
Non-realistic waveforms, pulse overlap is changed to induce hard switching

Two novel setups for on-wafer hard switching test

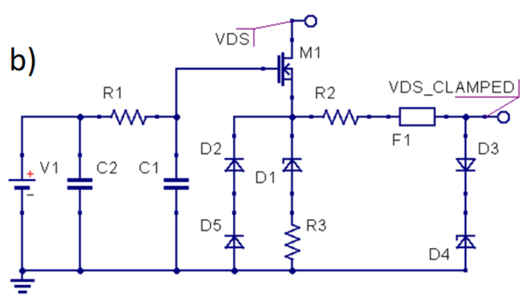
On-wafer boost converter

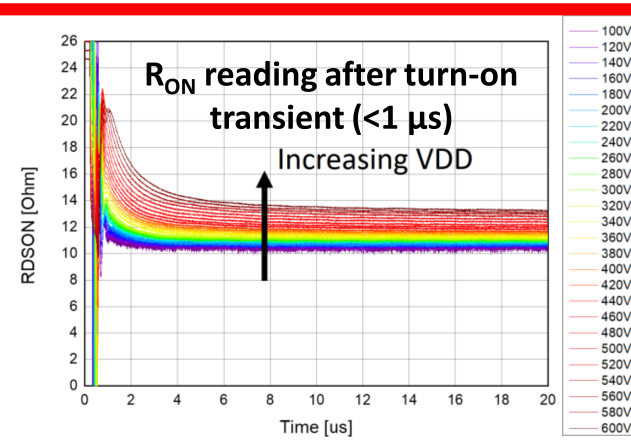


Capacitor-based circuit

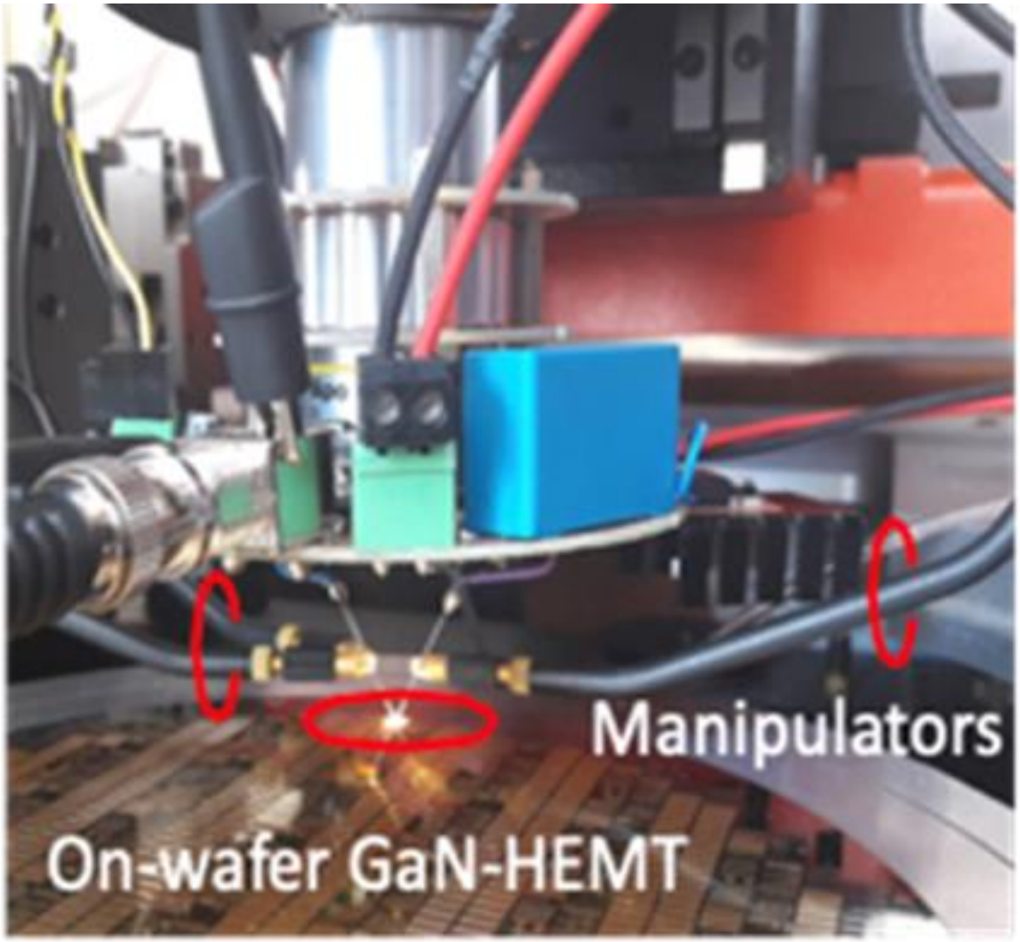


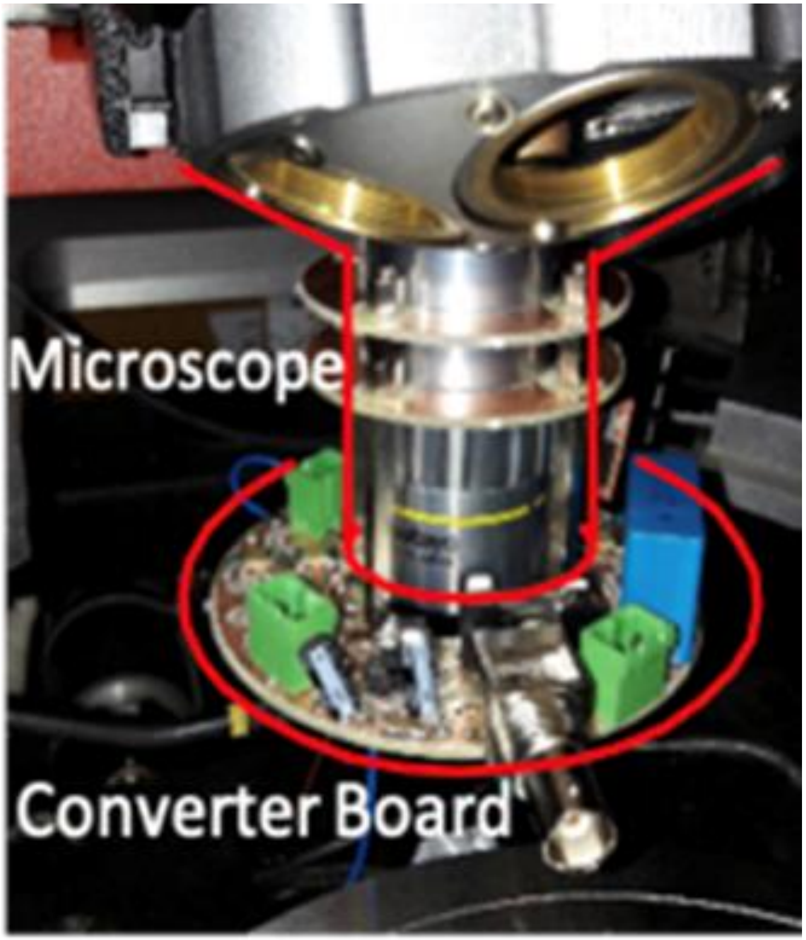
Clamp circuit to get fast scope reading



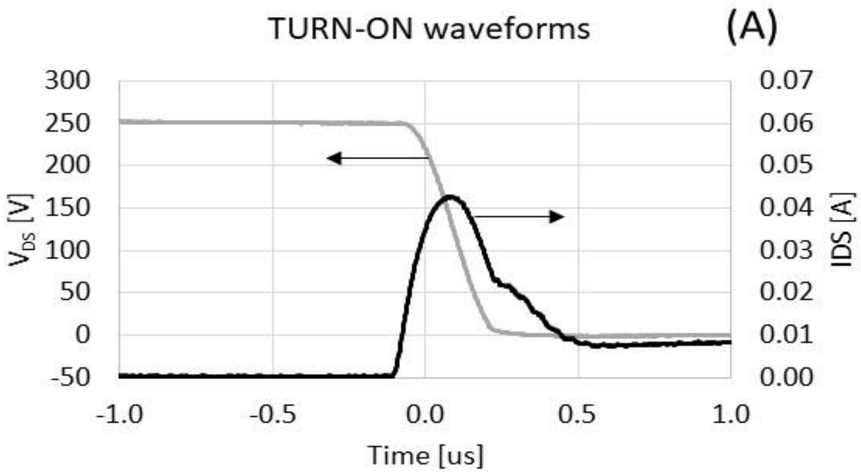


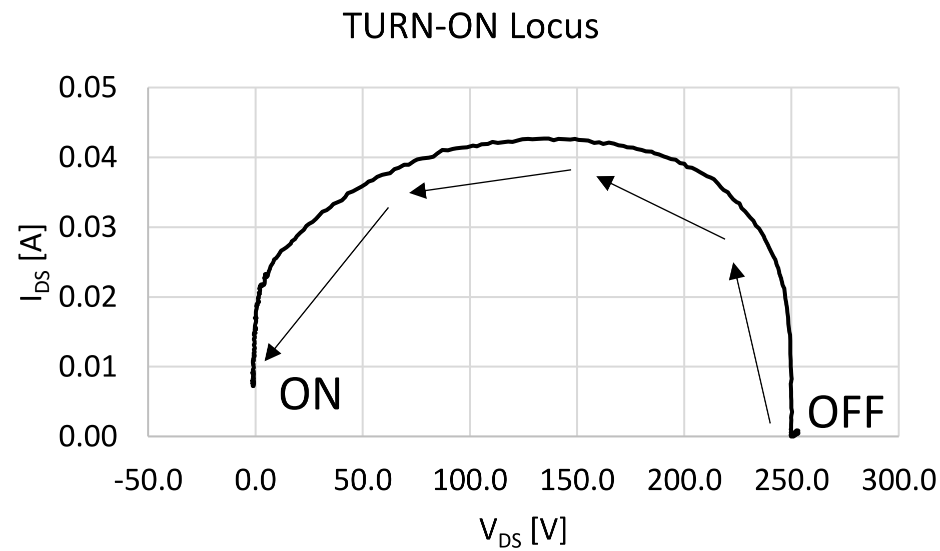
Novel setups for on-wafer hard switching test





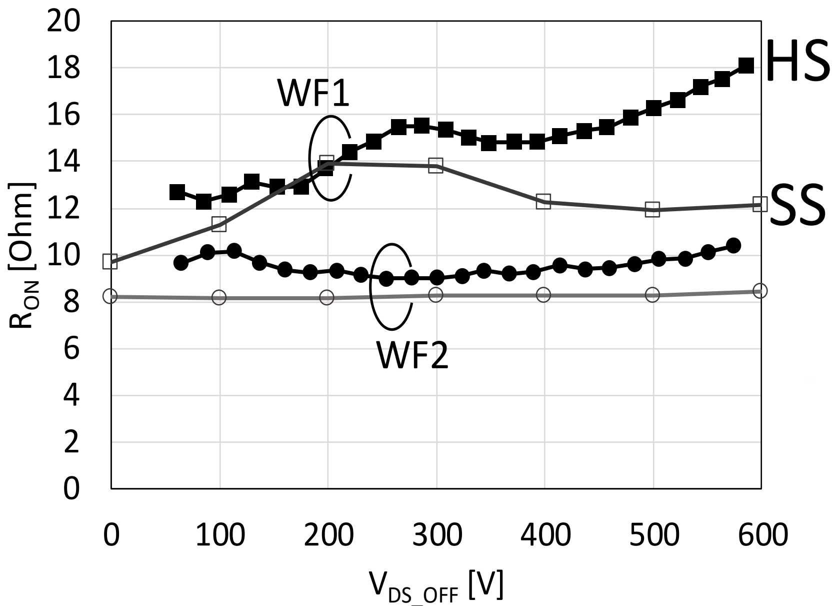
Turn-on waveforms

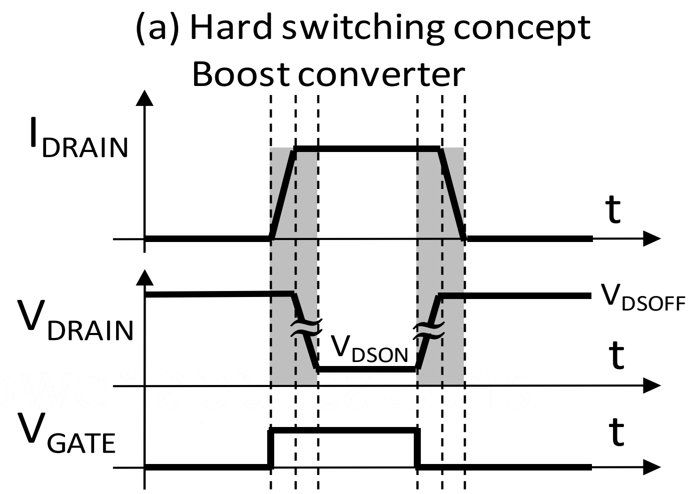




- I_{DS} starts increasing well before V_{DS} drops to zero → hard switching transitions are much longer (few 100 ns) than real power converters (few ns) to evaluate worst case scenarios
- During the turn-on transitions, high current levels (200 mA/mm) are reached with voltages around 500 V

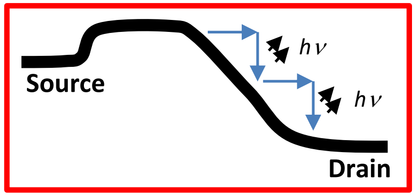
HARD SWITCHING AND SEMI-ON STATE

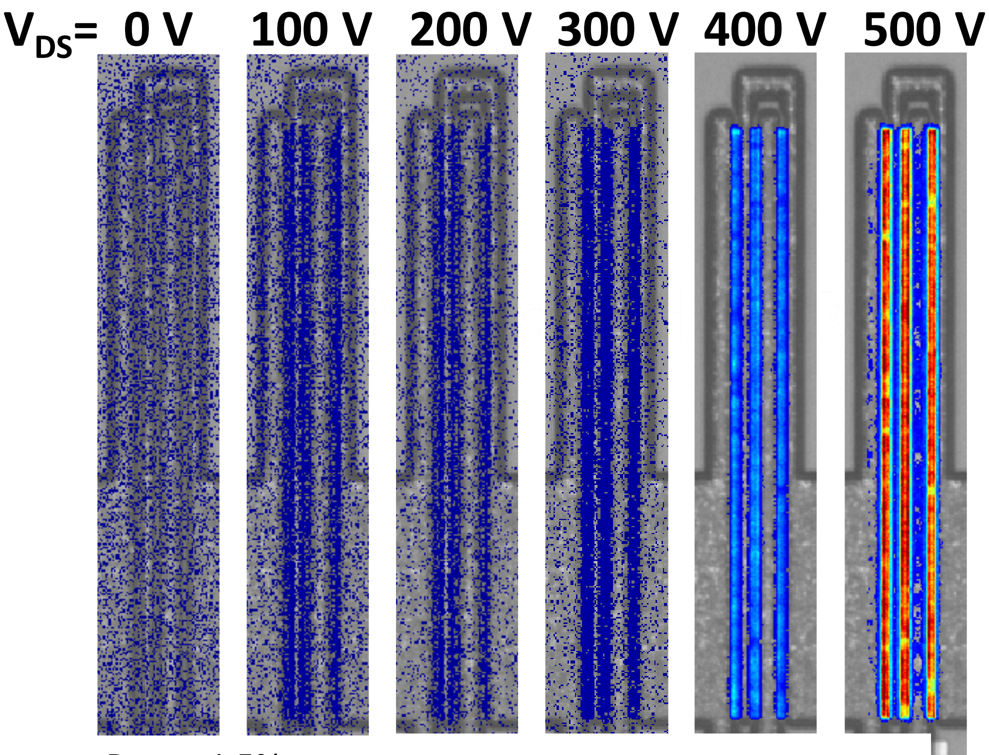


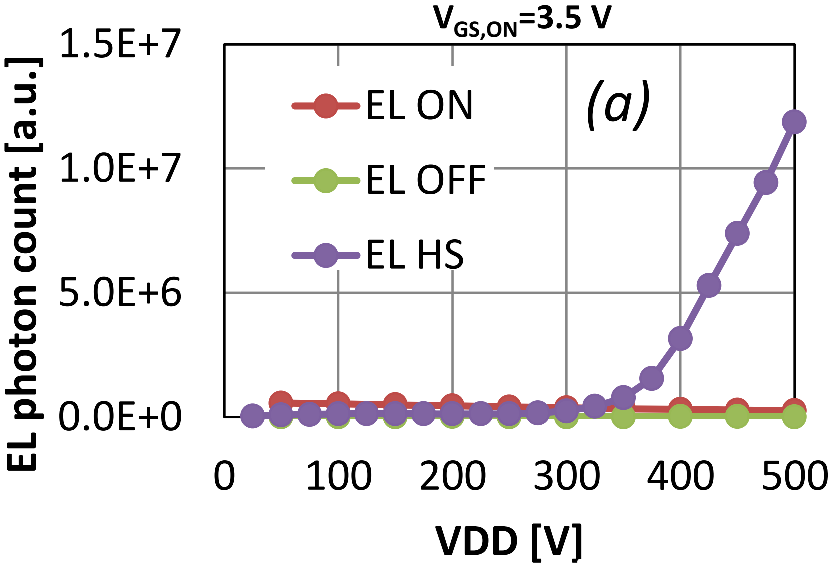


- Dynamic-Ron can be measured directly in a boost converter (on-wafer)
- Comparison between hard-switching and soft-switching, evaluation of hot-electron effects

Increased R_{on} due to hot-electrons

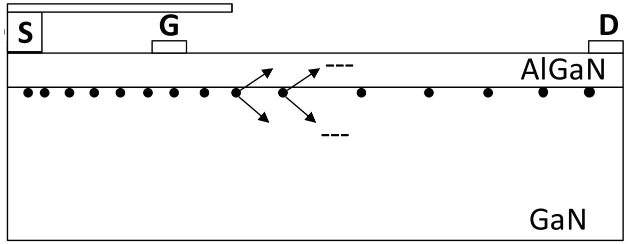






Duty = 1.5%
T_{period} = 10us

EL measured on-wafer, under hard switching

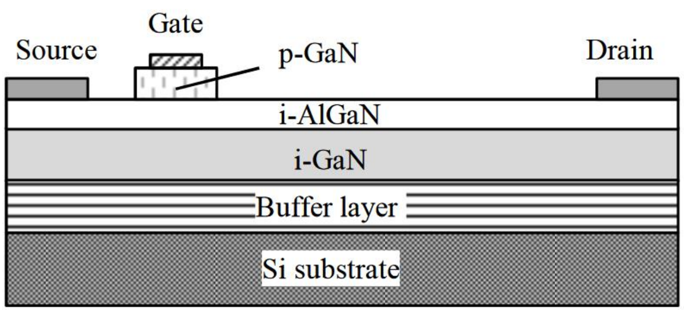


Impact of semi-on stress on the dynamic performance

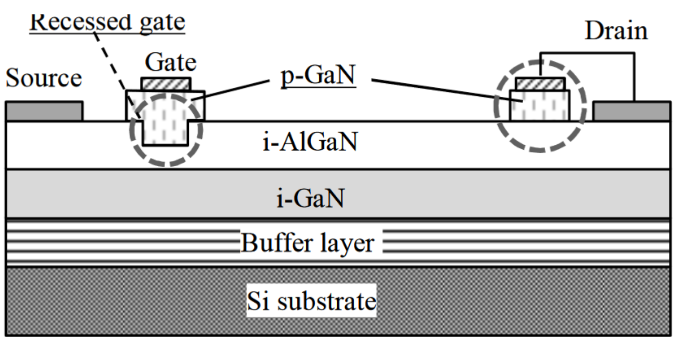
- We investigated hot electron effects on GITs → Normally-off devices with p-GaN gate

- We also analyzed Hybrid-Drain embedded GIT (HD-GIT) → p-GaN region electrically connected to the drain terminal, to reduce trapping processes

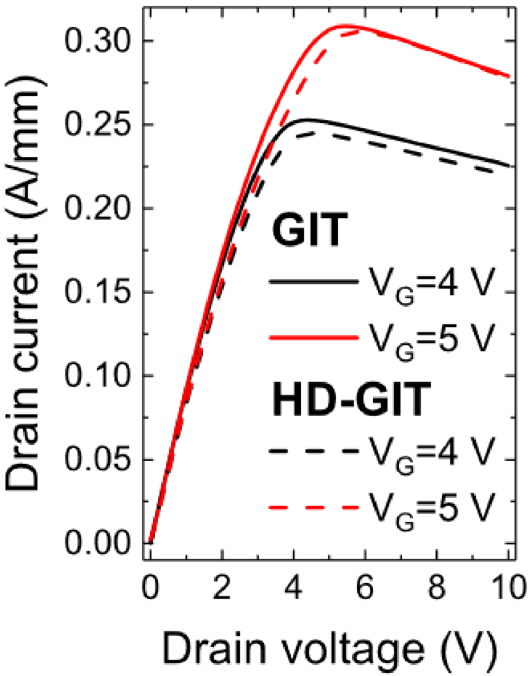
GIT

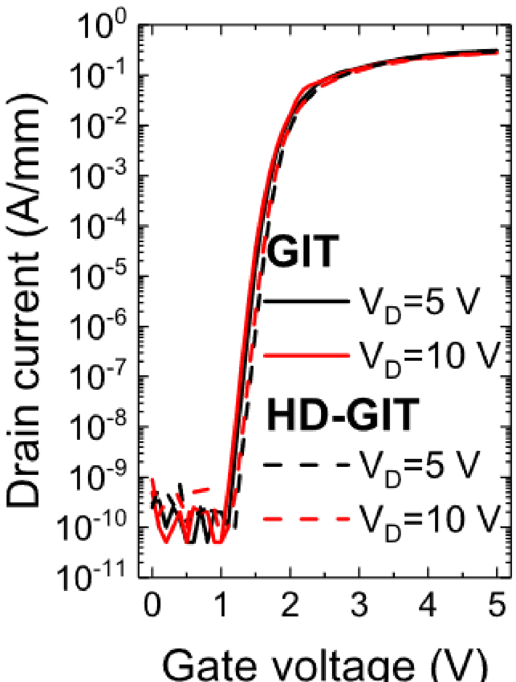


HD-GIT

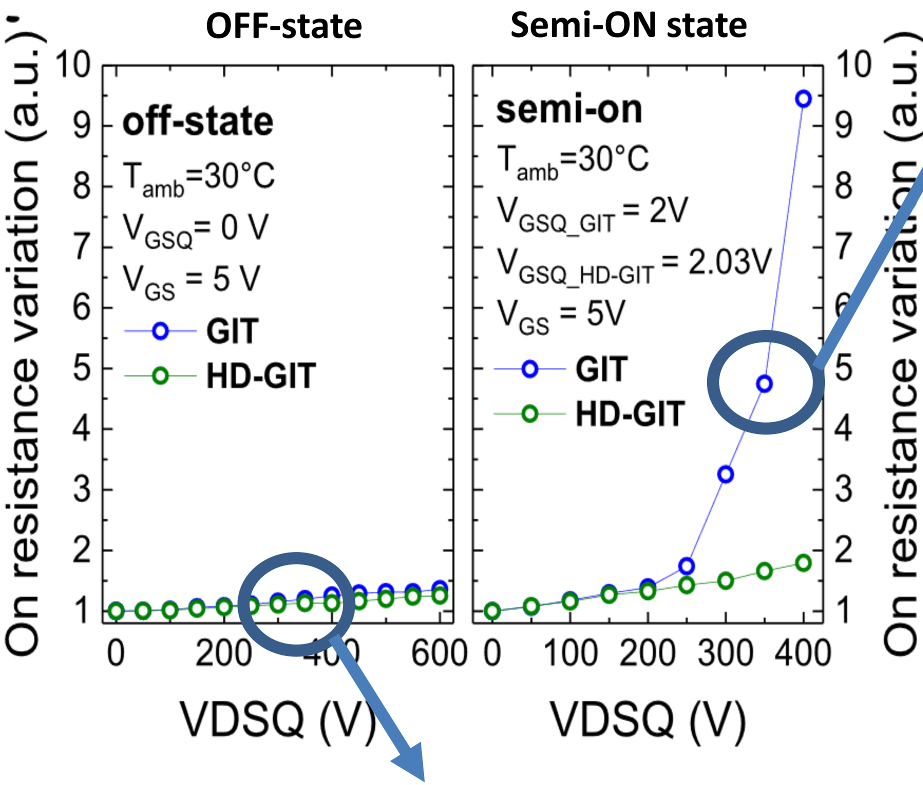


Kaneko, ISPSD 2015

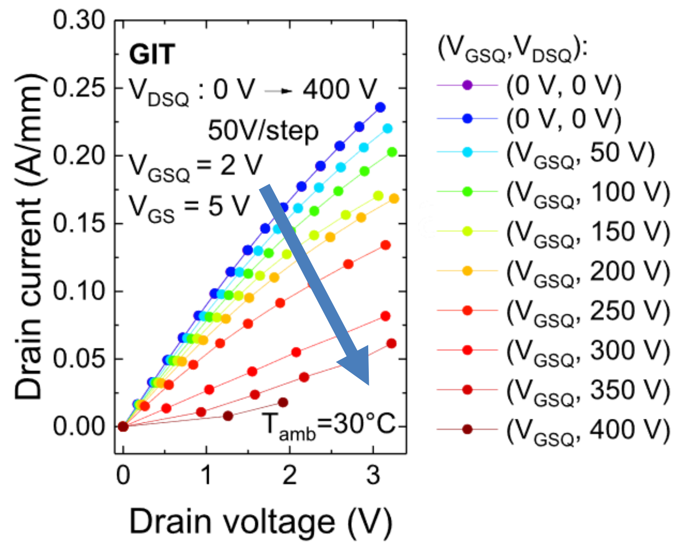




GITs and HD-GITs: dynamic Ron in off-state and semi-on state



In semi-on conditions, GITs show a significant trapping, while HD-GITs are stable

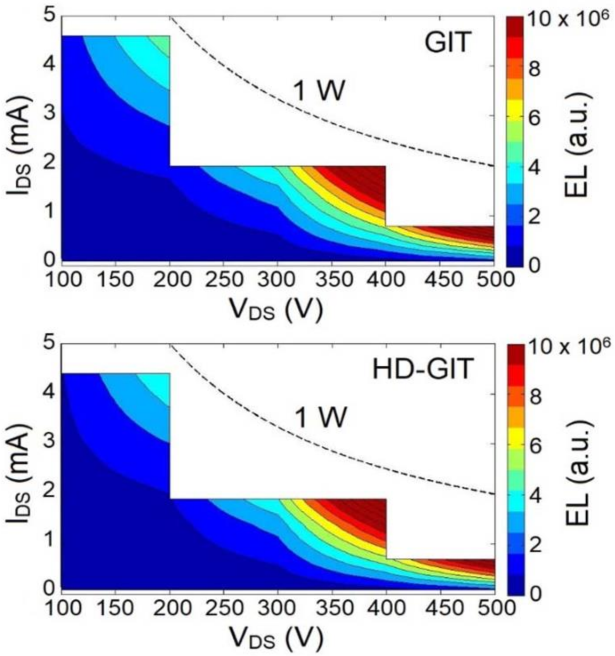


Negligible dynamic Ron in off-state conditions for both GITs and HD-GITs (good epitaxy); GIT has slightly higher Ron, consistent with **Tanaka APL 107, 163502**

What is the origin of this difference?

Fabris, IEEE TED 66, 337 (2019)

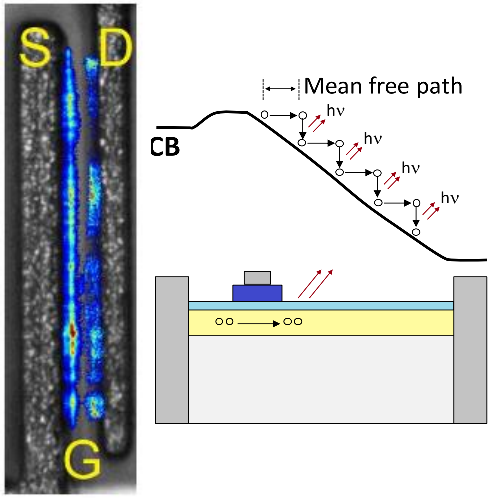
EL measurements: role of hot-electrons

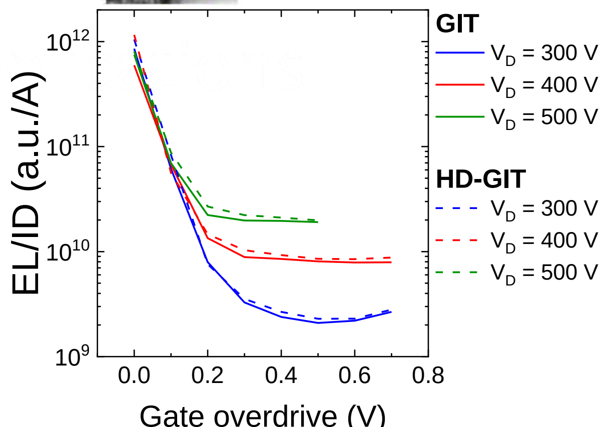


In semi-on conditions, a weak luminescence signal is emitted by the devices

- EL intensity gives an indication on the amount/energy of hot electrons
- EL is proportional to drain current, and dependent on the electric field

$$EL \propto I_D \cdot f(E)$$



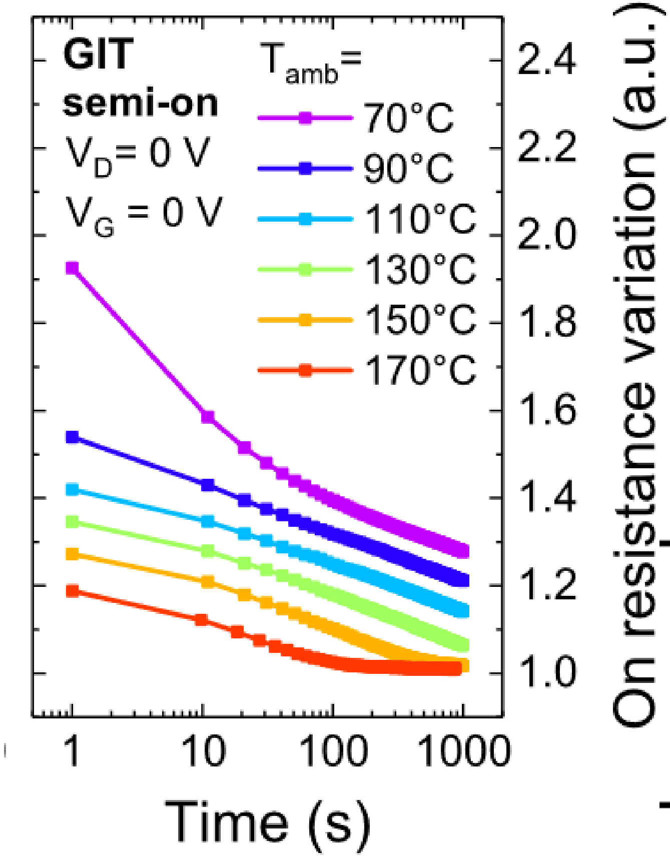


GITs and HD-GITs have the same EL intensity; also EL/ID is identical
→ Same number/energy of hot-electrons

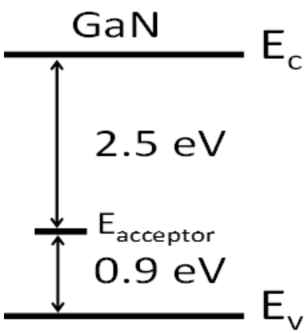
In semi-on state, the **electron trapping rate is identical** in GITs and HD-GITs

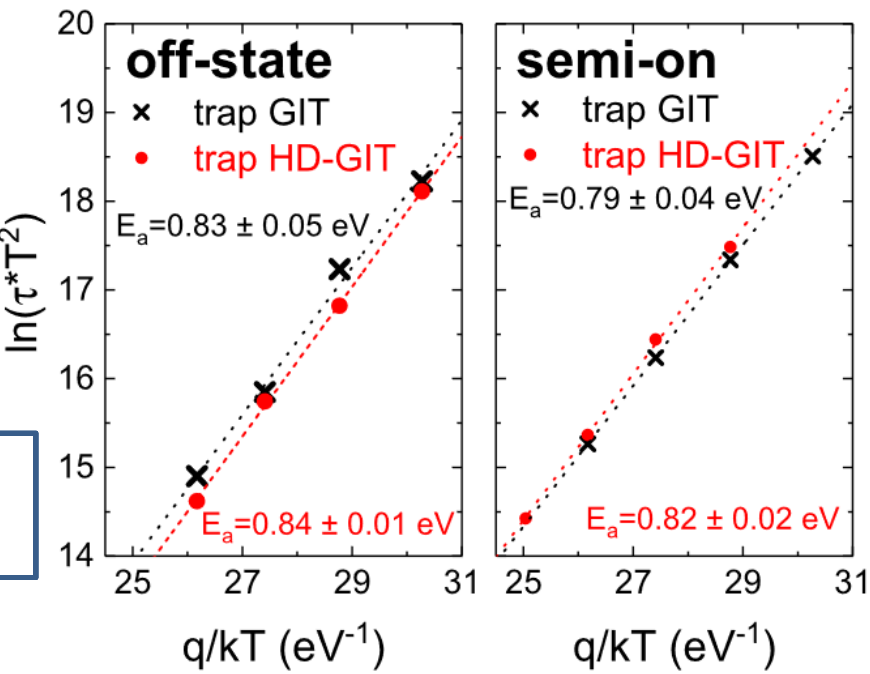
Fabris, IEEE TED 66, 337 (2019)

Do we have different traps in GITs and HD-GITs?



On-resistance transients were measured after trapping in semi-on conditions, to see if GITs and HD-GITs have different traps



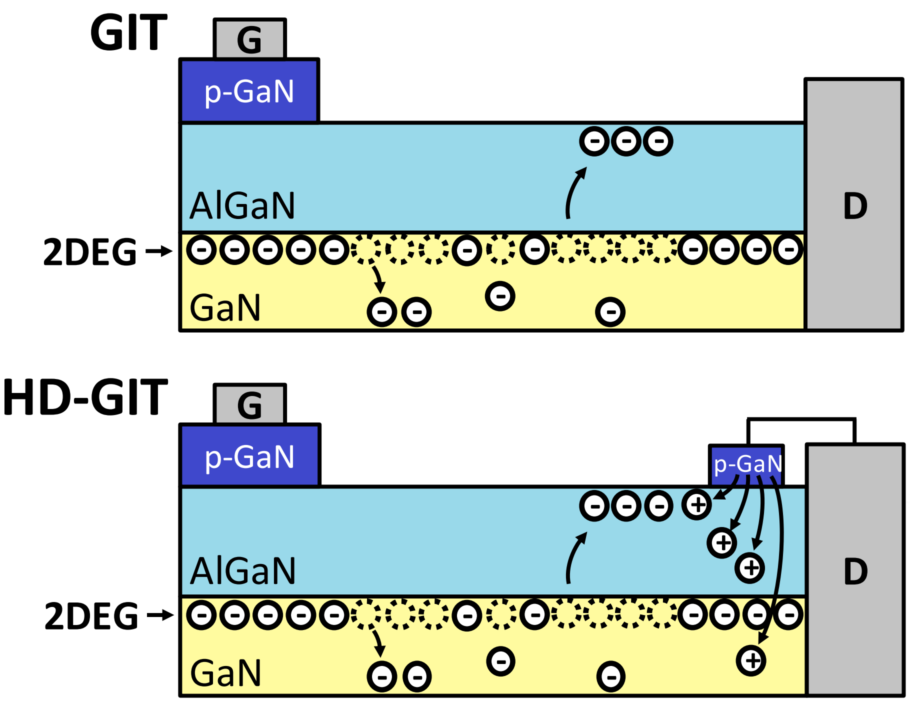


The same trap is filled in both devices

→ Ea≈0.8 eV, C_N defects

Fabris, IEEE TED 66, 337 (2019)

How to explain the difference between GITs and HD-GITs?

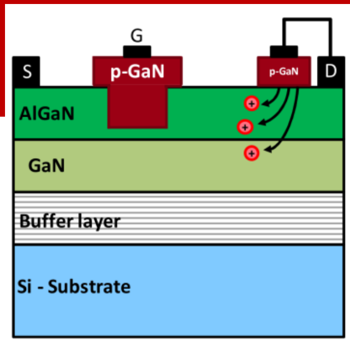


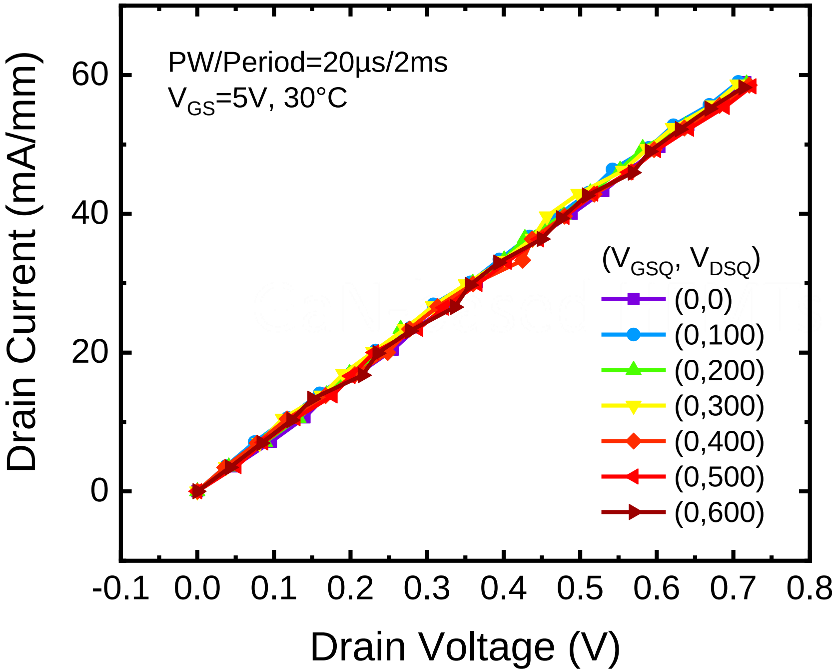
- In both GITs and HD-GITs, **hot-electron trapping is present with similar rates**
- **In both cases, the dominant trap is C_N** (0.8 eV)
- In HD-GITs, when the drain bias is high, **holes can be injected** from the pdrain towards the AlGaN/GaN heterostructure

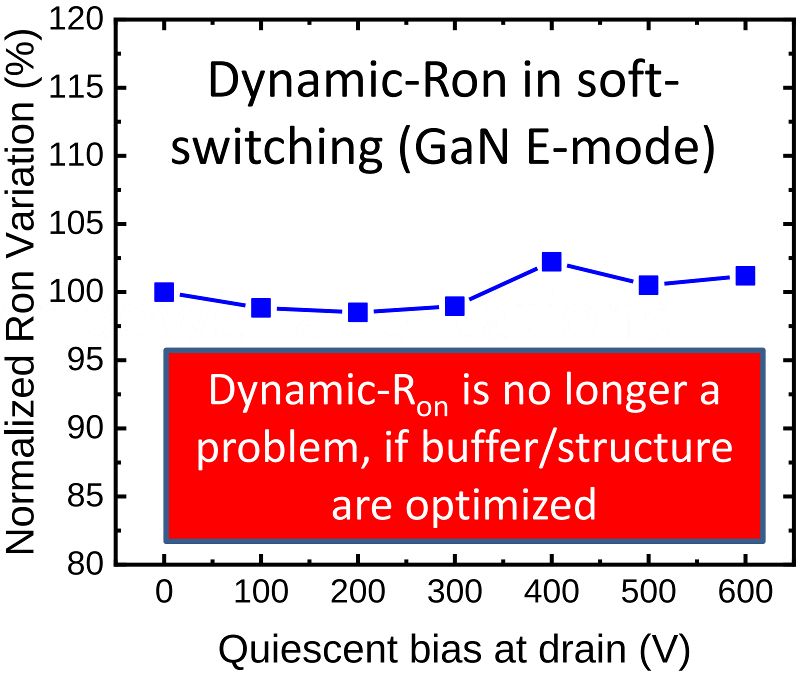
Such holes can neutralize the trapped electrons

In this view, GITs and HD-GITs have **the same electron trapping rate**,
but **different de-trapping rates**, thanks to hole injection

Stability and reliability in soft switching







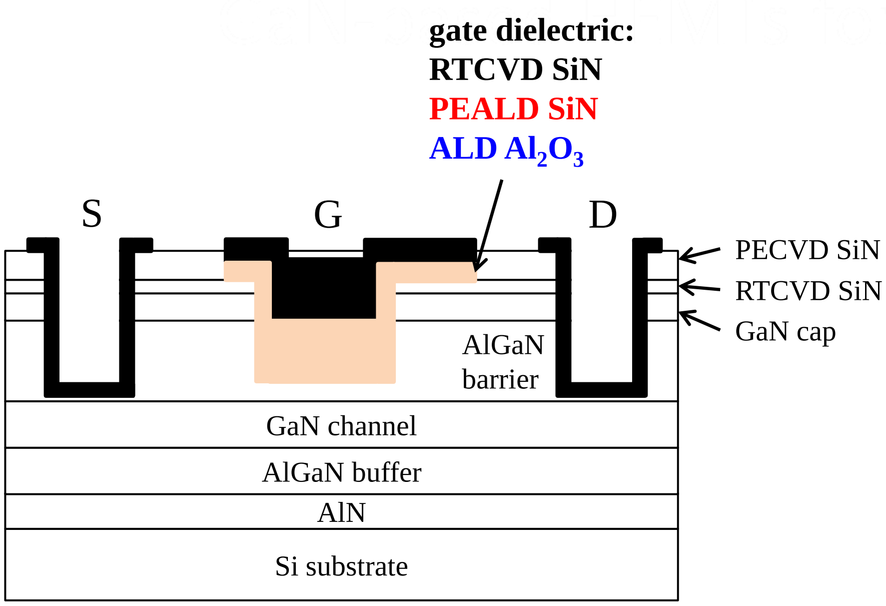
Kaneko, ISPSD 2015

Reference samples show zero dynamic-Ron up to V_{DS}=600 V in soft-switching

Does dynamic-Ron become an issue in hard switching?
How to characterize this effect?

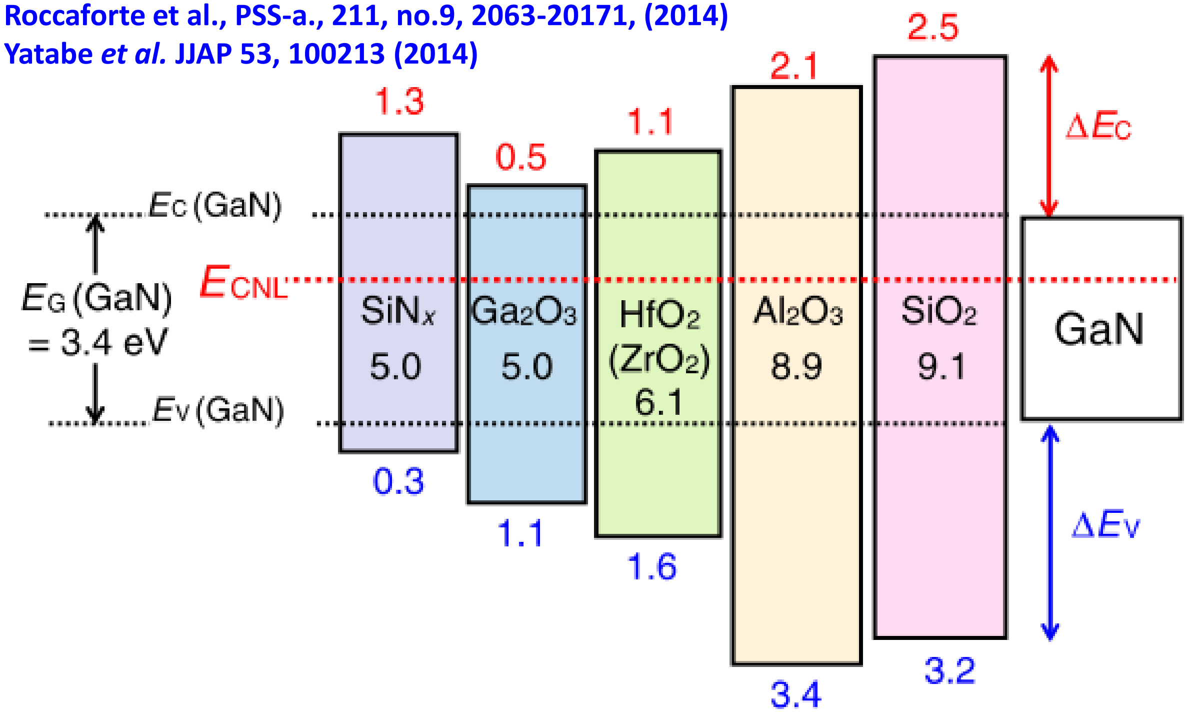
Need an isolated Gate to minimize gate leakage current.

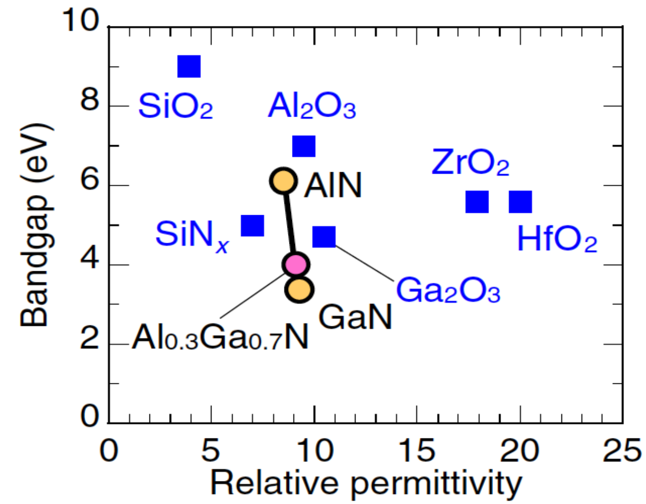
GaN-MIS HEMTs: Degradation at positive gate bias



Different gate insulators for GaN-based MIS-HEMTs

Roccaforte et al., Appl. Surface Sci., 301, 9-18 (2014)
Roccaforte et al., PSS-a., 211, no.9, 2063-20171, (2014)
Yatabe *et al.* JJAP 53, 100213 (2014)

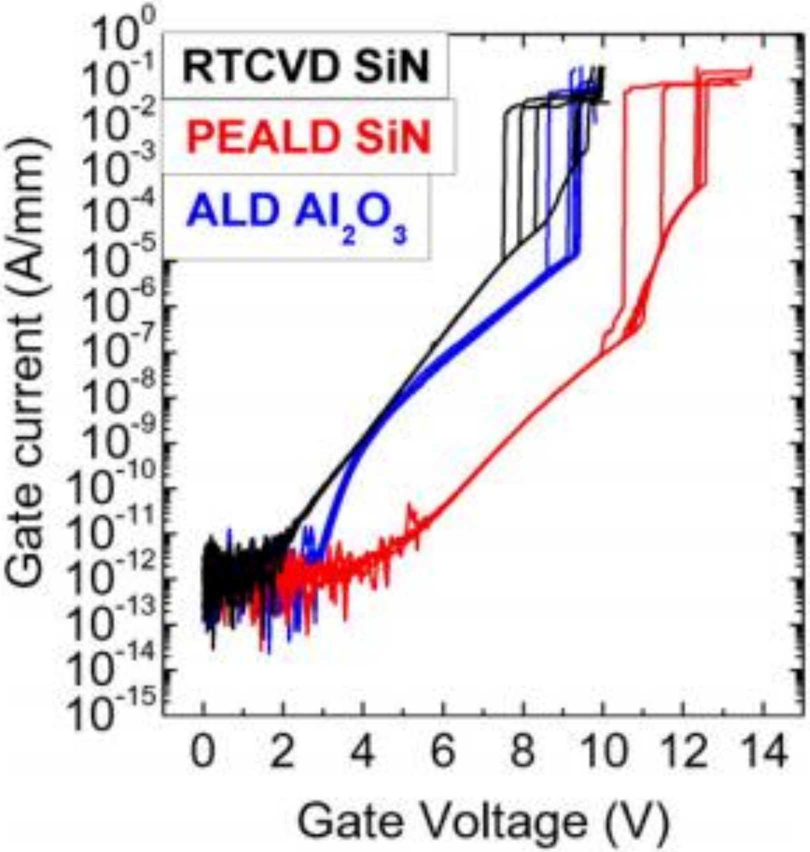




Large band-offset energy is required at the insulator/ AlGaN interface for the suppression of leakage current.

- MIS gate structures employing Ga_2O_3, ZrO_2, and HfO_2 dielectric materials are relatively susceptible to leakage current problems

Different gate insulators for GaN-based MIS-HEMTs



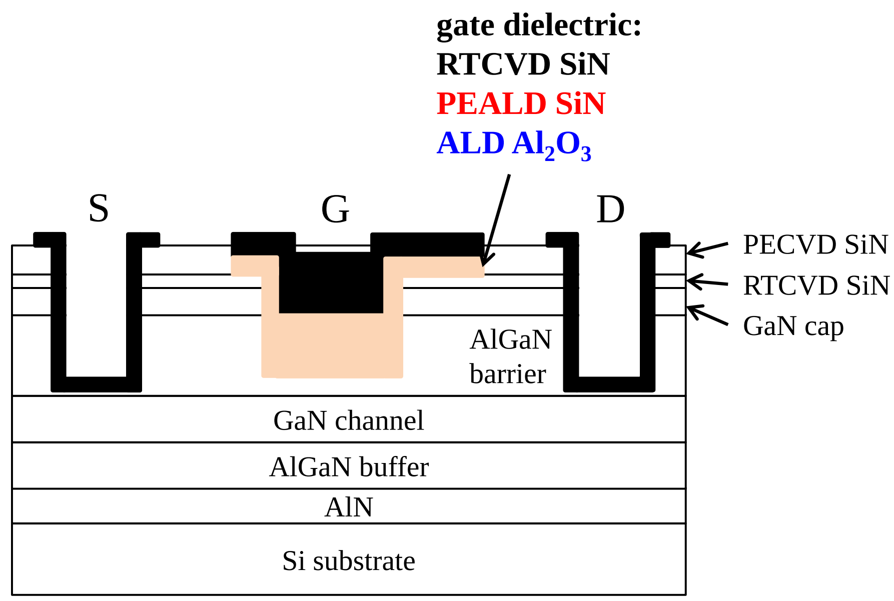
	$I_{G,leak}$ at V_G = 5V (A/mm)	V_{BD} (V)
ALD Al_2O_3	$1.1 \cdot 10^{-8}$	9.3
RTCVD SiN	$1.8 \cdot 10^{-8}$	8.7
PEALD SiN	$5.3 \cdot 10^{-12}$	11.9

Tian-Li Wu et al., IEEE IRPS 2015 6C.4.1

Three different gate insulators were used:

- 15 nm SiN layer deposited by rapid thermal chemical vapor deposition (RTCVD)
- 15 nm SiN layer deposited by plasma enhanced atomic layer deposition (PEALD)
- 15 nm Al_2O_3 layer deposited by atomic layer deposition (ALD)

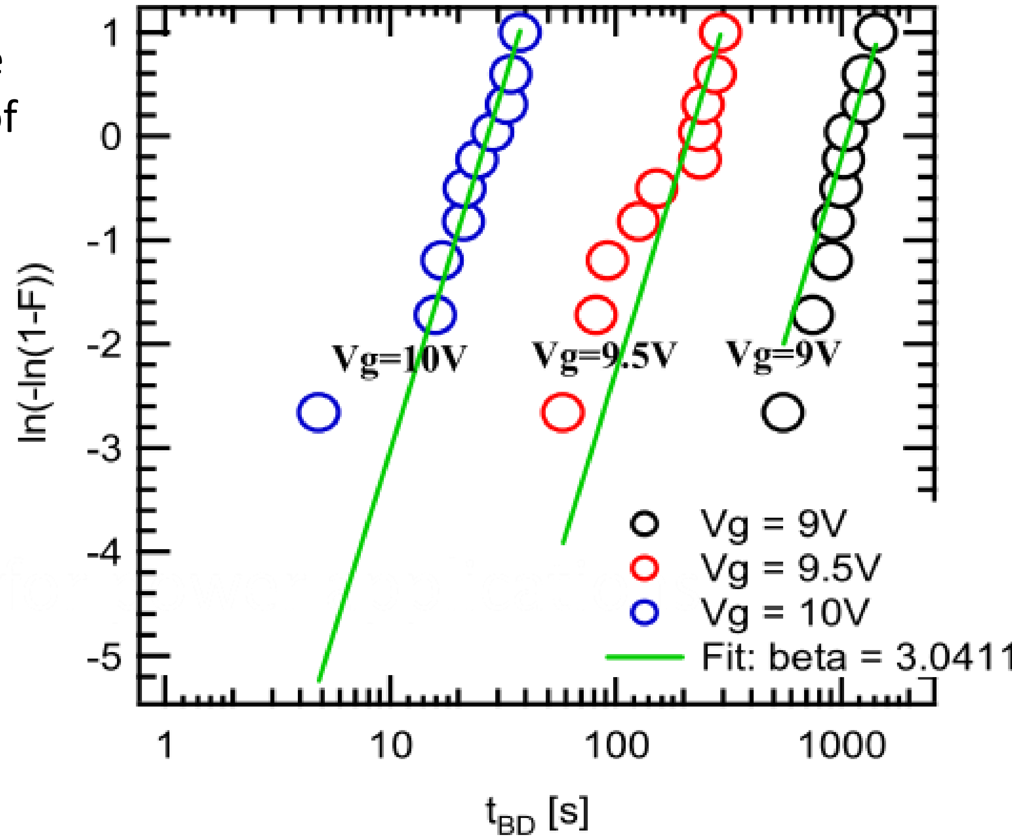
«Reliability and parasitic issues in GaN-based power HEMTs», SST, in press

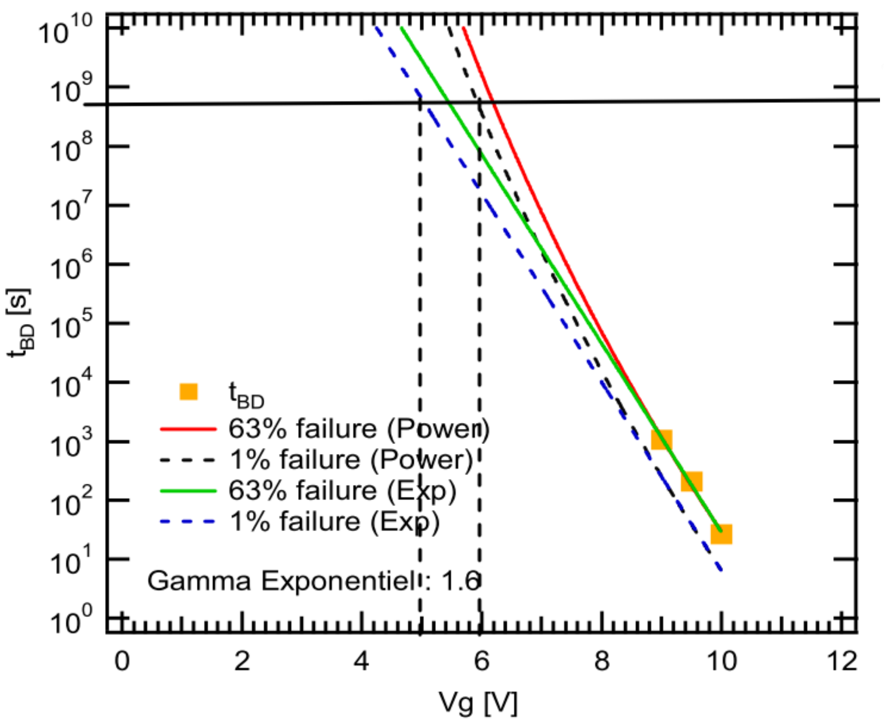


Time-dependent dielectric breakdown (Forward voltage)

Similar to the TDDB evaluation in CMOS gate dielectrics, the time-to-breakdown (t BD) of MIS-HEMT is Weibull distributed

By fitting with a Weibull distribution, a large β = 3 is obtained→ tight breakdown distribution and small variability



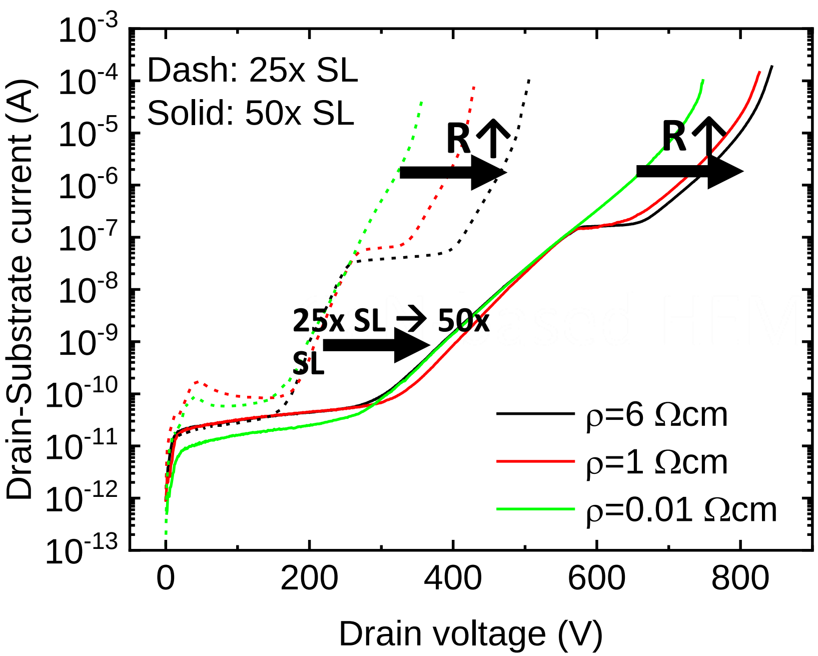


Lifetime extrapolation to 1% of failures (power law fitting for VG=5-6 V) → Excellent breakdown voltage strength and the 20-year lifetime of the dielectric at 200°C.

Source: Wu et al., IRPS 2013

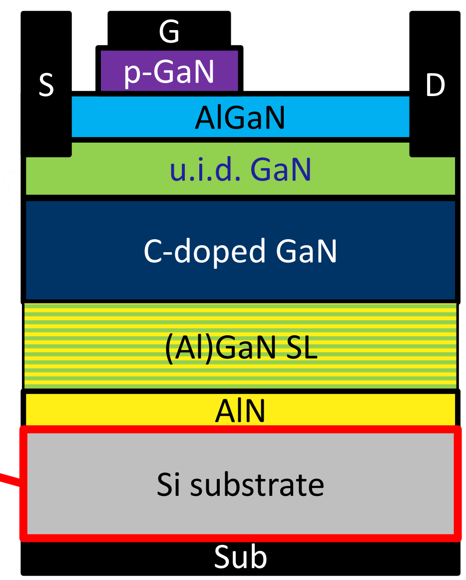
Understanding vertical conduction → p- substrates

- Role of injection and bulk on vertical leakage?
- How to improve vertical breakdown voltage (BV)?



Enhancement-mode device: use p-GaN layer to raise conduction band and obtain $V_{TH} > 0$ V

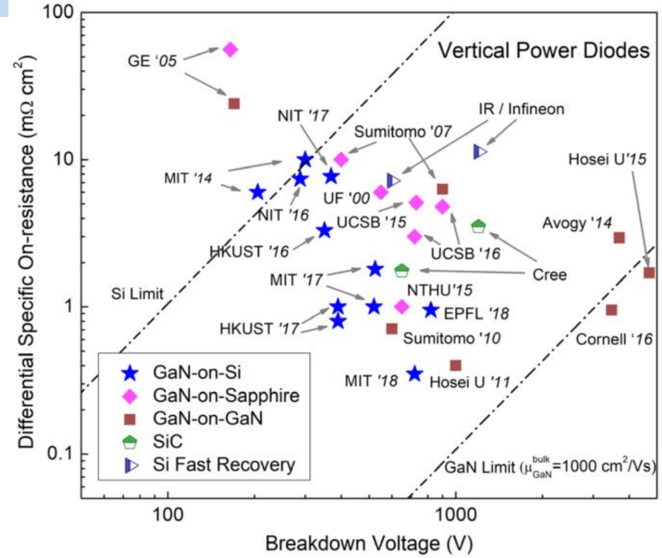
Resistivity:
- ρ = 0.01Ωcm
- ρ = 1Ωcm
- ρ = 6Ωcm



- Highly resistive substrates create a plateau in the vertical I-V plots
- Increase in breakdown voltage with semi-insulating substrates
- Further improvement obtained by increasing the SL thickness

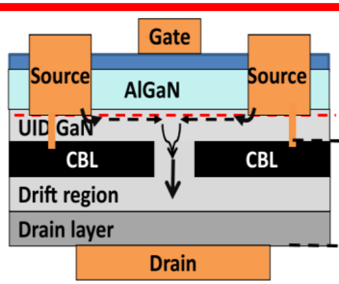
GaN reliability – Future challenges (vertical devices)

- The competition with Si/SiC is becoming stronger
- GaN vertical devices can target the 1-10 kV range, with low R_{on} and parasitic capacitance
- GaN lateral: sensitive to surface trapping, BDV scales with cost, lower current density

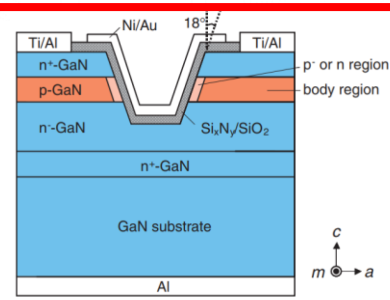


J. Phys. D: Appl. Phys. 51(2018) 273001

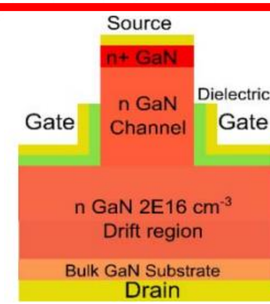
Over the last couple of years, we've evaluated/tested different structures:



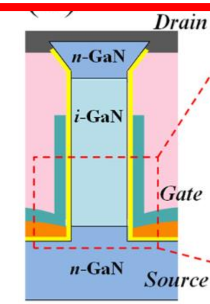
Semicond. Sci. Technol. 28 (2013) 074014
(not tested in our labs)



Appl. Phys. Express 1 (2008) 011105



Sun, DRC 2016



Yu, APL 2016

All of these structures have potential advantages and drawbacks, in terms of reliability → **Not problems, but research opportunities!**

GaN-HEMTs: failures related to the dielectrics

Conclusions – power GaN HEMT

- With gallium nitride you never get bored
- Reliability issues are being continuosly discovered and solved
- Some examples were described today…

- We started from extrinsic reliability (dielectric-related)…
- …and discovered that GaN itself shows TDDB → Polar nature
- Resistive substrates as a way to increase breakdown voltage → Trade-off with trapping

- Dynamic-R_{on} is no longer a problem, if buffer/structure are optimized
- Hard switching can promote hot-electron trapping
- This was investigated by a novel wafer-level setup → EL confirms role of hot electrons

- Future challenges are on vertical devices → Enabling a wider adoption of GaN for HV applicatons (>1 kV) → Work in progress!

Despite the ever increasing understanding → We are still scratching the surface!

http://www.alinwon-fp7.eu/fp7/

http://www.hiposwitch.eu/

http://www.inrel-npower.eu/

http://www.powerbase-project.eu/

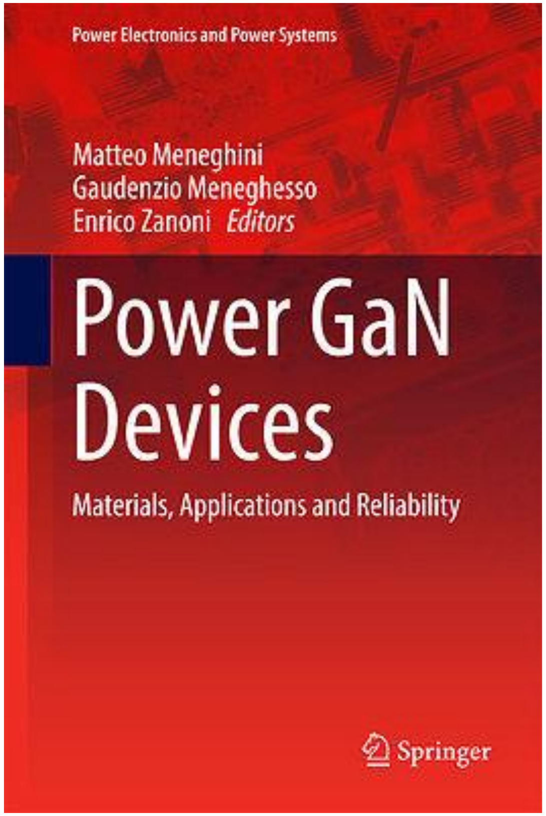
http://www.e2cogan.eu/

ONR project N000141010608,
monitor: Paul Maki

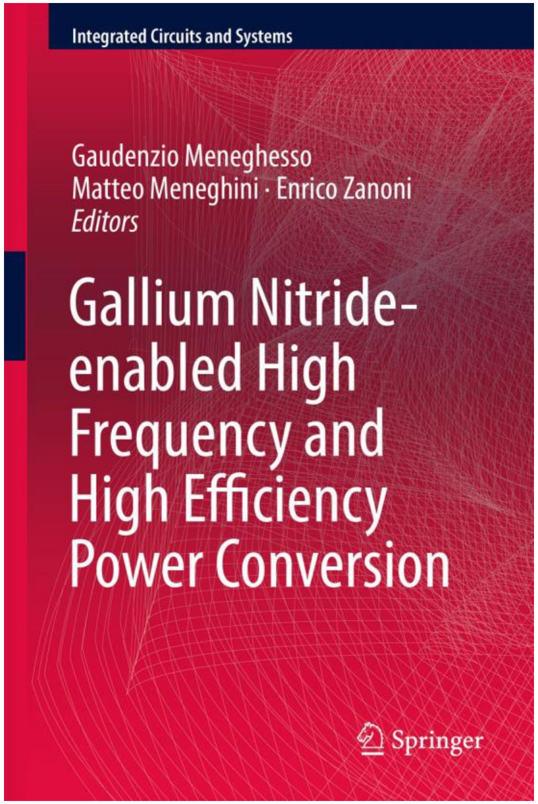
EDA projects
MANGA
EuGANICC

https://www.eda.europa.eu

Recent Books on GaN



M. Meneghini, G. Meneghesso, E. Zanoni (Eds.)
Power GaN Devices Materials, Applications and Reliability
Series: Power Electronics and Power Systems
Springer 2016. ISBN: 978-3-319-43197-0
http://www.springer.com/gp/book/9783319431970



G. Meneghesso, M. Meneghini, E. Zanoni (Eds.)
Gallium Nitride-enabled High Frequency and High Efficiency Power Conversion
Series: Integrated Circuits and Systems
Springer 2018: ISBN 978-3-319-77993-5
https://www.springer.com/it/book/9783319779935

Conclusions

- GaN-based devices are excellent devices for future RF and power applications
- GaN-power devices → almost ideal performance, but…
- The main issues are trapping (current collapse, dynamic Ron) and degradation → Strongly dependent on both epitaxial quality and processing
- We reviewed the trapping mechanisms, and the methods for evaluating parasitics in GaN HEMTs (database for defects in GaN)
- Degradation strongly depends on bias conditions: we reviewed off-state degradation, FW gate stress, and breakdown mechanisms → High reliability is possible only through optimized epitaxy and process (field plates, defects, …)
- Further suggested readings in the next slides…