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Semiconductor Power Devices :

Part 1 : From Junction to Material Engineering Part 2 : Reliability Basics

Peter Moens



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Semiconductor Power Devices : Part 1 : From Junction to Material Engineering

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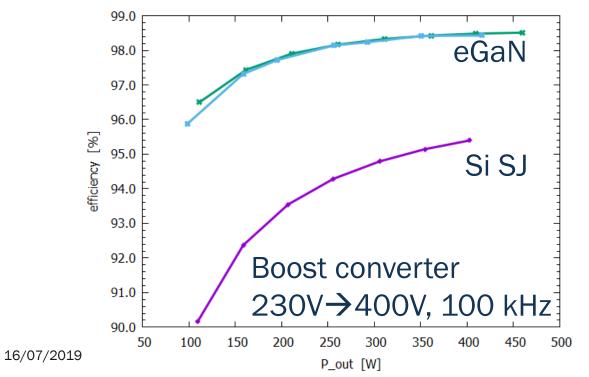


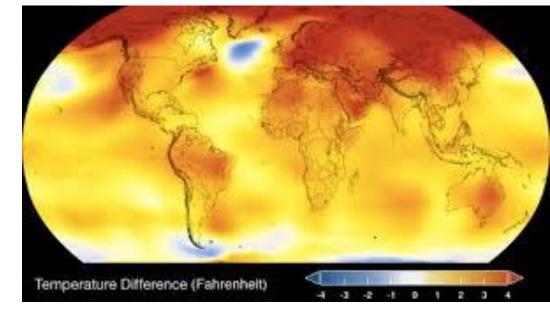
Global Challenges : Global Warming

- 50% of all energy in the world is electrical (~8 TW.yr out of ~18 TW.yr)
- 40-60% of all produced electricity is lost, mainly due to the many transmission and conversion steps (HV to LV, AC to DC etc.) →~4TW.yr is lost !
- E.g 4 conversion steps :

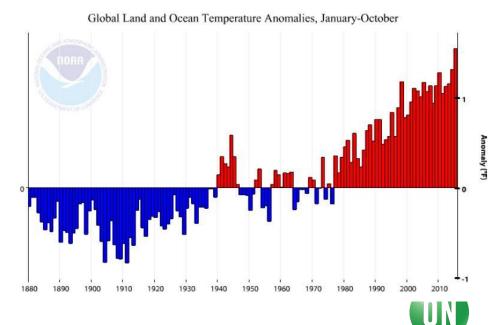
3

- Si : 95% of each step : total eff. ~81%
- GaN: 98% of each step: total eff. ~92%



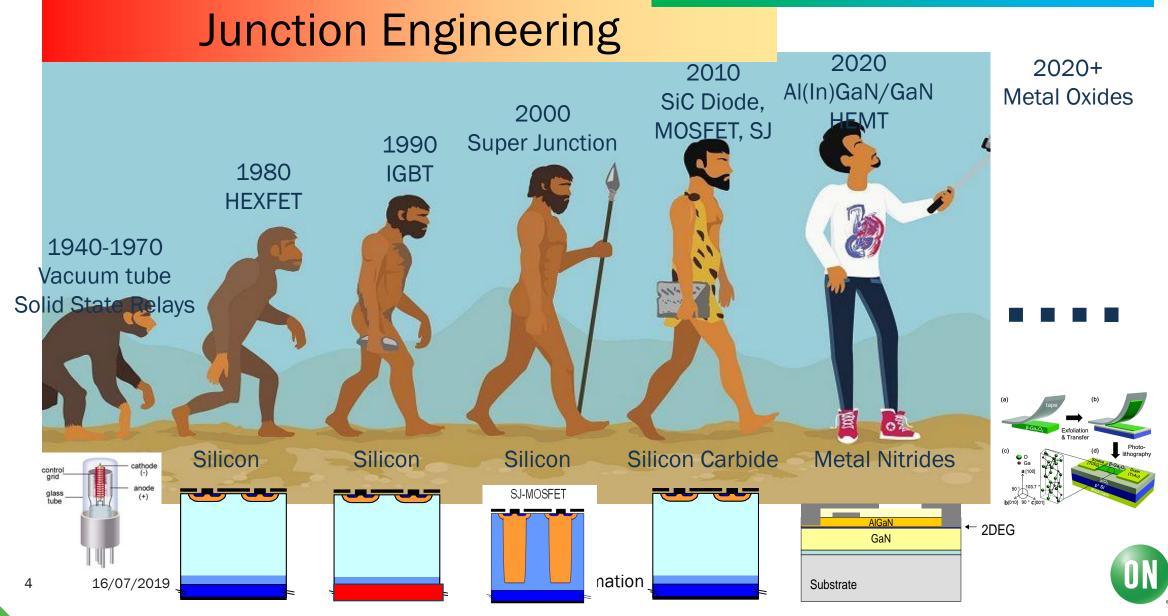


Global Land and Ocean Temperature Departure from 20th Century Average, January-October



The Evolution of Power Devices

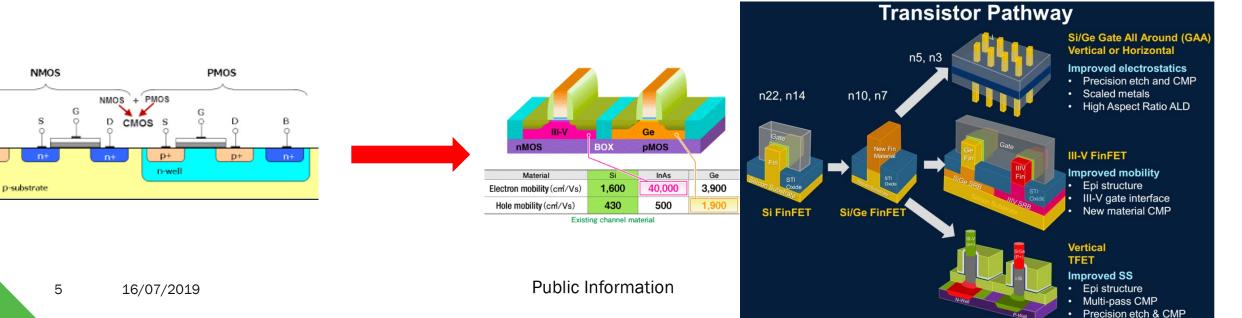
Materials Engineering



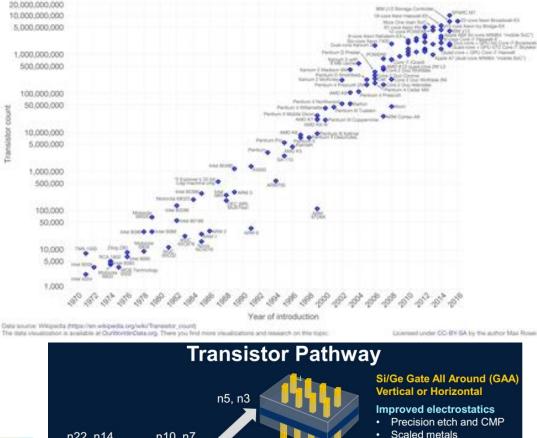
The Evolution of Logic Devices

Moore's law driven by scaling.

- Up to 10nm node "junction engineering"
 - Si nMOS and pMOS
 - High k gate dielectric and metal gates
- Below 10nm node "material engineering"
 - Ge-based for pMOS
 - III-V based for nMOS



Moore's Law – The number of transistors on integrated circuit chips (1971-2016) Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important as other aspects of technological progress – such as processing speed or the price of electronic products – are strongly linked to Moore's law.



The ideal power semiconductor switch

- Off-state
 - Should block a high voltage, with no leakage current
- On-state
 - Should have no resistance (ideal conductor)
- During switching from off to on (and vice versa)
 - Should happen immediately
 - No hysteresis
 - No charge storage

Enabled by new material properties and novel device concepts which enable new system solutions



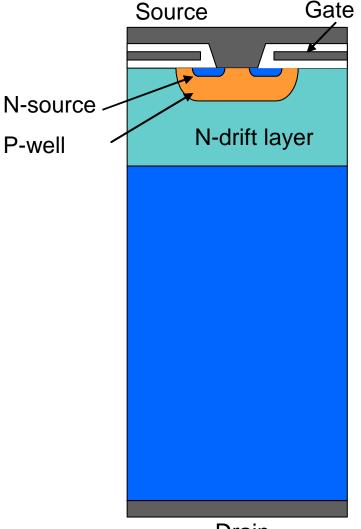
Outline

- Power devices=material properties
 - 1D limit for a vertical transistor
 - Resurf effect (2D)
- Non-polar and polar materials
 - Concept of polarization charge
 - Simple band structure
- HEMT "High Electron Mobility Transistor"
 - HEMT versus vertical power device
- Ron and Capacitance versus Voltage
- Cost and performance



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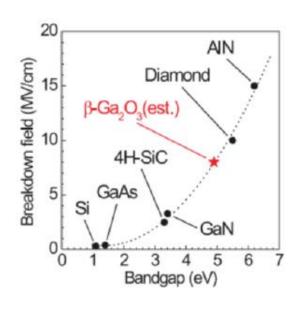


The Baliga Figure of Merit—1D

Baliga Figure-of-Merit is a metric for how good a material is for <u>uni-polar</u> power device technology.

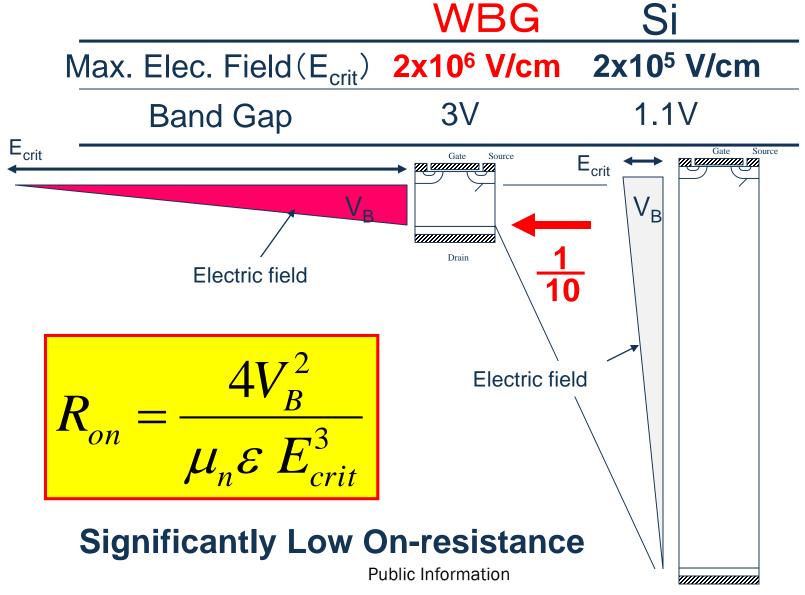
• [note : Ec and mobility are assumed constant (independent of doping) !]

$$Ron \left[\Omega. cm^{2}\right] = \frac{4. V_{bd}^{2}}{\varepsilon. \mu. E_{c}^{3}}$$



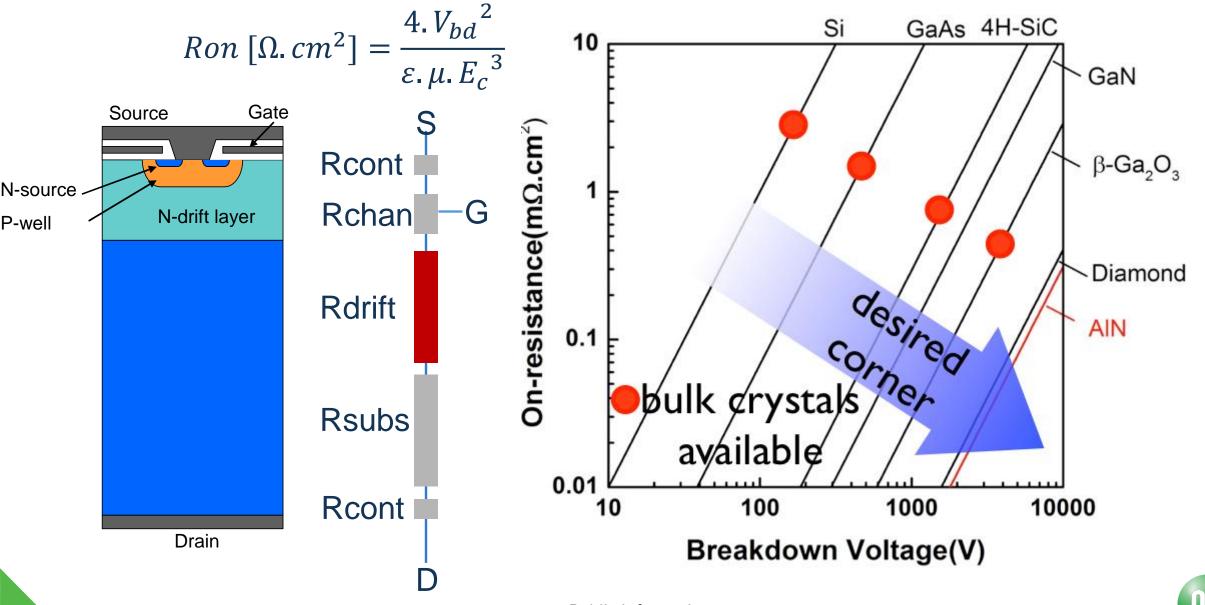
			WE	3G	U-WBG				
Baliga's FOM $\epsilon \mu E_b^3$	1	15	340	870	24664	3444	32158		
Relative dielectric constant ε	11.8	12.9	9.7	9.0	5.5	10	8.5		
Breakdown field E_b (MV/cm)	0.3	0.4	2.5	3.3	10	8	15		
Bandgap Eg (eV) Electron mobility μ (cm ² /Vs)	1.1 1400	1.4 8000	3.3 1000	3.4 1200	5.5 2000	4.8-4.9 300	6 500		
	Si	GaAs	4H-SiC	GaN	Diamond	β-Ga ₂ O ₃	AlN		

Wide Band Gap Semiconductor Advantage



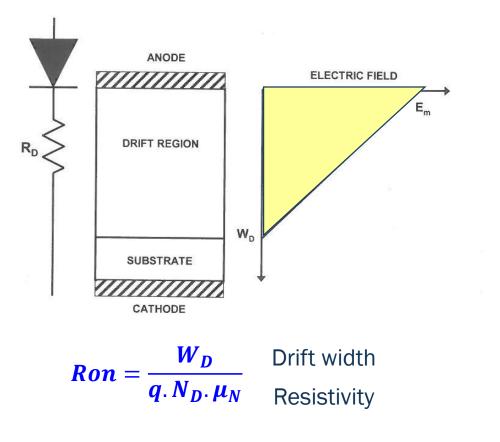


Baliga FOM—only for drift region (1D)



Basic Equation for Power Semiconductors

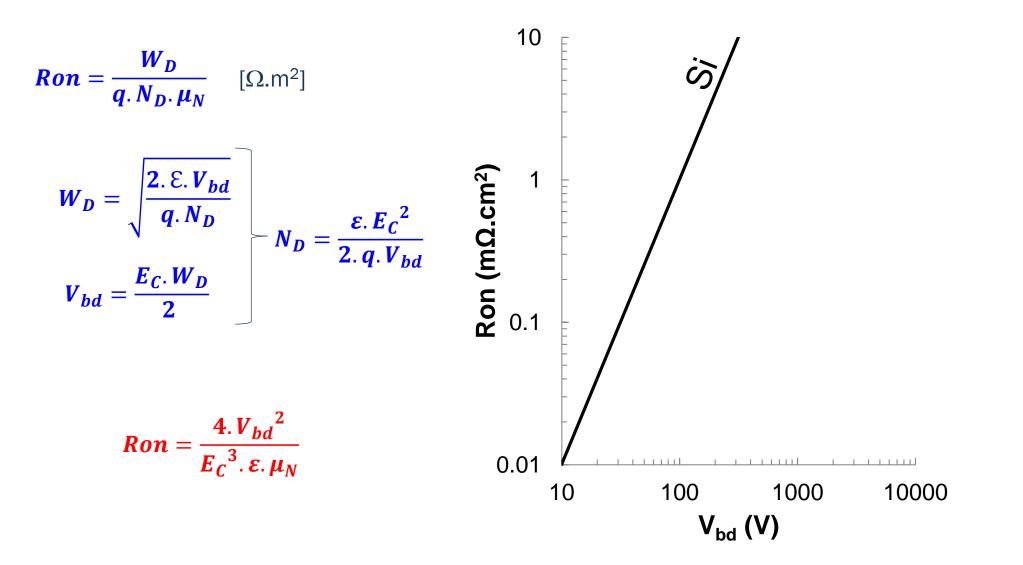
Assume an abrupt junction, parallel plane



$$\frac{\partial^2 V}{\partial x^2} = -\frac{\partial E}{\partial x} = \frac{-q \cdot N_D}{\varepsilon}$$
$$E(x) = \frac{-q \cdot N_D}{\varepsilon} \cdot (W_D - x)$$
$$V(x) = \frac{q \cdot N_D}{\varepsilon} \cdot (W_D \cdot x - \frac{x^2}{2})$$
$$V(W_D) = V_{bd} \qquad V_{bd} = \frac{E_C \cdot W_D}{2}$$
$$W_D = \sqrt{\frac{2 \cdot \varepsilon \cdot V_{bd}}{q \cdot N_D}}$$



Figure-of-merit : Ron versus Vbd





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Super Junction : An Example of Junction Engineering

Public Information



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How to go beyond the Baliga FOM ?

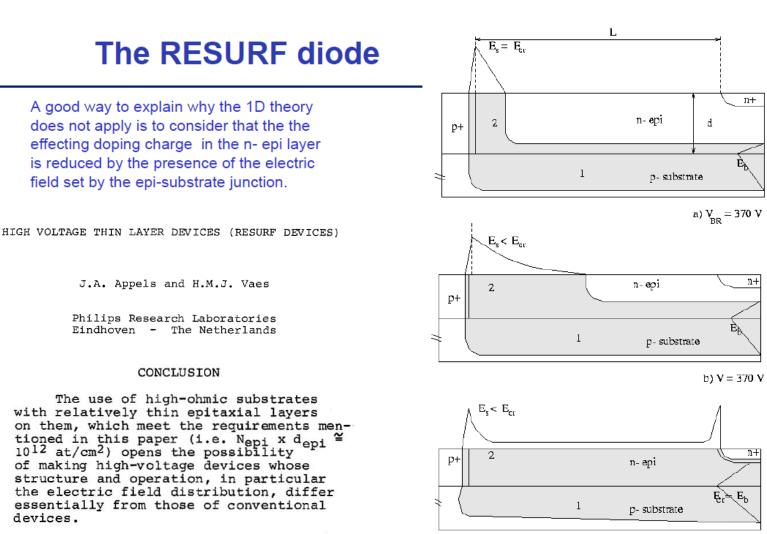
Can we do better than the 1D approximation ?

1. <u>RESURF</u> is a way of shaping the electrical fields in a device in such a way that the breakdown voltage is increased in comparison with the 1D planar junction

2. <u>RESURF</u> is a way of increasing the drift doping in a device (lowering the Ron) without the BVds going down, by shaping the electrical field



Junction Resurf Diode



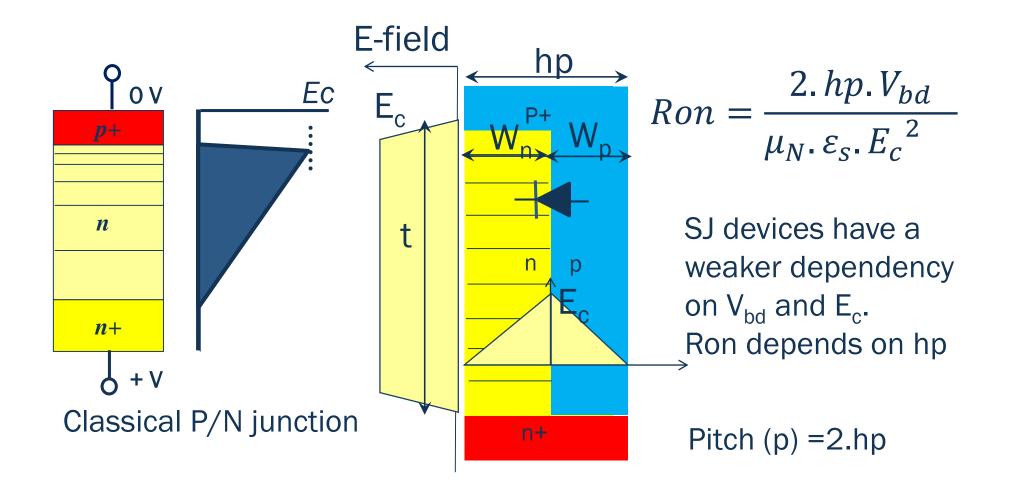
Ref.

1) Late News Paper, ESSDERC '79 München.

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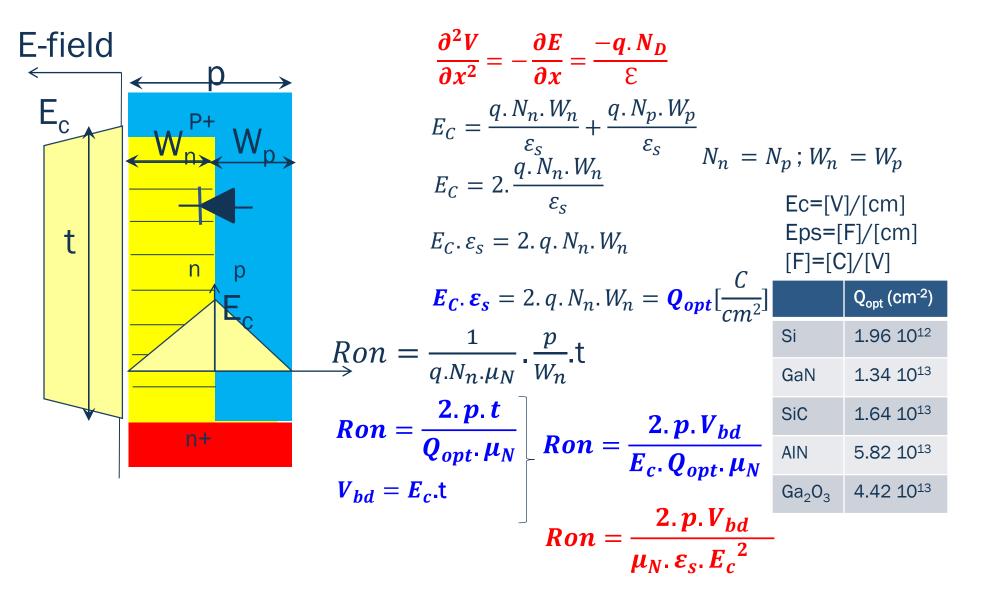
c) $V_{_{\rm RD}} = 1150 \text{ V}$

Junction Resurf Diode





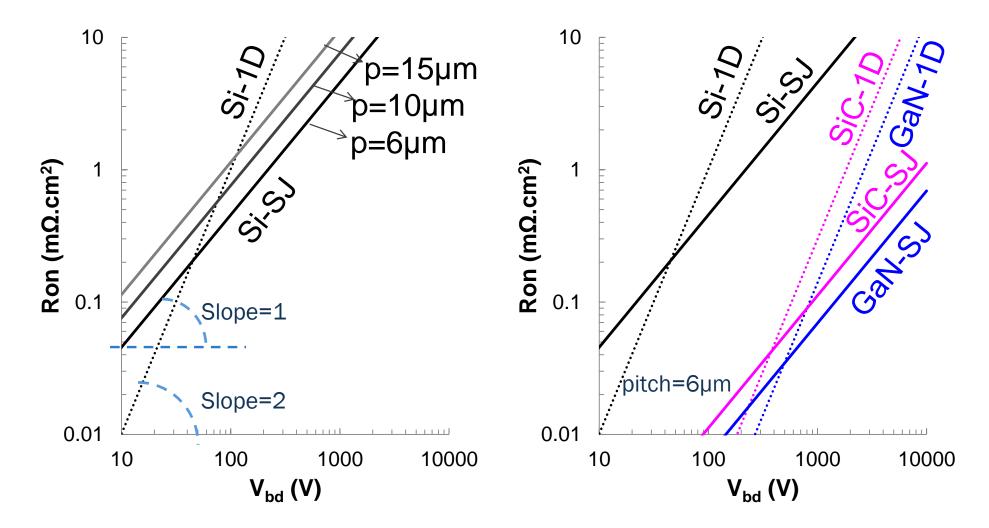
Resurf Limit (2D)–Optimal Charge





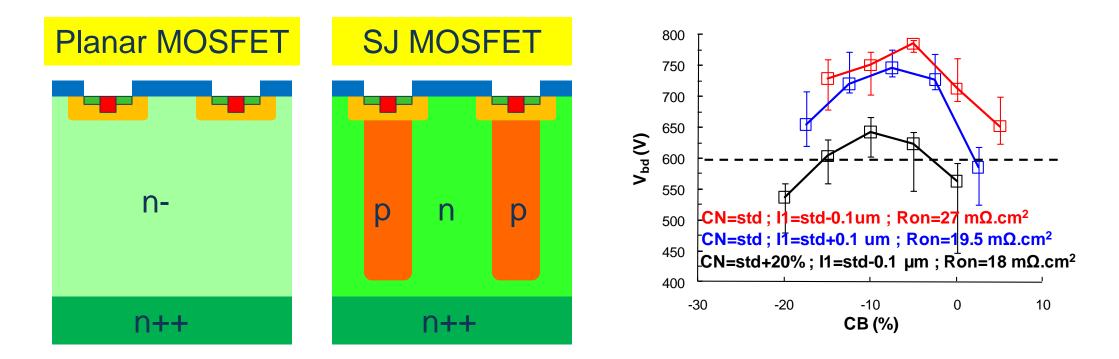
Resurf limit–2D

Depends on device pitch (p) : process capability





Super Junction Transistors (Based on Resurf)



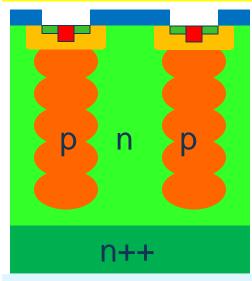
To achieve Resurf Action, the total charge in the n and p columns must be balanced across the total structure !

Tight Process control is key !



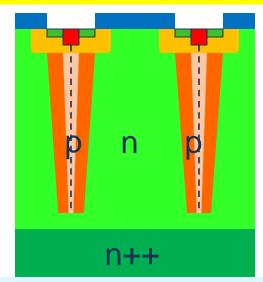
Ways to achieve a vertical SJ structure

Multi-epi multi-implant



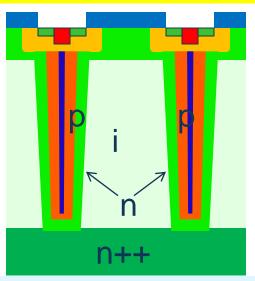
n-epi control ~2-3%
p-type control <1%
Shrinking limited by litho and diffusion, need more epi/implant steps

Deep trench etch single epi refill



Shrinking potential
n-epi control ~2-3%
p-type control ~ 2-3%
Deep trench etch taper angle for seamless epi fill

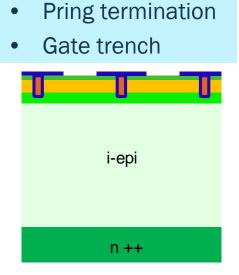
Deep trench etch, dual epi, oxide fill



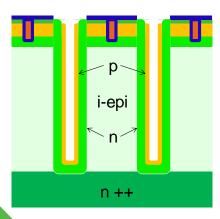
Large shrinking potential
n-epi/p-epi control ~2-3%,
grown during same run !
Dielectric fill

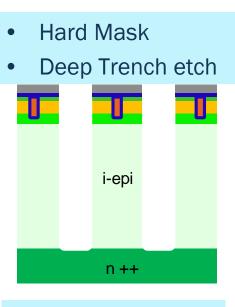


Trench based Super Junction Device cross-section

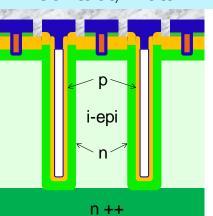


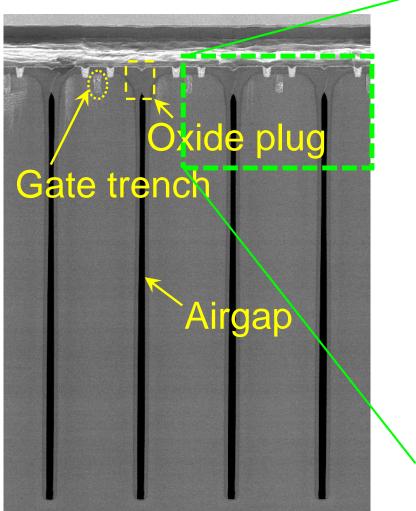
 Selective epi, n- and p-type

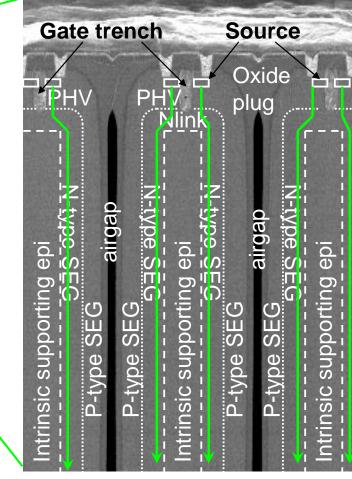




- Oxide seal
- Contact, metal









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Periodic Table & Electro Negativity

H 2.1												III	IV	V			He
Li 1.0	Be 1.5											В 2.0	C 2.5	N 3.0	0 3.5	F 4.0	Ne
Na <mark>0.9</mark>	Mg 1.2											AI 1.5	Si 1.8	Р 2.1	S 2.5	CI 3.0	Ar
K 0.8	Ca 1.0	Sc 1.3	Ti 1.5	V 1.6	Cr 1.6	Mn 1.5	Fe 1.8	Co 1.8	Ni 1.8	Cu 1.9	Zn 1.6	Ga 1.6	Ge 1.8	As 2.0	Se 2.4	Br 2.8	Kr 3.0
Rb 0.8	Sr 1.0	Y 1.2	Zr 1.4	Nb 1.6	Мо 1.8	Тс 1.9	Ru 2.2	Rh 2.2	Pd 2.2	Ag 1.9	Cd 1.7	In 1.7	Sn 1.8	Sb 1.9	Те 2.1	І 2.5	Xe 2.6
Cs 0.7	Ва <mark>0.9</mark>	La 1.1	Hf 1.3	Та 1.5	W 1.7	Re 1.9	0s 2.2	lr 2.2	Pt 2.2	Au 2.4	Hg 1.9	Ti 1.8	Pb 1.8	Bi 1.9	Po 2.0	At 2.2	Rn 2.4
Fr 0.7	Ra <mark>0.7</mark>	Ac 1.1	Unq	Unp	Unh	Uns	Uno	Une									
Ce	Pr	Nd	Pm	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu				
1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.2				
Th 1.3	Ра 1.5	U 1.7	Np 1.3	Pu 1.3	Am 1.3	Cm 1.3	Bk 1.3	Cf 1.3	Es 1.3	Fm 1.3	Md 1.3	No 1.3	Lr				

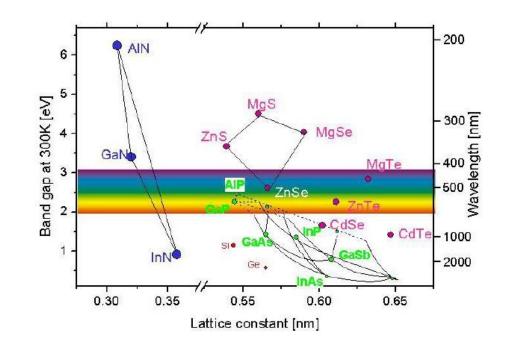


GaN/AIGaN/InAIGaN (III-V)

- Al/Ga/In Nitride system ("III-V") stems from LEDs
 - By tuning the In %, the full visible spectrum can be covered (photon emission), Direct bandgap
 - Bandgap engineering by tuning Al % for power devices
- 2 Nobel prizes in Physics
 - Alferov et al., 2000
 - Akasaki et al., 2014

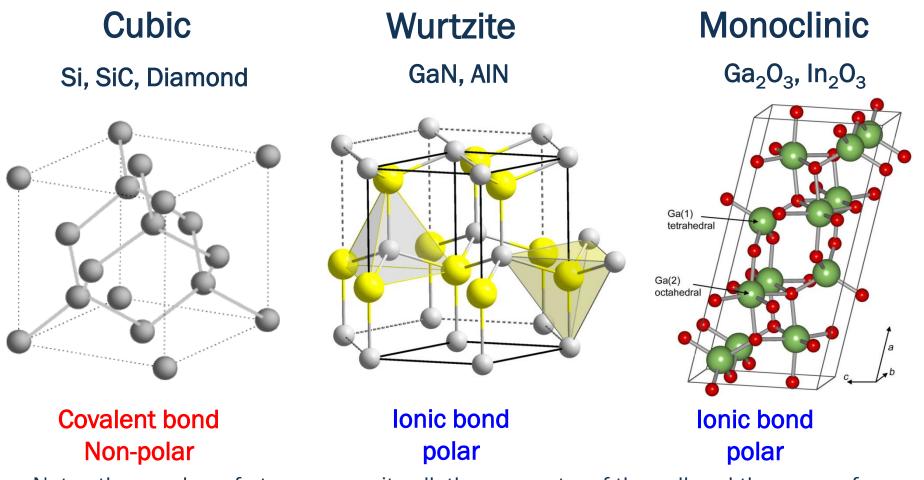


Isamu Akasaki, Hiroshi Amano and Shuji Nakamura, Nobel Prize 2014





Crystal Structures. Polar vs non-polar

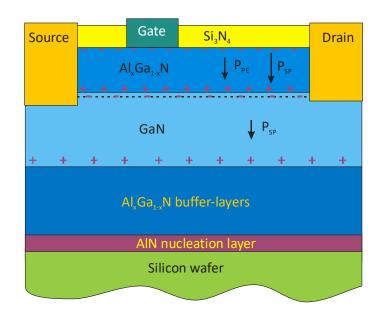


<u>Note</u> : the number of atoms per unit cell, the symmetry of the cell and the mass of the elements determines the thermal conductivity of the material.

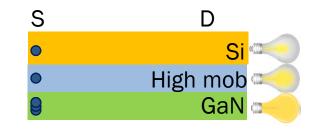


AIGaN/GaN Lateral HEMT Devices

AIGaN/GaN <u>High Electron Mobility Transistors feature :</u> Low Ron due to high 2DEG density with n_s~9x10¹² cm⁻² and high mobility (~2000 cm²/V.s) High breakdown because of high bandgap (3.4 eV) Low capacitance : no junctions to deplete (un-doped)



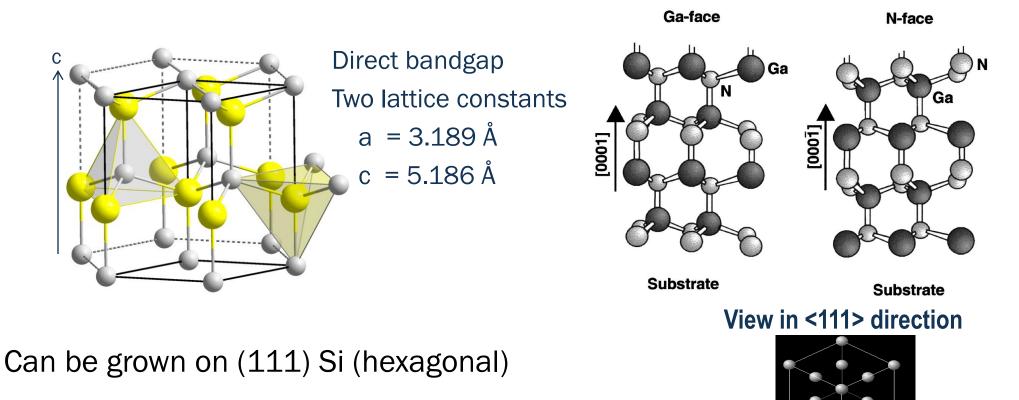
Device Property Material Property





GaN Crystal Structure–Wurtzite

- GaN has a <u>Wurtzite</u> structure, thermodynamically stable.
- Growth is along the c-axis, can be <u>Ga-face</u> or N-face. Two interpenetrating hexagonal close-packed sublattices.





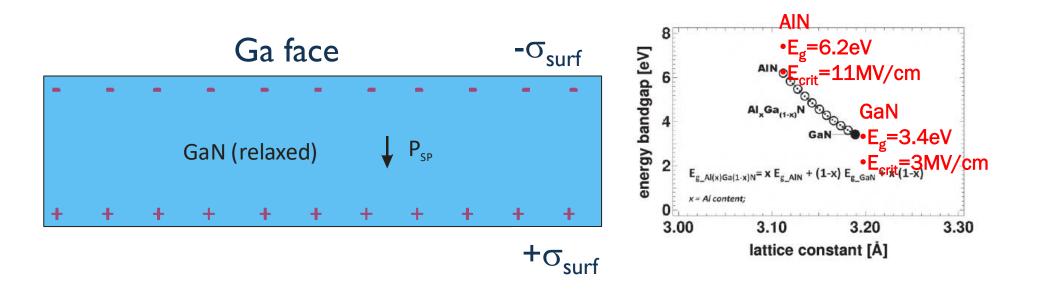
Spontaneous polarization

<u>Spontaneous Polarization</u> due to electro-negativity difference between N-atoms and Ga-atoms (binary crystal).

• Pauling's electronegativity : N=3.4, Ga=1.8, Al=1.6

Poisson's equation yields σ_{surf}

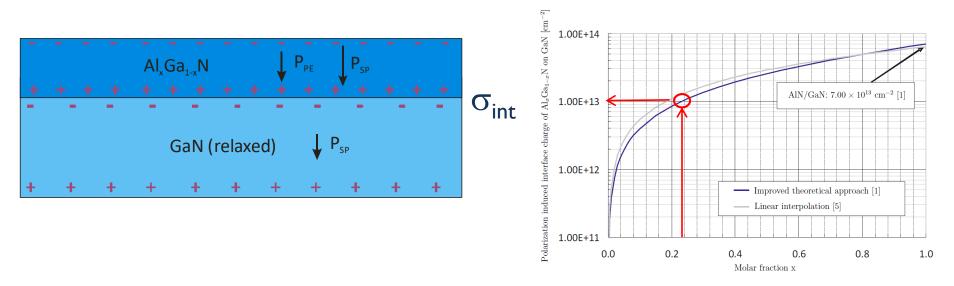
Results in a polarization field P





Spontaneous and piezo-electric polarization

• Al(Ga)N has larger polarization field than GaN (due to larger Electro-negativity difference)

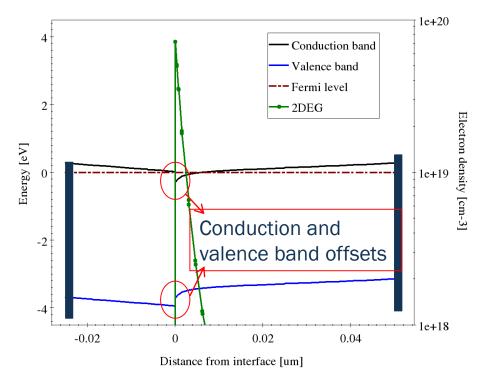


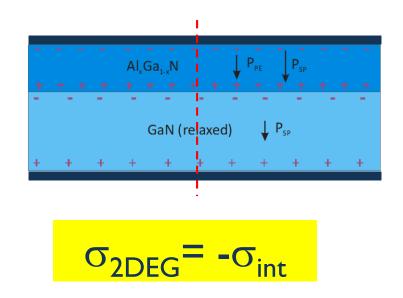
- Thin AlGaN layer strained \rightarrow piezo-electric pol.
- Induced net positive charge at the AlGaN/GaN interface (but inside the AlGaN !) is very large !
 - HEMT n_s~ 10^{13} cm⁻² \leftrightarrow Typical MOSFET n_s ~ 10^{12} cm⁻²



Solving the Poisson equation—1D

- Ohmic contacts at bottom and top of the structure
- Charge neutrality : Electrons compensate the net positive polarization charge, i.e. creation of a <u>2DEG</u>
- Leads to the creation of a quantum well at the AlGaN/GaN interface (but in the GaN layer !)



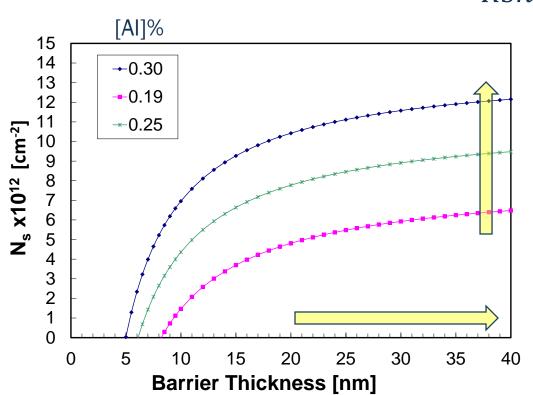




Device Engineering (AlGaN/GaN)

2DEG is a sheet of electrons

- Density n_s (set by barrier design)
- Mobility μ_N



$$Rsheet = \frac{1}{q.n_s.\mu_N} \left[\Omega/\Box\right]$$

Limitations :

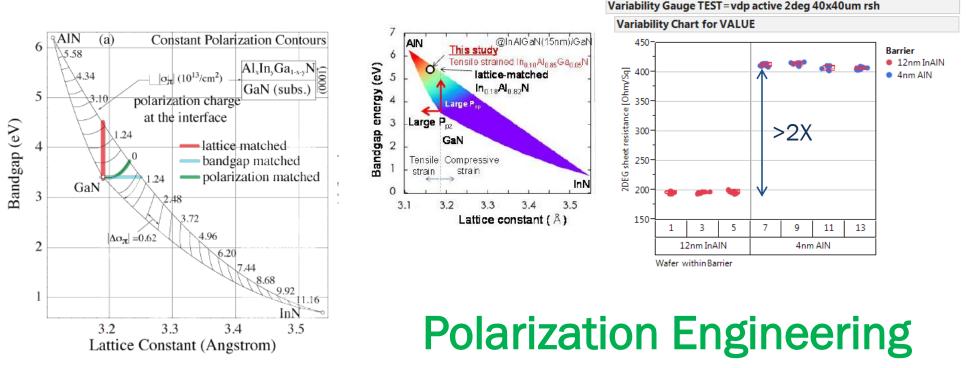
- If the (strained) AlGaN barrier is too thick, it will crack.
- The higher the [Al]%, the lower the critical thickness



Polarization Engineering : Quarternary alloys

Al_xIn_yGa_{1-x-y}N quarternary alloys coherently grown on GaN

- Lattice matched (reliability?), Polarization matching (E-mode)
- Higher sheet density (lower Ron) & larger bandgap



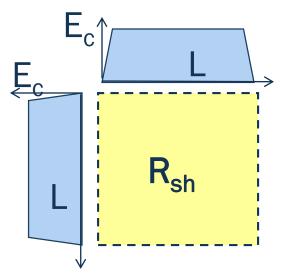
DJ Jena et al, 2010

Reduces Ron by 2-3X



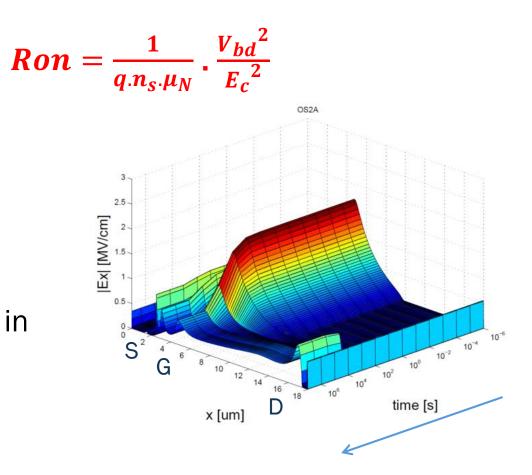
Ron/Vbd of a HEMT (drift region only !)

• Semiconductor is un-doped i.e. behaves like a dielectric→Electric field is rectangular



 Surface field shaping and dynamic effects might result in more triangular electric field

$$Ron = \frac{4}{q.n_s.\mu_N} \cdot \frac{V_{bd}^2}{E_c^2}$$

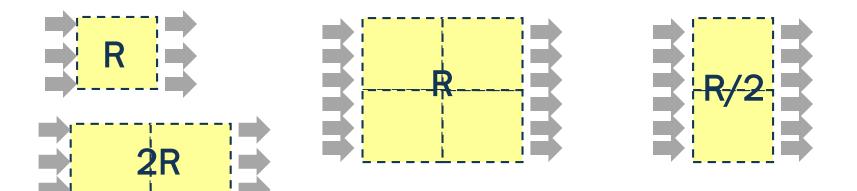




Sheet Resistance

- The resistance of a thin sheet with uniform doping (e.g. 2DEG). Conveniently expressed in Ω /square, or Ω /
- Just count #squares parallel to the current flow Depends on carrier density (n_s) and mobility

$$Rsheet = \frac{1}{q.n_s.\mu_N} \left[\Omega/\Box\right]$$





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Summary : Ron versus Vbd for different device concepts

1D unipolar device :

$$Ron = \frac{4.V_{bd}^2}{E_c^3.\varepsilon.\mu_N}$$

2D unipolar Super Junction device :

$$Ron = \frac{2.V_{bd}}{E_c^2.\varepsilon.\mu_N}$$

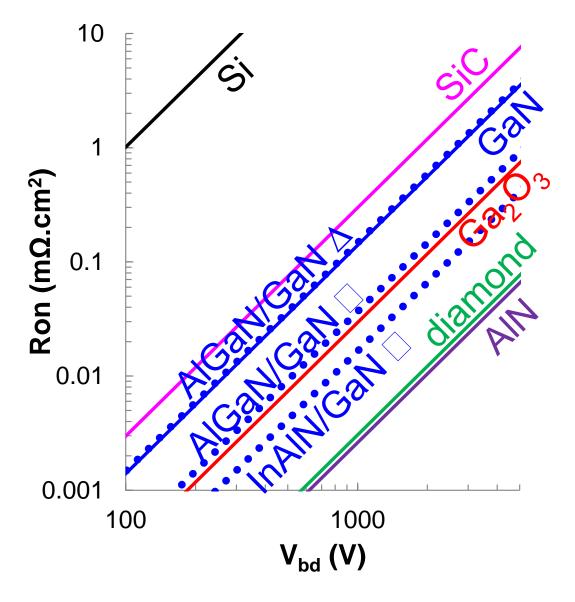
Lateral hetero-structure HEMT :

$$Ron = \frac{1}{q.n_s.\mu_N} \cdot \frac{V_{bd}^2}{E_c^2}$$



Ron/Vbd of a HEMT (drift region only !)

- AlGaN/GaN HEMT with rectangular field will go beyond the 1D GaN limit.
- By introducing polarization engineering (InAIN), even the Ga_2O_3 1D limit is broken.





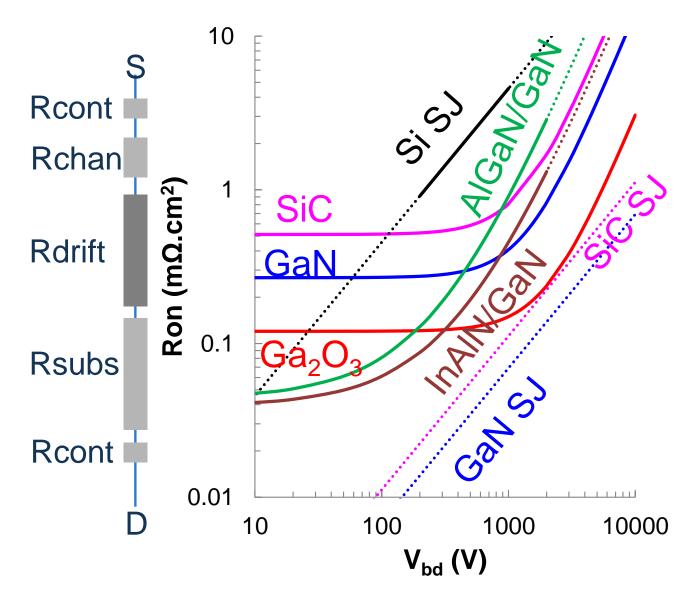
The Baliga FOM revisited

S Rcont Ga_2O_3 GaN **HEMT** Si SJ SiC TrenchMOS V-MOS Rchan Very low Rcont <5% <5% ~10% low Rsubs <3mΩ.cm 20mΩ.cm $10m\Omega.cm$ 6mΩ.cm NA Rdrift $Ron = \frac{4.V_{bd}^{2}}{E_{c}^{3}.\varepsilon.\mu_{N}} Ron = \frac{4.V_{bd}^{2}}{E_{c}^{3}.\varepsilon.\mu_{N}}$ $Ron = \frac{2.V_{bd}}{E_c^2.\varepsilon.\mu_N}$ $Ron = \frac{4.V_{bd}^{2}}{E_{c}^{3}.\varepsilon.\mu_{N}}$ Rdrift $Ron = \frac{1}{q \cdot n_s \cdot \mu_N} \cdot \frac{V_{bd}^2}{E_c^2}$ Medium Rchan Very low ? low **Rsubs** Source Gate Undoped AIGaN Anode (Cu/Au/Ni), q400 µm Gate Source Source $_{
m /}\,{\rm HfO_2(50~nm)}$ Al_sGa_{sa}N P_{ec} /D, = 2.5 μ P_{sp} $V_{\text{trench}} = 4.8 \, \mu \text{m}$ $W_{\text{mesa}} = 1.2 \, \mu \text{m}$ PG Rcont Ga2O3 film, 6 × 1016 cm-3, 7 µm Ρ N P Undoped GaN Carbon-doped GaN n-GaN drift layer Ga₂O₃ substrate 2.5 × 10¹⁸ cm⁻³, 350 µm Silicon wafer GaN Substrate D Cathode (Ti/Au) N⁺_{sub} Drain **n+** Drain



Public Information

The Baliga FOM revisited



Si SJ

- p=6µm HEMTs
- E_c=2MV/cm (triang field)
- E-mode (R_{ch}=2XR_{access}) SiC
- TrenchMOS
- Subs=100μm, 20mΩ.cm
- p=5 μ m, μ_{ch} =100cm²/V.s GaN
- V-MOS
- Subs=100μm, 10mΩ.cm
- + p=10µm, μ_{ch} =1500cm²/V.s Ga_2O_3
- Schottky diode
- Subs=200μm, 6mΩ.cm
- $\mu_{\text{bulk}}=300 \text{ cm}^2/\text{V.s}$



Capacitances : jct transistor vs HEMT

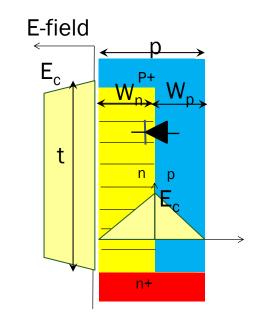
<u>1D-Jct transistor</u>, C_{depl} is dependent on voltage

$$C_{depl} = \frac{\epsilon}{W_D}; W_D = \sqrt{\frac{2.\epsilon.(V_{applied} + V_{bi})}{q.N_D}} \qquad Q_{OSS} \Big|_V = \sqrt{2.\epsilon.q.N_D}.V^{1/2} \qquad Q_{OSS} = \epsilon.E_C$$
$$N_D = \sqrt{\frac{\epsilon.E_C^2}{2.q.V_{BD}}} \qquad E_{OSS} \Big|_V = \frac{1}{3}\sqrt{2.\epsilon.q.N_D}.V^{3/2} \qquad E_{OSS} = \frac{1}{3}\epsilon.E_C.V$$

Super-junction device

Depletion of $Q_{opt}(Q_{opt}=313nC/cm^2)$ Large junction area, will deplete at ~25V Once depleted, capacitance is very low

$$\boldsymbol{E_{C}} \cdot \boldsymbol{\varepsilon_{s}} = 2. q. N_{n} \cdot W_{n} = \boldsymbol{Q_{opt}} [\frac{C}{cm^{2}}]$$
$$Q_{OSS} \Big|_{V} = 313. hp. \frac{V}{E_{C}}$$





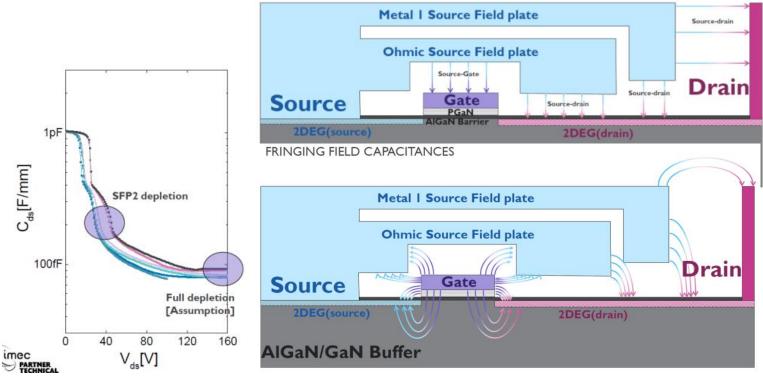
Public Information

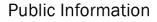
Capacitances : jct transistor vs HEMT

<u>**HEMT</u>** : capacitance is a sum of dielectric capacitances, each independent of voltage</u>

- Field plate capacitors that deplete the 2DEG
- Substrate capacitance
- Fringe capacitances

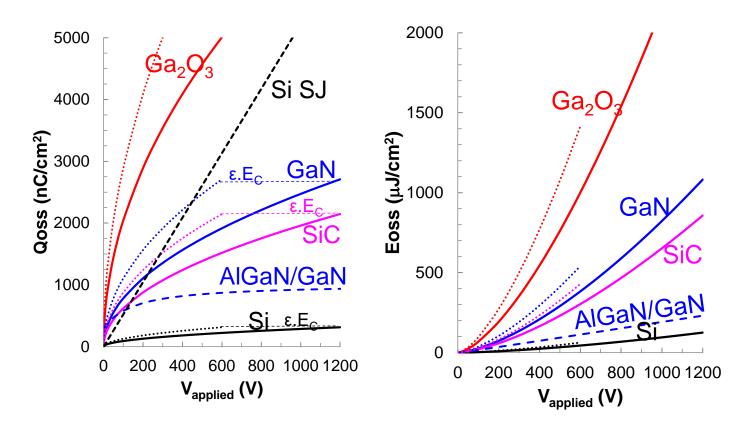
PARALLEL PLATE CAPACITANCES





Capacitances

- Q_{oss} and E_{oss} are ~ to ϵE_c [in cm⁻², per unit area]
 - 1S--Si is better than GaN and SiC and Ga₂O₃
 - AIGaN/GaN HEMT behaves differently
 - Si SJ has high Q_{oss} due to large effective junction area





Outline

- Power devices=material properties
 - 1D limit for a vertical transistor
 - Resurf effect (2D)
- Non-polar and polar materials
 - Concept of polarization charge
 - Simple band structure
- HEMT "High Electron Mobility Transistor"
 - HEMT versus vertical power device
- Ron and Capacitance versus Voltage
- Cost and performance



The Baliga FOM revisited

	Si SJ	SiC TrenchMOS	GaN V-MOS	Ga ₂ O ₃ Schottky	HEMT
Rcont	Very low	low	<5%	<5%	~10%
Rsubs	<3mΩ.cm	20mΩ.cm	10mΩ.cm	6mΩ.cm	NA
Rdrift	$Ron = \frac{2.V_{bd}}{E_c^2.\varepsilon.\mu_N}$	$Ron = \frac{4.V_{bd}^2}{E_c^3.\varepsilon.\mu_N}$	$Ron = \frac{4.V_{bd}^2}{E_c^3.\varepsilon.\mu_N}$	$Ron = \frac{4.V_{bd}^2}{E_c^3.\varepsilon.\mu_N}$	$Ron = \frac{1}{q.n_s.\mu_N} \cdot \frac{V_{bd}^2}{E_c^2}$
Rchannel	low	high	Medium	?	Very low
Capacitance	low	medium	medium	high	low
Wafer (mm)	200-300	100-150	75-100	50-100	150-200
Cost/wfr (\$)	lowest	high	Very high	medium	low
Robustness	High	High	Some	?	None
	P N P N ⁺ _{sub}	Source Gate	Undoped AIGaN Source P.GaN well P.GaN well Undoped GaN Carbon-doped GaN n-GaN Substrate Drain	Anode (Cu/Au/Ni), φ 400 µm HfO ₂ (50 nm) $D_{trench} = 4.8 µm$ $W_{mess} = 1.2 µm$ Ga ₂ O ₃ film, 6 × 10 ¹⁶ cm ³ , 7 µm Ga ₂ O ₃ substrate 2.5 × 10 ¹⁶ cm ³ , 350 µm Cathode (Tt/Au)	Source Gate SI,N, Drain Al Ga,N I P., P., P., Gan I P., 4. + + + + + + + + + Al Ga, N Exitor layer All inclusion layer Silicon water

Public Information



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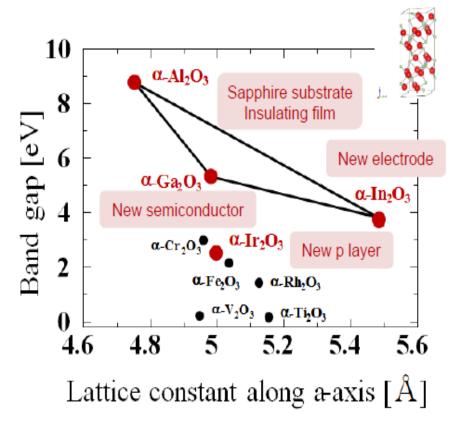
Metal Oxides : The Case of Ga₂O₃

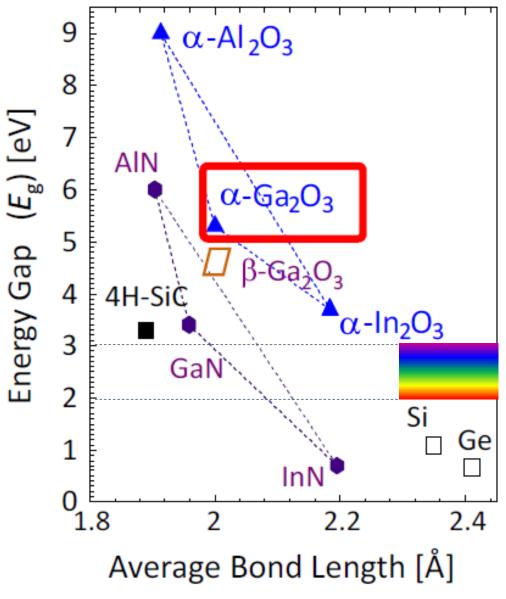
Public Information



α -Ga/Al/In/₂O₃ (III-VI)

- α -Ga₂O₃, α -Al₂O₃ and α -In₂O₃ have same crystal structure
 - Alloys & Hetero-structures
 - P-type !







Ga₂O₃ has many poly-types

 α -Ga₂O₃

- Rhombohedral ; stable till ~800°C
- Eg=5.6eV
- Ec=10MV/cm
- Alloys / heterostructures with Al/Ir/Rh/In₂O₃
- N-type doping by Sn, Si, ...
- P-type ! Ir/Rh/₂O₃
- Grown on Sapphire + liftoff

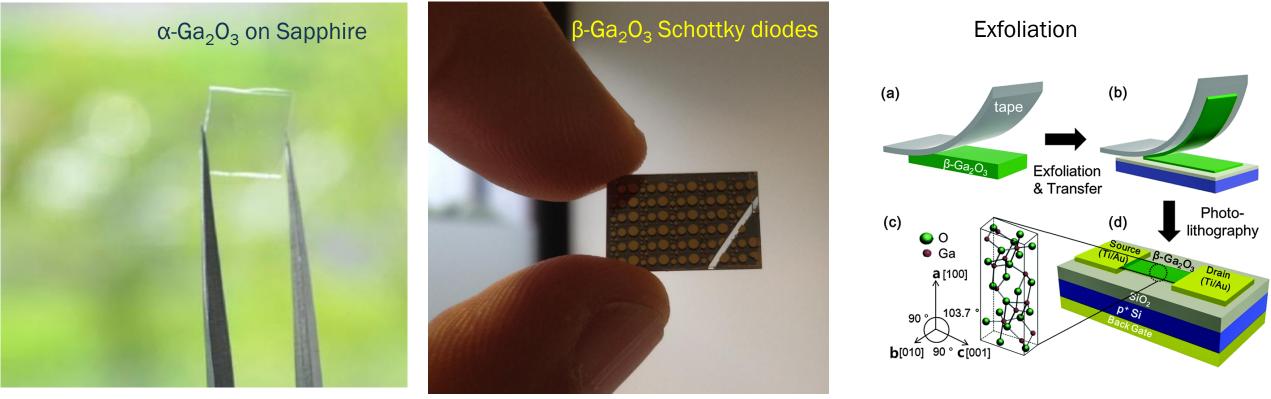
 β -Ga₂O₃

- Monoclinic, stable till melting point (~1700°C)
- Eg=4.8eV
- Ec=8MV/cm
- No alloys or heterostructures
- N-type doping by Sn, Si, ..
- No P-type ! (Mg, deep acc)
- Grown from the melt (CZ)



How Cool is That !

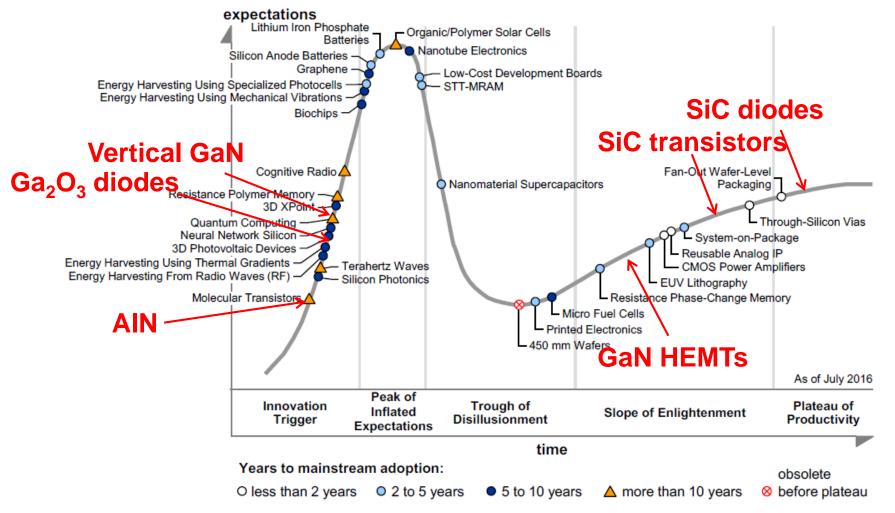
- Metal Oxides are transparent to the visible light
- They have a direct bandgap → opto-electronic devices
- Exfoliation of 20 μ m films \rightarrow flexible electronics

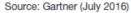




The Hype Cycle for Electronic Technologies

Figure 1. Hype Cycle for Semiconductors and Electronics Technologies, 2016

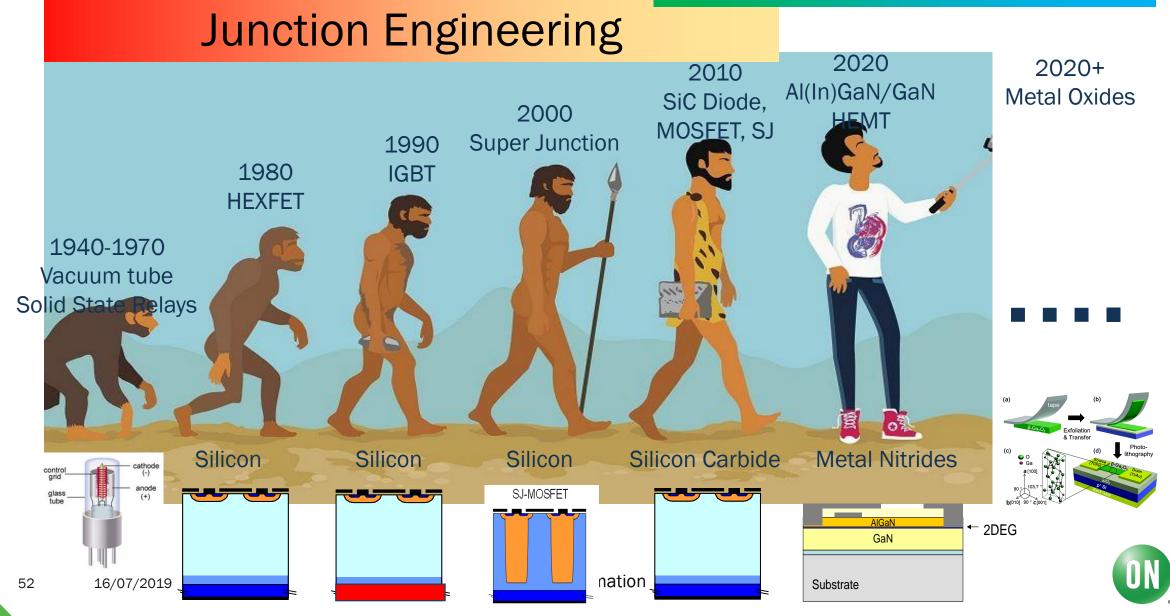






The Evolution of Power Devices

Materials Engineering



THINK ON.

Semiconductor Power Devices : Part 2 : Reliability Basics

Peter Moens



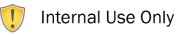
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Outline

- Reliability Basics
 - What is Reliability ?
 - Reliability Distribution Functions & Failure rates
 - Lognormal and Weibull Statistics
 - Acceleration testing and Lifetime Prediction







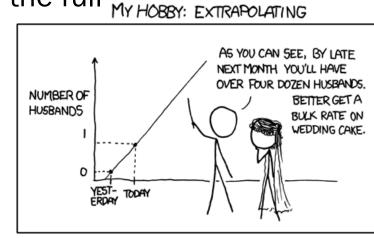




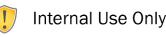
Reliability : What ?

re-li-a-bil-i-ty ra līa biladē/ the quality of being trustworthy or of performing consistently well

- Reliability = predict and guarantee a certain function over the full
 MY HOBBY: EXTRAPOLATING
 lifetime of the product
 - What is the desired "performance" ?
 - What is the desired "lifetime" ?
 - How to predict ?
- Reliability = Quality over time
- Reliability = physics, mathematics, statistics, economics and psychology
- Reliability = engineering in its most practical form







No reliability

No Product

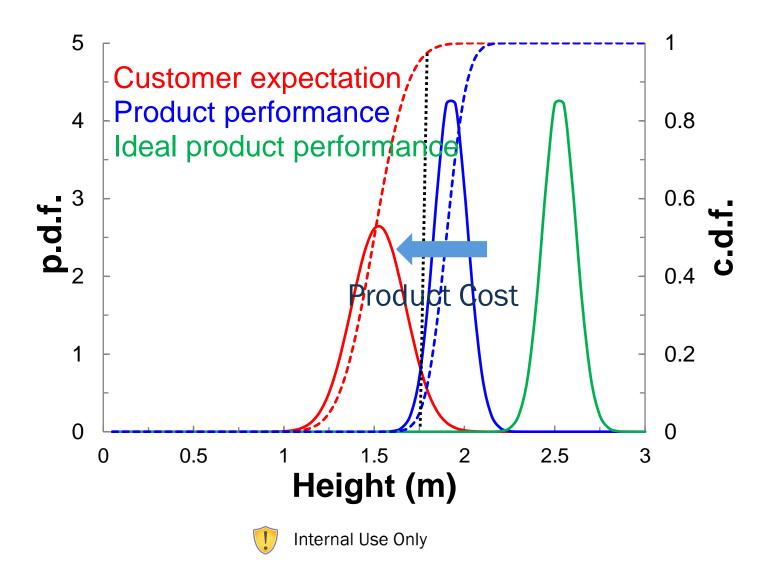
No Money





Product Reliability : the economical approach

• Example : product return due to dropping of a smartphone from a certain height.





Electronic Product Reliability Grades

- Consumer
- Industrial
- Automotive/Medical
- Military
- Space

Stress Test HTOL [®] IC HTRB Discrete	Consumer (g, h) ~2-3 year life 77 Units/Lot 504 Hours Tj=125°C 77 Units/Lot 504 Hours	Industrial (g) > 3 year life 77 Units/Cot 1008 Hours Tj=125°C	Automotive/Medical (b,c,f) 77 Units/Lot Grade 1: 1000 Hr¢0, Ta≠125°C, See Q100 for	Military (d, e) 45 Units/Lot
	504 Hours Tj=125°C 77 Units/Lot	1008 Hours Tj=125°C		45 Units/Let
HTRB Discrete			other grades	40 Onligitot 1000 Hr @ Ta=125°C or 184 Hr @ Ta=150°C
	Tj=150°C or specified TJ(max)	77 Units/Lot 1008 Hours Tj=150°C or specified TJ(max)	77 Units/Lot 1008 Hours Tj=150°C or specified TJ(max)	NA to Discrete Military.
HTGB [*] Discrete	77 Units/Lot 504 Hours Tj=150°C or specified TJ(max)	77 Units/Lot 1008 Hours Tj=150°C or specified TJ(max)	77 Units/Lot 1008 Hours Tj=150°C or specified TJ(max)	NA to Discrete Military.
HTBB* VHVIC only	77 Units/Lot 504 Hours Tj=125°C	77 Units/Lot 1008 Hours Tj=125°C	77 Units/Lot 1008 Hours Tj=125°C	NR
HVTHB* VHVIC only	77 Units/Lot 168 Hours Tj=85°C/60%RH	77 Units/Lot 168 Hours Tj=85°C/60%RH	77 Units/Lot 168 Hours Tj=85°C/60%RH	NR
ELFR IC	NR	48 Hours @ Tj=125C 24 hrs @ Tj=150C (Ontional, EIO)	Grade 1: 48 Hours @ Ta=125C or 24 hrs @ Ta=150C. See AEC Q100-008 for other grades	NA
LFR Discrete(not mandatory, not gating)	NR	NR	800 Units/Lot 48 Hours @ Tj=150C or specified TJ(max)	NA
HTSL [®] IC	25 Units/Lot 504 Hours Ta=T _{atorige max}	25 Units/Lot 1008 Hours Ta=T _{storage max}	77 Units/Lot Grade 1: +150°C Ta for 1000 hours or +175°C Ta for 500 hours, see AEC Q100 for other grades	45 Units/Lot 1008 hrs Ta=T _{storage max}
HTSL [®] Discrete	25 Units/Lot 504 Hours Ta=Tutuurs	25 Units/Lot 1008 Hours Ta=T _{storage max}	77 Units/Lot 1008 Hours Ta=T _{storage max}	45 Units/Lot 1008 hrs Ta=T _{storage max}
NVM Data Retention IC as required by technology	25 Units/Lot 504 Hours Ta=T _{storage max}	25 Units/Lot 1008 Hours Ta=T _{skrage max}	77 Units/Lot Grade 1: +150°C Ta for 1000 hours or +175°C Ta for 500 hours, see AEC Q100 for other grades	45 Units/Lot 1008 hrs Ta=T _{storage max}
PC surface mount only	SECTION 4	SECTION 4	SECTION 4	SECTION 4
TC* IC	25 Units/Lot 500 cyc -55 to 150 °C	25 Units/Lot 500 cycles -85 to 150 °C	77 Units/Lot Grade 1: 1000 cyc -55 to 150 °C or equiv, see AEC Q100 for other grades	45 Units/Lot 1000x @ -65 to 150 °C
TC ^a Discrete	25 Units/Lot 500 cyc -55 to 150 °C	25 Units/Lot 1000 cycles -55 to 150 °C	77 Units/Lot 1000 cycles -55 to 150 °C	NA to Discrete Military.
IOL Discrete	25 Units/Lot Per per Table 6 Mid Read Point	25 Units/Lot Per Table 6 Final Read Point	Per Per Per Table 6 Final Read Point	NA to Discrete Military.
AC or UHAST ^a	25 Units/Lot 48hrs	25 Units/Lot 96 hrs	// Units/Lot 96 brs	45 Units/Lot 96 hrs
HAST	25 Units/Lot 48hrs 25 Units/Lot	25 Units/Lot 96 hrs/Cu wire 192 hrs 25 Units/Lot	77 Units/Lot 98 hrs 77 Units/Lot	45 Units/Lot 96 hrs 45 Units/Lot
THB in lieu of HAST* IC	504 hrs 25 Units/Lot	1008 hrs/Cu Wire 2016 hrs 25 Units/Lot	1008 hrs // Units/Lot	1008 hrs

Sample sizes may be adjusted by the rel engineer based on historical knowledge or product need.





Sample size ? How many parts to test ?

- Samples shipped to the customer should obey the Poisson distribution function
 - Probability that an event (failure) occurs in a fixed interval of time, is constant, and independent of the time since the last event
 - For large sample size, the Poisson distribution is a good approximation of the Binomial distribution ("Poisson limiting theorem")

•
$$P(x) = \frac{n!}{x! * (n-x)!} p^x * (1-p)^n$$

P(x) : probability of having x failuresn : sample sizep : probability of having a single failx : number of failures

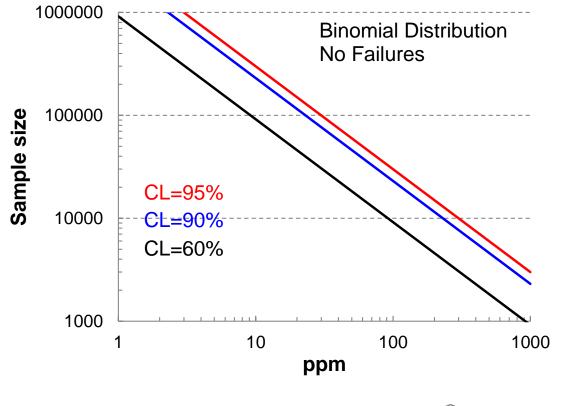




Sample size from Binomial distribution

$$P(x) = \frac{n!}{x! * (n-x)!} p^{x} * (1-p)^{n}$$

E.g. : Failure rate of a product is 100ppm. How many samples should be tested at CL=90% to prove you have 0 fails during qual ?

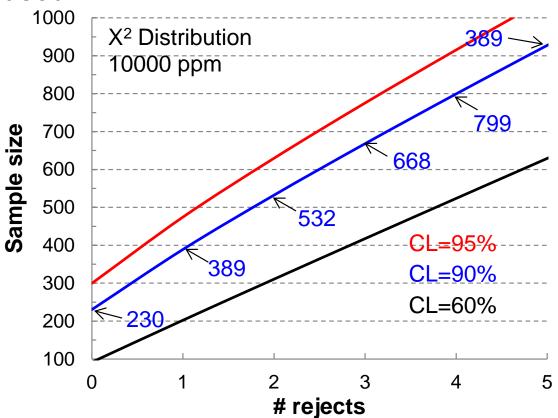


P(x) : probability of having x failures : 0.1 n : sample size : ? p : probability of having a single fail : 1e-4 x : number of failures : 0

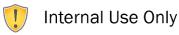


Sampling Statistics

- Sampling statistics allow you to draw conclusion on an unknown distribution based on sampling
- χ^2 distribution is the most widely used
 - For Hypothesis testing, Confidence Intervals, ML etc,
 - Distribution of the sum of squares of normally distributed variables
 - χ2 test is part of t-test or F-test



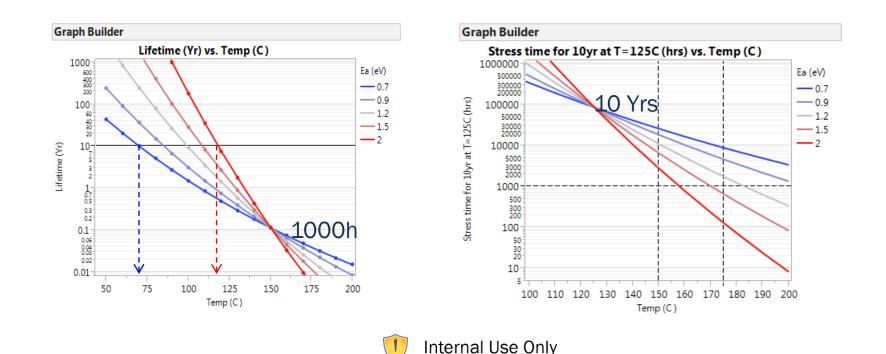
 $- N \ge \frac{1}{2} \cdot \chi^2 (2c+2;1-CL) \cdot (1/ppm-0.5)$





Accelerated testing : JEDEC Testing—designed for Si !

- JESD47 : (for Si) use an apparent $E_a = 0.7 eV$
 - T_{use} =55°C, T_{stress} =125°C \rightarrow 1000h at T=125°C equals 9 yrs at T=55°C
 - $T_{use}=70^{\circ}C$, $T_{stress}=150^{\circ}C \rightarrow 1000h$ at T=150°C equals 10 yrs at T=70°C
- E_a for GaN ? Little data available. E_a=2.1 eV ? [Whitman, MR 2014]
 - Larger E_a yields stronger impact of temperature on lifetime





FIT rates (Failure in time)

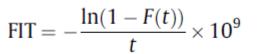
- 1FIT=1 failure per 10⁹ device.hours
- Acceleration factors for temperature and field
 - Stress at highest Voltage : AF_V=1

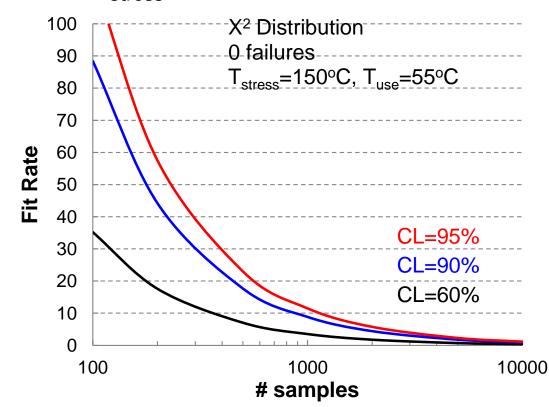
• T_{use} = 55°C for consumer

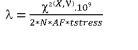
• T_{use} = 85°C for industrial

• T_{use} = 70°C for commercial

• Use Arhenius for AF_T with $E_a=0.7 \text{ eV}$ (Si), $T_{\text{stress}}=150^{\circ}\text{C}$







- $-\lambda = FIT rate$
- X = 1-CL (confidence level)

Tstress=1008 hrs

-v = 2r - 2

- To be looked up in chi-square table
- r = amount of rejects
 N = total sample size
- $AF = AF_V * AF_T$
- $AF_V = e^{\gamma * (V_{stress} V_{use})}$
- $AF_T = e^{\frac{E_a}{k} \cdot (\frac{1}{T_{uss}} \frac{1}{T_{stress}})}$
- t_{stress} = total stress time





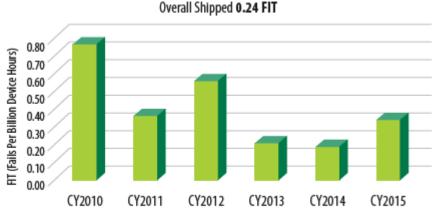
JEDEC Testing

What comes to mind when you hear "JEDEC Qualification": a typical qualification table

				Parameter		
Part Type	Test	Conditions	Duration	measurements @	Quantity	
Part no "X"	TC	-55°C/150°C	1000 cy	0/168/500/1000	3 x 77	
	H ³ TRB	85°C/85%RH/100V	1000 hrs	0/168/500/1000	3 x 77	
	HTRB	150°C/960V	1000 hrs	0/168/500/1000	3 x 77	
	HTGB	150°C/20V	1000 hrs	0/168/500/1000	3 x 77	
	IOL	delta Tj = 100°C	5,000 cy	0/2500/5000	3 x 77	
	AC	121°C/15psig	96 hrs			
	AC	121°C/15psig	96 hrs	Field Reli	eliability	

When you pass the JEDEC test, you have proven that (with For a binomial distribution (Poisson distribution) \rightarrow Constan

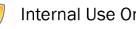
- FIT rate<18 for CL=60% (χ^2 estimate)
- FIT rate<38 for CL=90% (χ^2 estimate)
- For FIT<10, one would need to test >1000 samples for : failures.



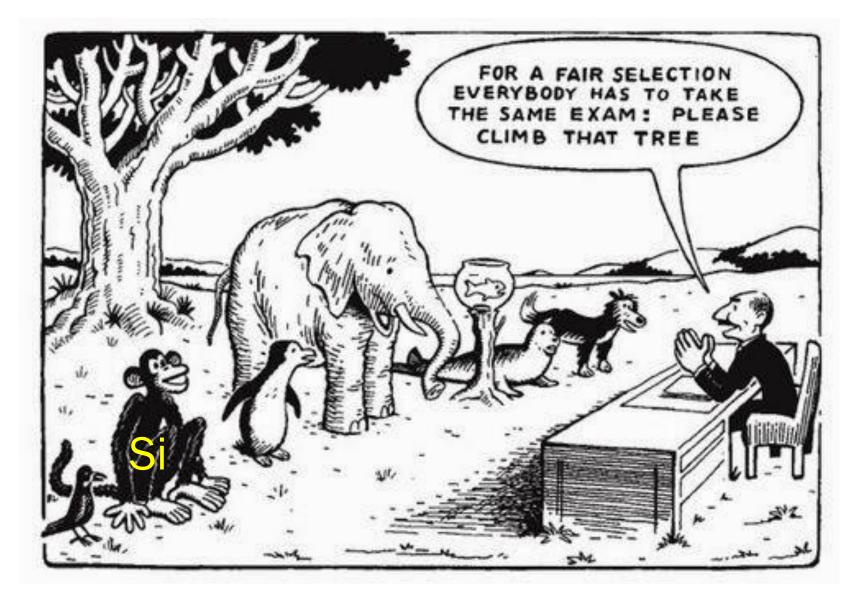
Actual FIT rates, EPC Reliability Report #7

Figure 6: Field reliability trend chart for all deployed eGaN products over the past 6 years. Values represent 60% confidence upper bound on the FIT rate.





JEDEC testing for WBG—makes sense?

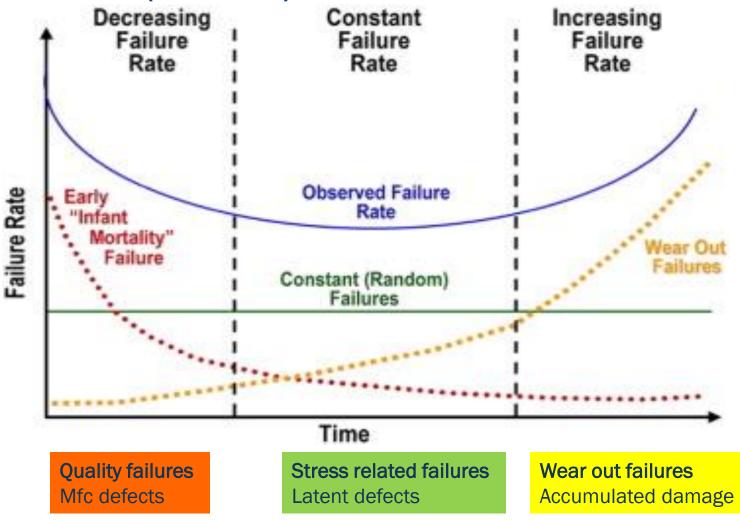






The Bath-tub Curve

• Failure (Hazard) rate λ as a function of time

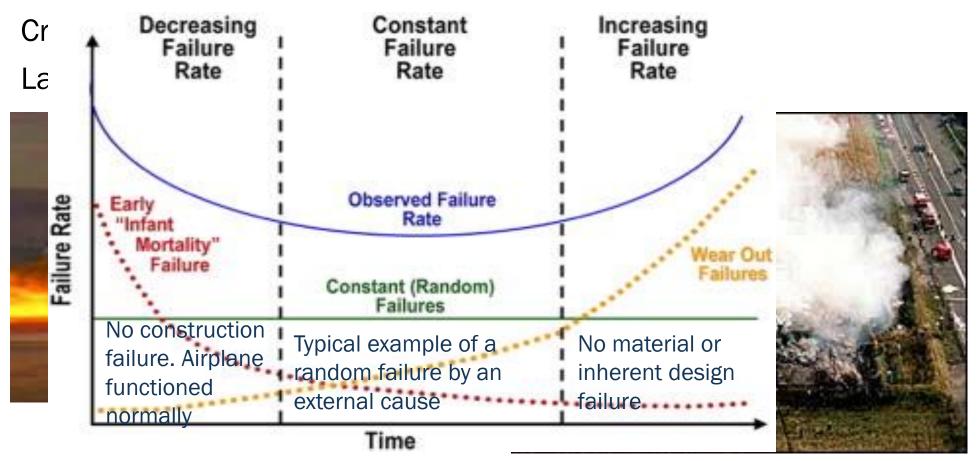




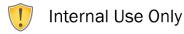


Crash of the Concorde (Mach 2)

First commercial flight on 12 Jan 1976

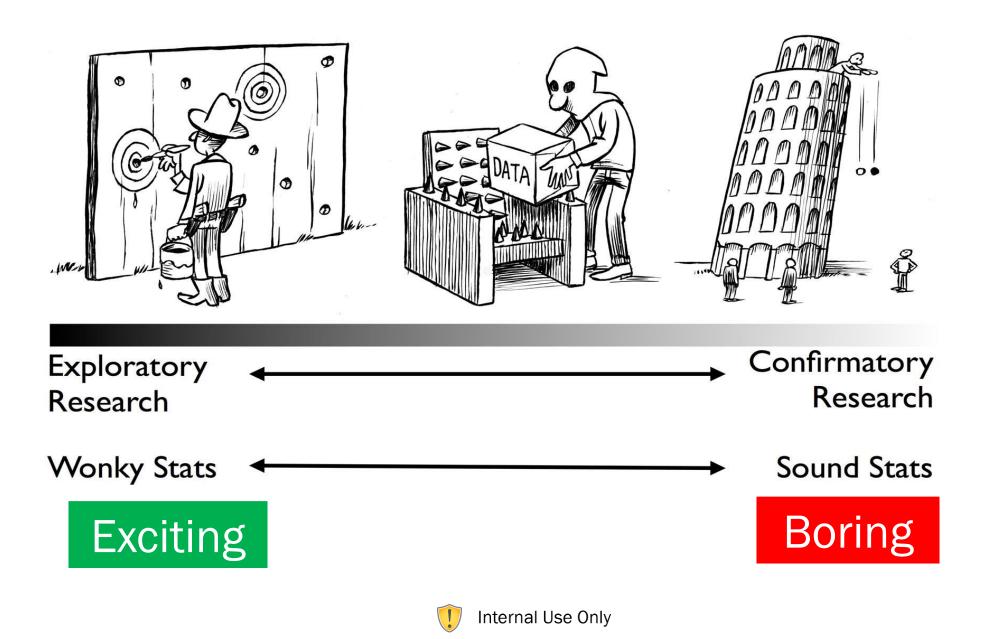


Was the Concorde less reliable after the crash ?





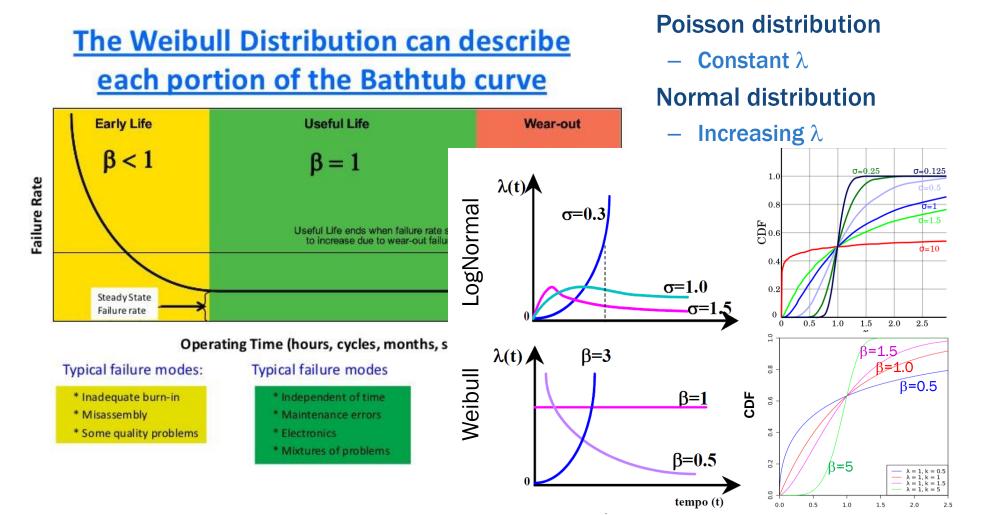
No Statistics=No Reliability





The Bath-tub Curve and Failure Functions

- Failure (Hazard) rate λ as a function of time



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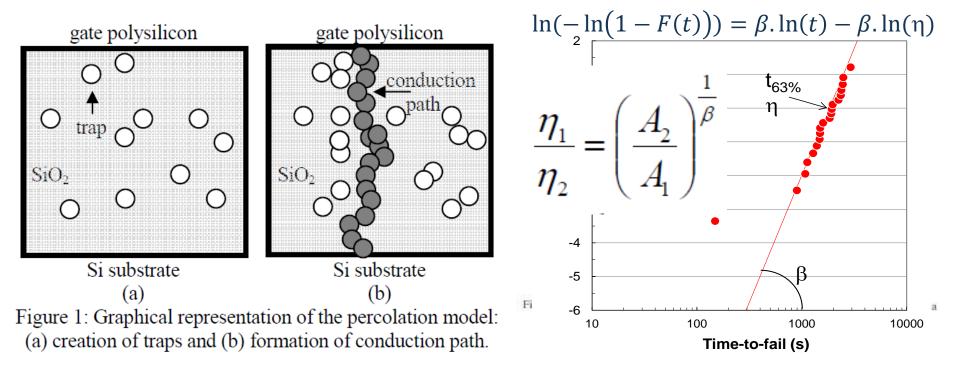


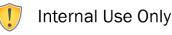
Weibull—Percolation

Weibull distribution is used for modeling "percolation" events. Has been widely used to model degradation of dielectrics.

Weibull distributed parameter is Charge-to-Breakdown ("Q_{bd}")

To assess Q_{bd} , constant current stress has to be applied (Q=I.t) Not practical, since lifetime acceleration/prediction requires voltage Constant voltage stress is used instead (but is actually <u>not</u> correct).







Weibull versus LogNormal distribution (eGaN gate reliability)

- Weibull and LogNormal differ in low percentiles
- LogNormal more optimistic
- All data for $100m\Omega$ devices, at T=150°C

