Fabrication of high power GaN transistors

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InRel
NPower

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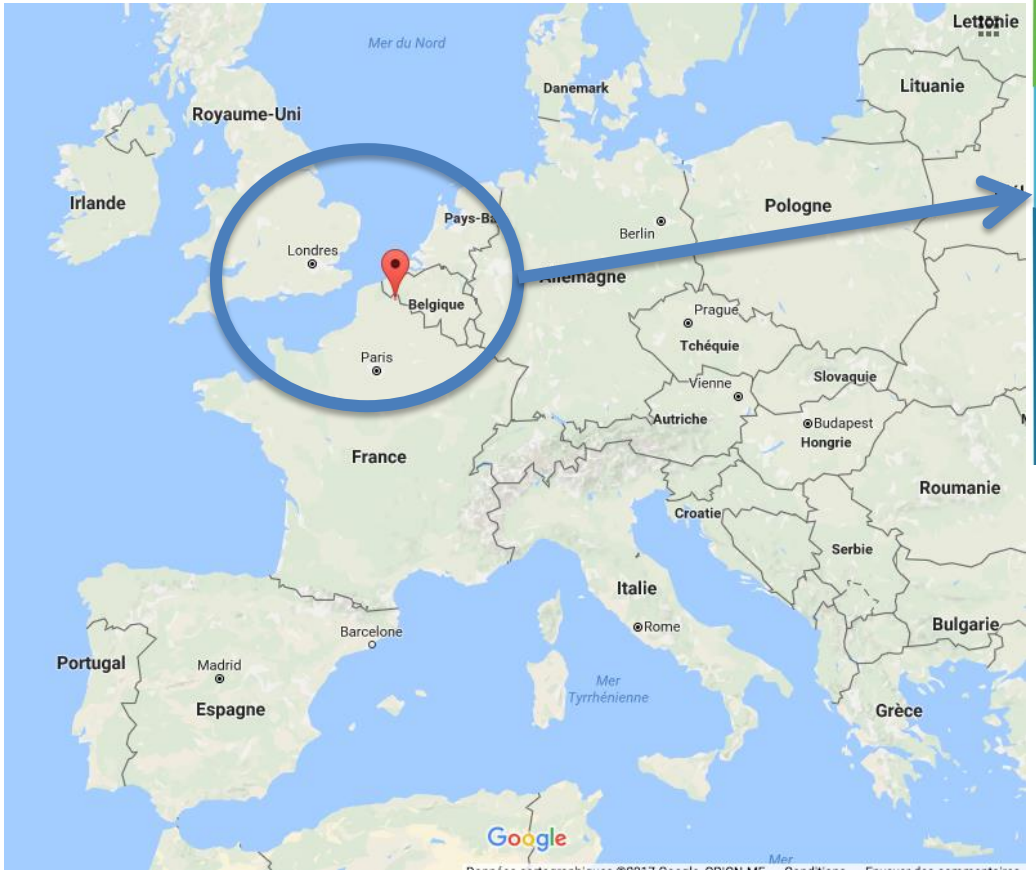
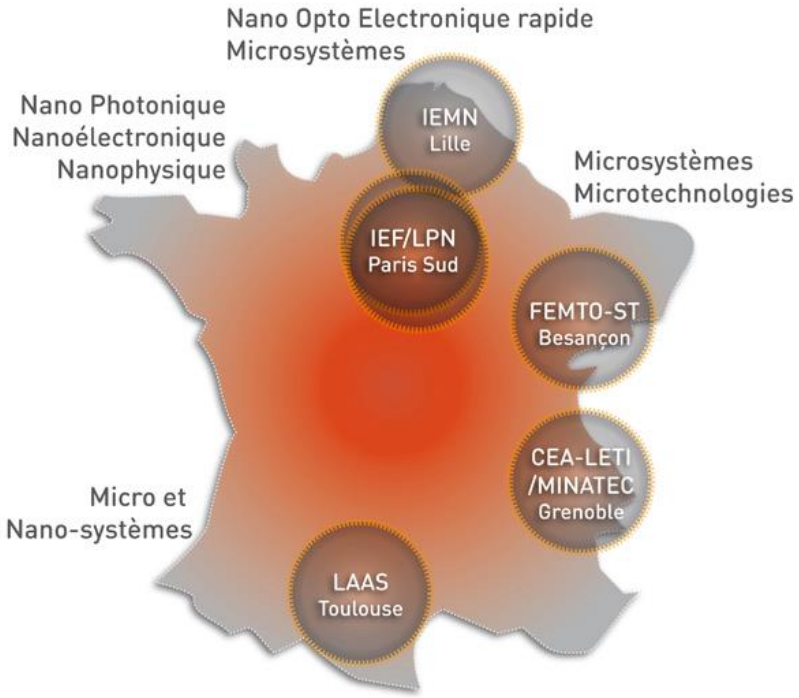
ISEN école d'ingénieurs ALL IS DIGITAL LILLE
RENATECH

Where are we ?

Lille city centre



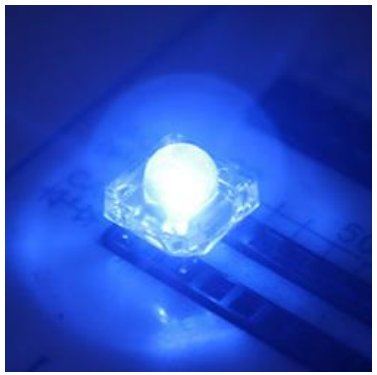
National Network of Large Technological Facilities for Basic Technological Research



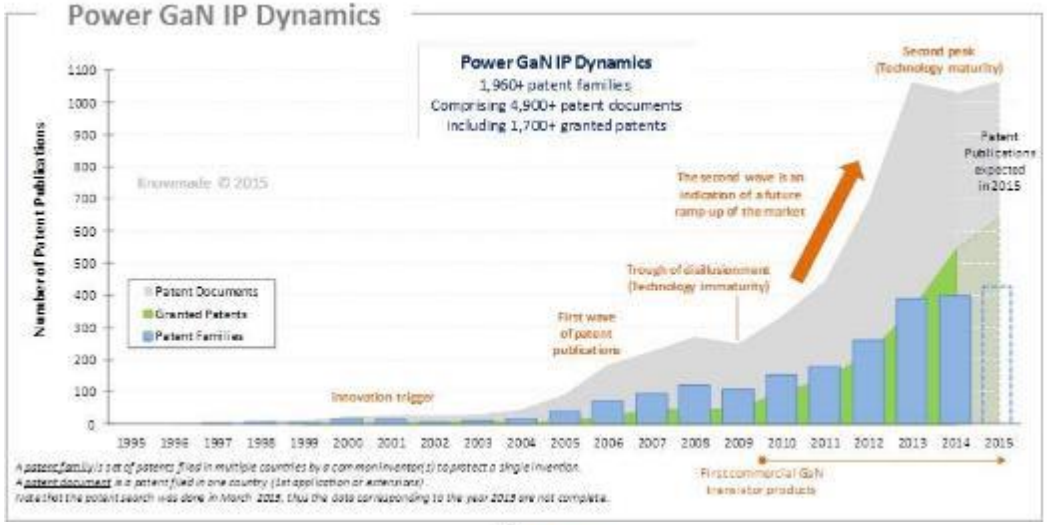
- Introduction
- Device design for high power devices
- Description of the device fabrication
  - Main processing techniques
  - Main technological bricks
- How to further push the breakdown limits of GaN-on-Si HEMTs
  - LSR approach developed within Inrel project
- Conclusion

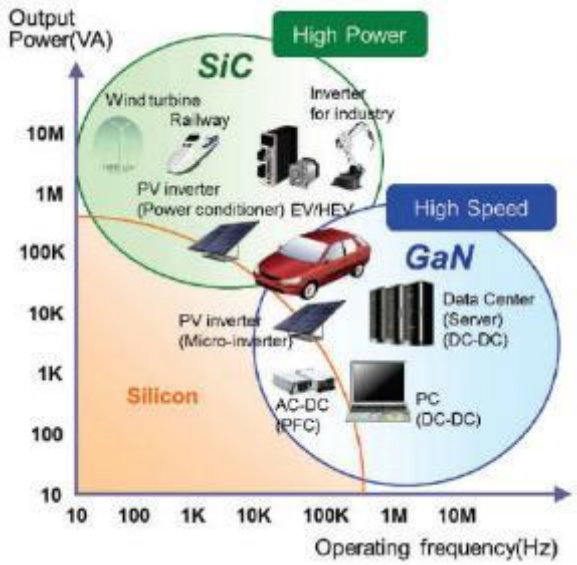
Gallium nitride is probably the most important new semiconductor since silicon

save energy, carbon emissions and enable totally secure communications

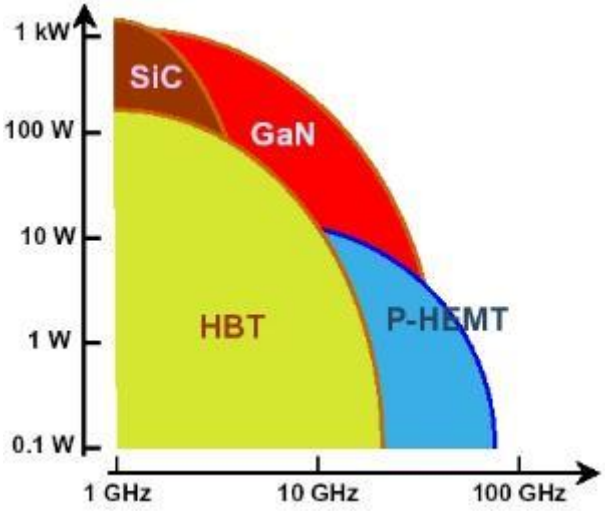


blue, green, yellow, red LEDs by adding more and more Indium to GaN



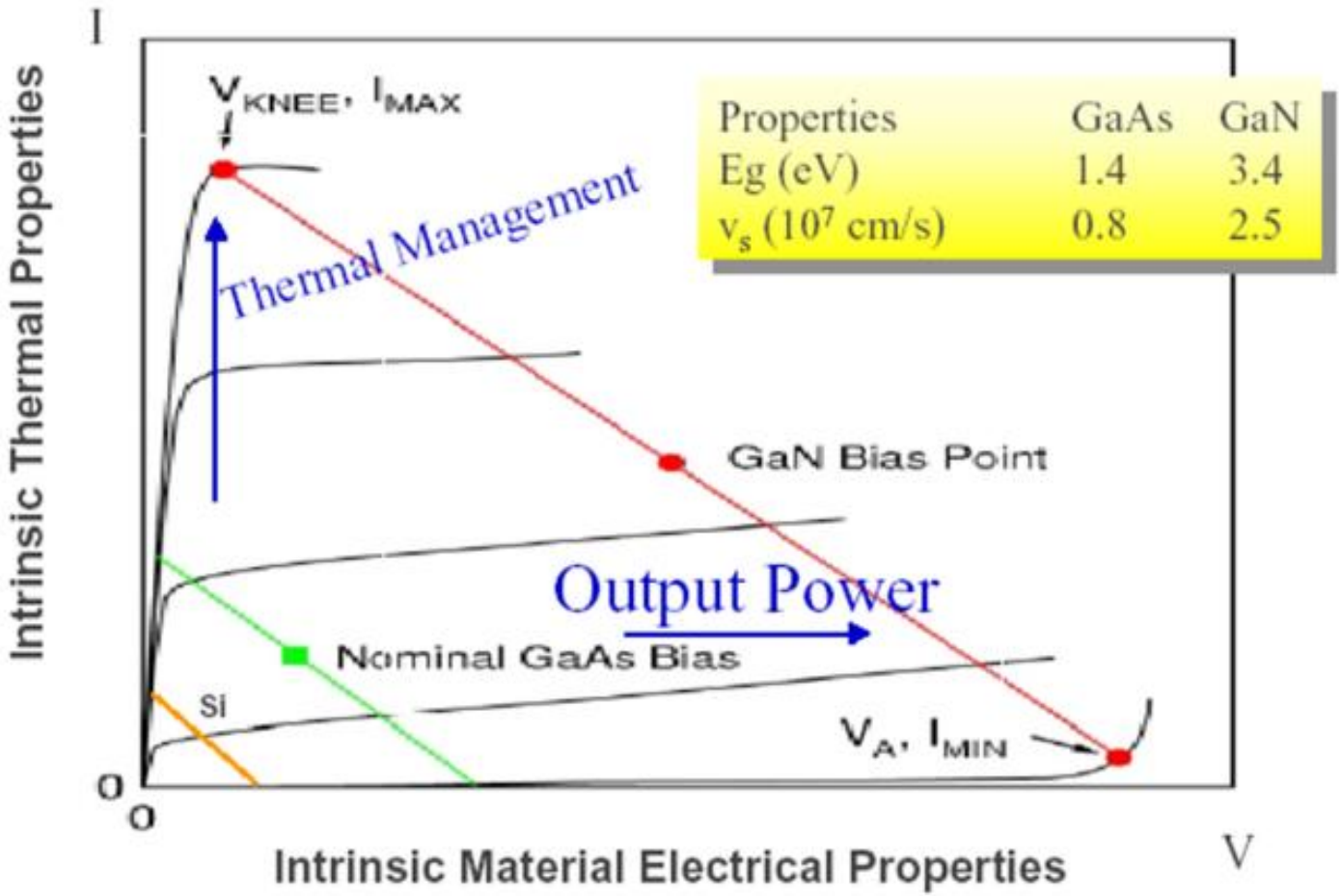


GaN superior to other semiconductor for both power and RF applications owing to its outstanding intrinsic properties

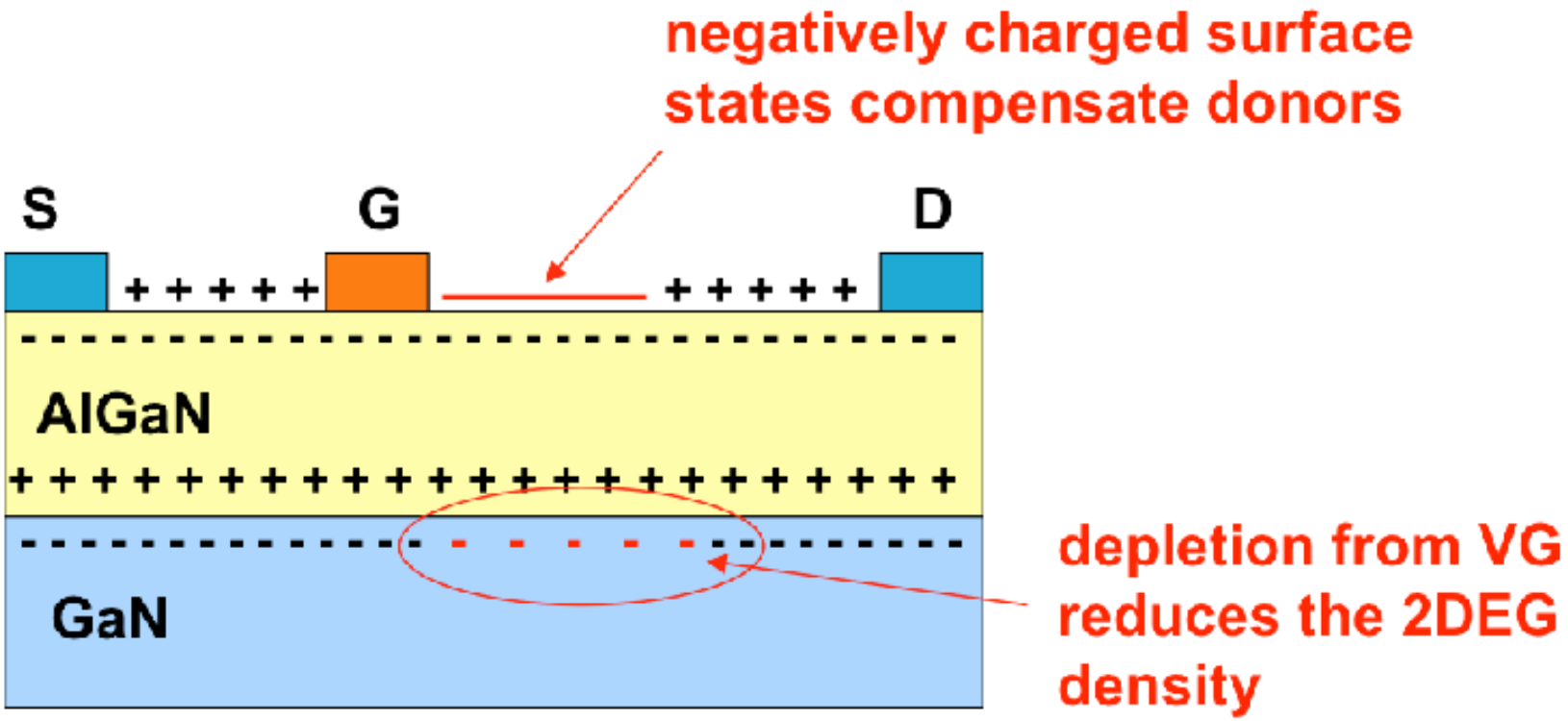


Breakthrough in terms of power performances

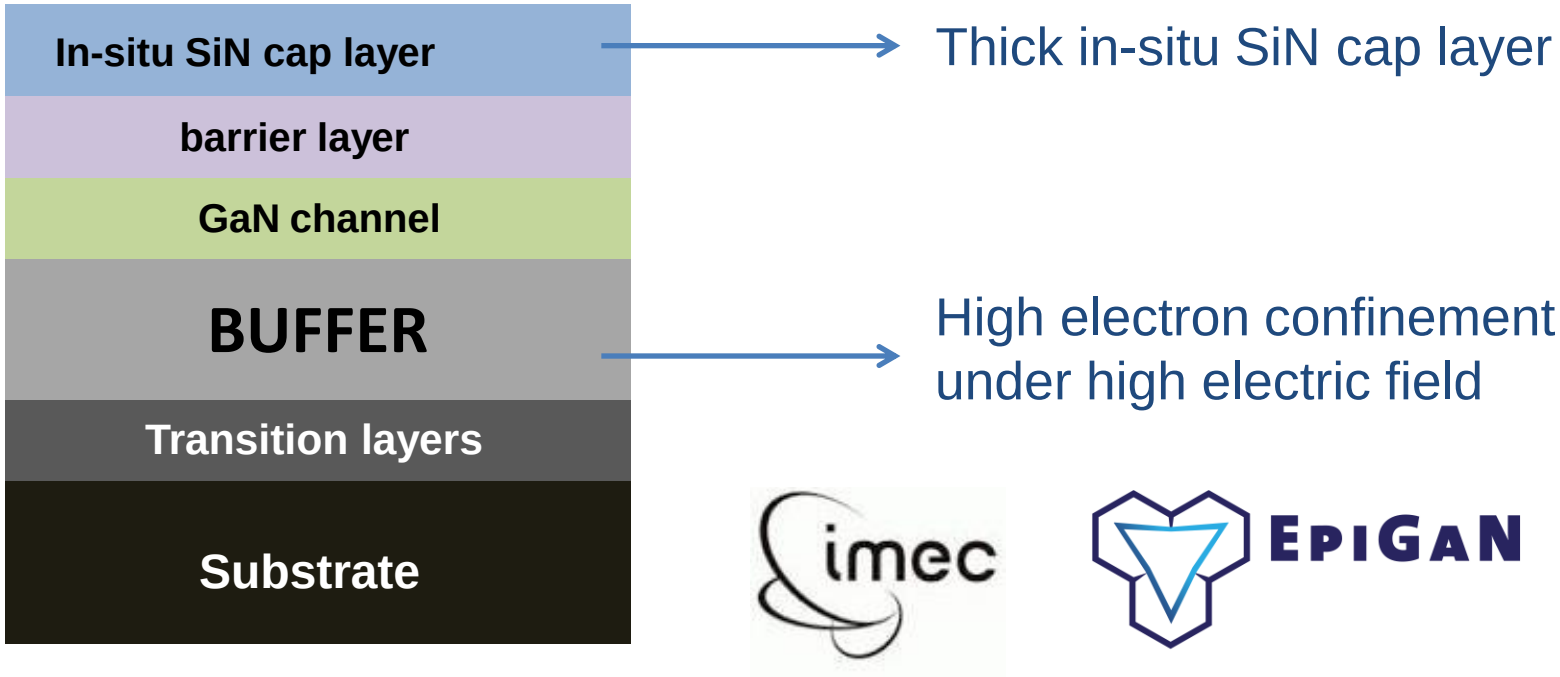
Much higher current density and voltage operation



Inherent surface charges causing 2DEG depletion and degradation of performances and/or device reliability

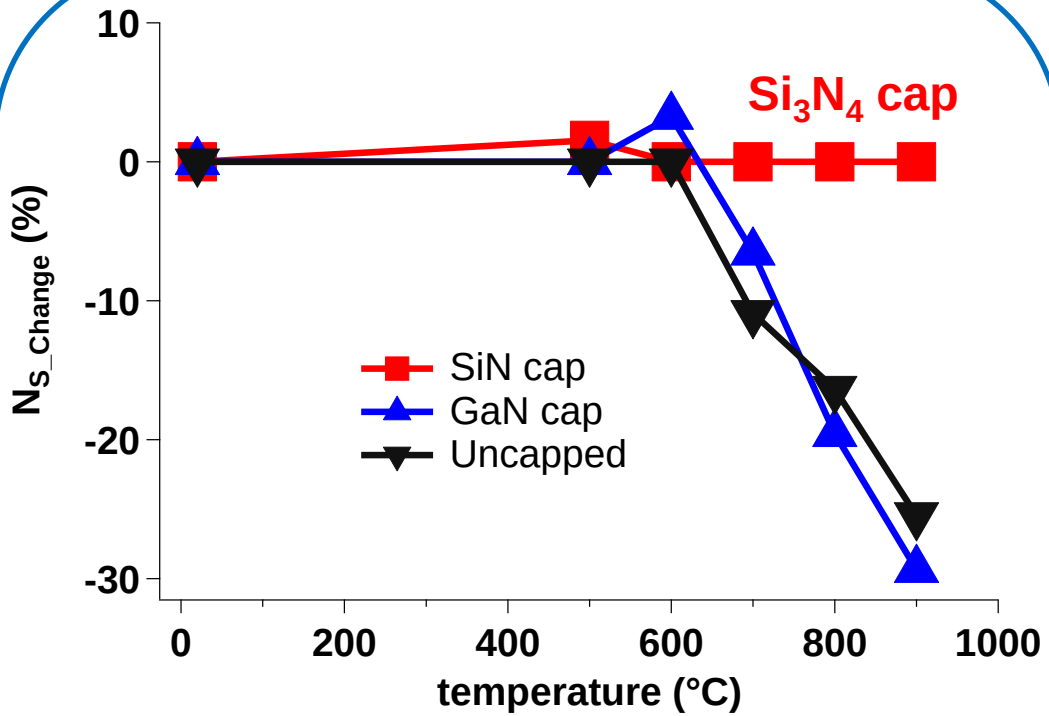


Device technology

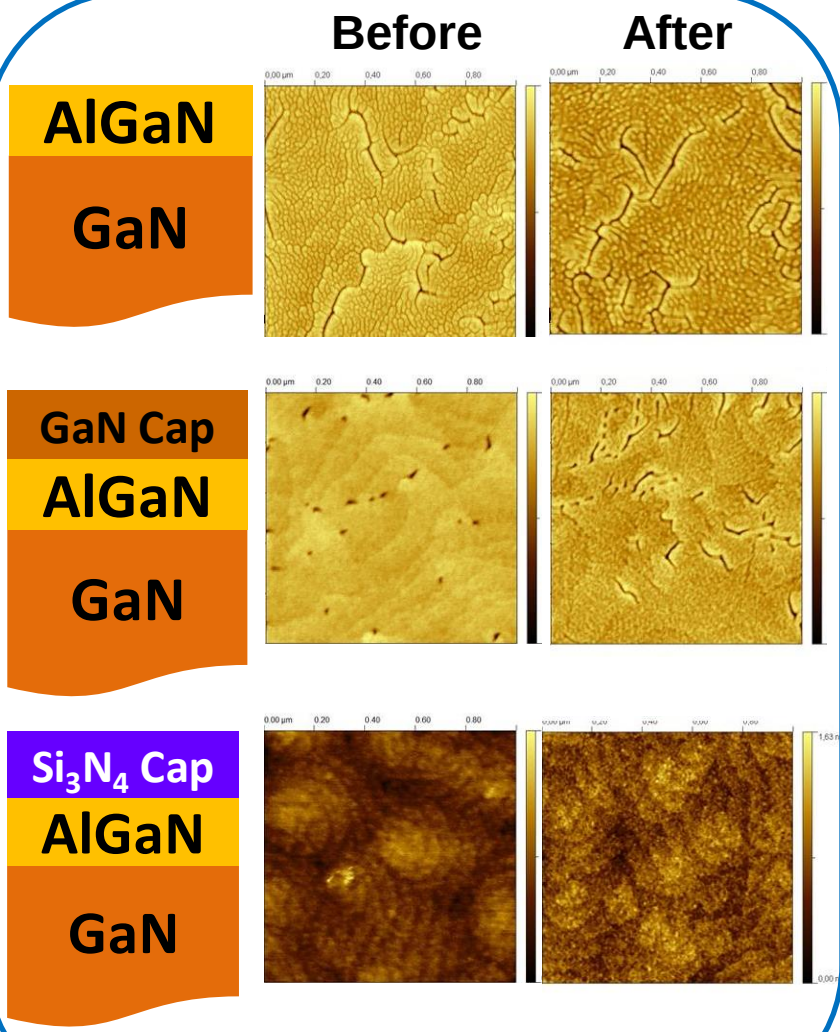


- Buffer layers specifically designed to enhance the electron confinement while avoiding deep traps
- Thick SiN cap layer used to improve the device robustness, especially to avoid gate leakage current increase after full passivation

Benefit of in-situ SiN cap layer



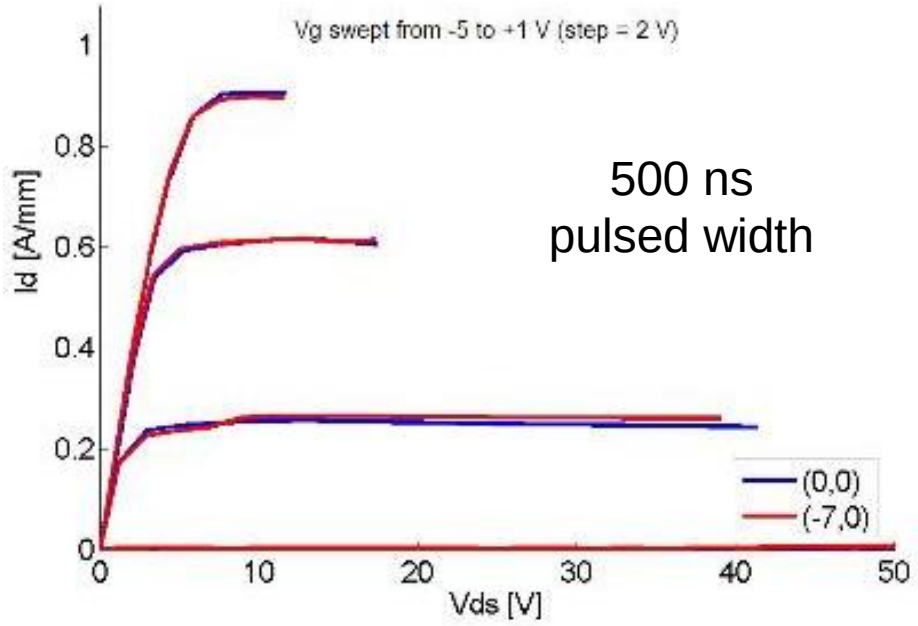
EXPERIMENT : The temperature was ramped up in vacuum to 900°C using a step of 100°C for 30 min. After each step Hall measurement was performed at RT.



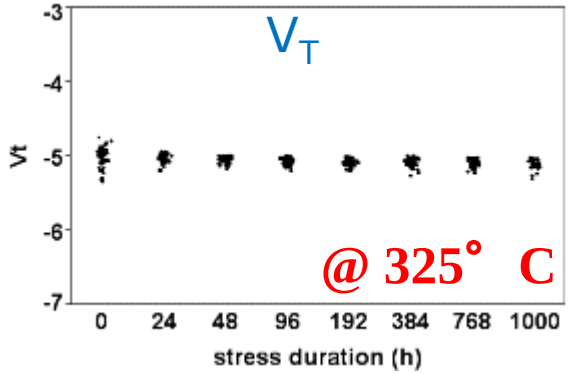
Benefit of in-situ SiN cap layer

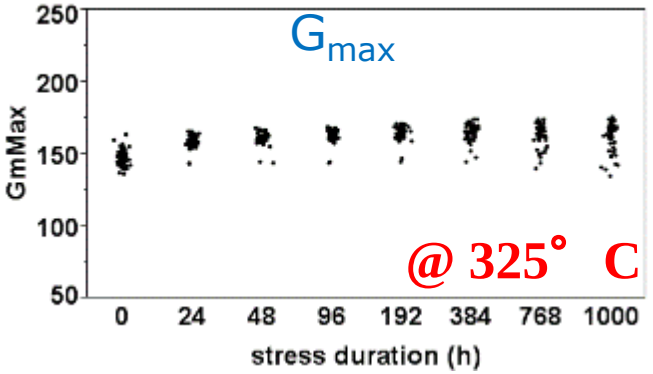
Thick in-situ SiN = key parameter for low dispersion and high stability

0.5 µm AlGaN/GaN-on-silicon technology



500 ns
pulsed width

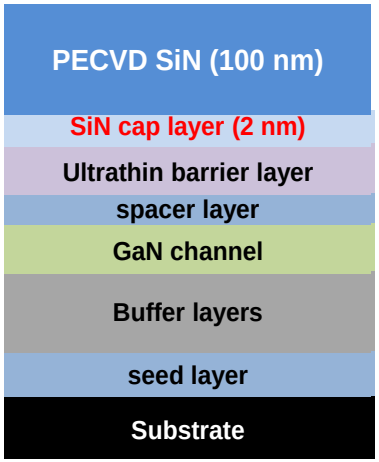


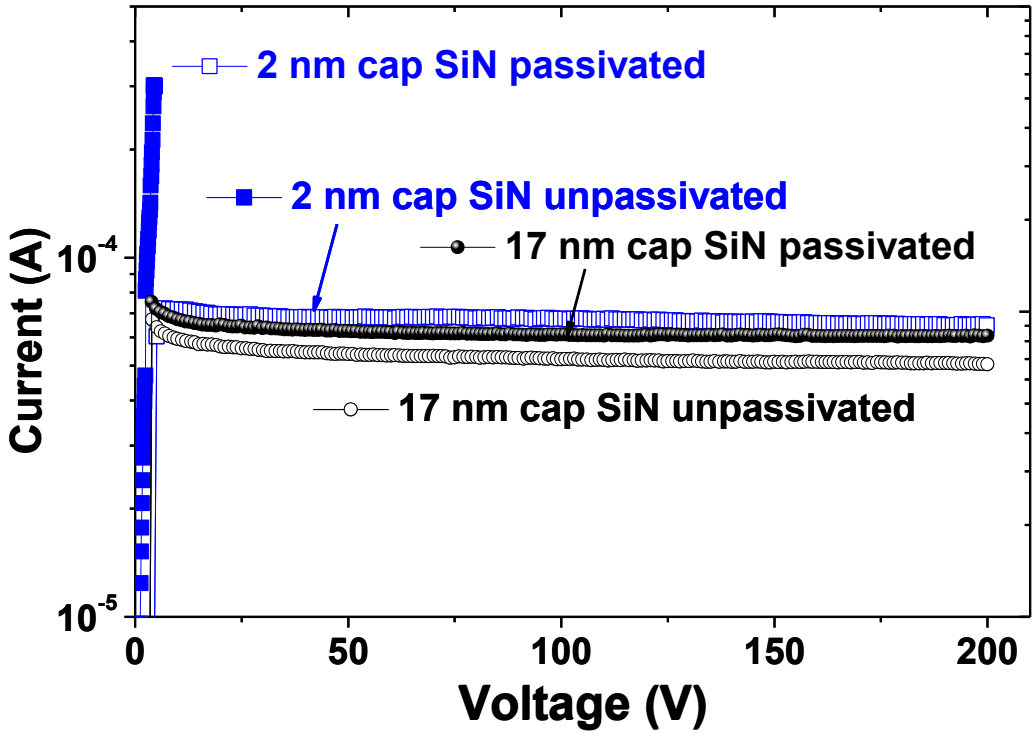


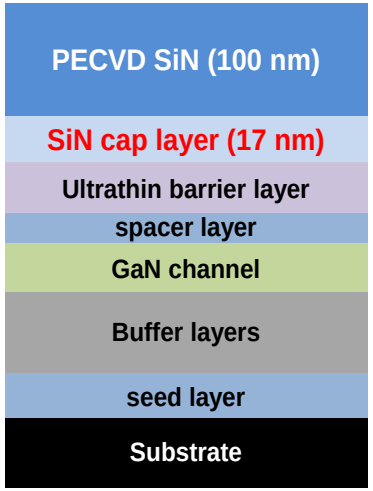
Low dispersion and High thermal stability above 300° C
(attributed to the in-situ SiN cap layer)

European Commission

60 µm circular diodes w and w/o 100 nm PECVD SiN passivation



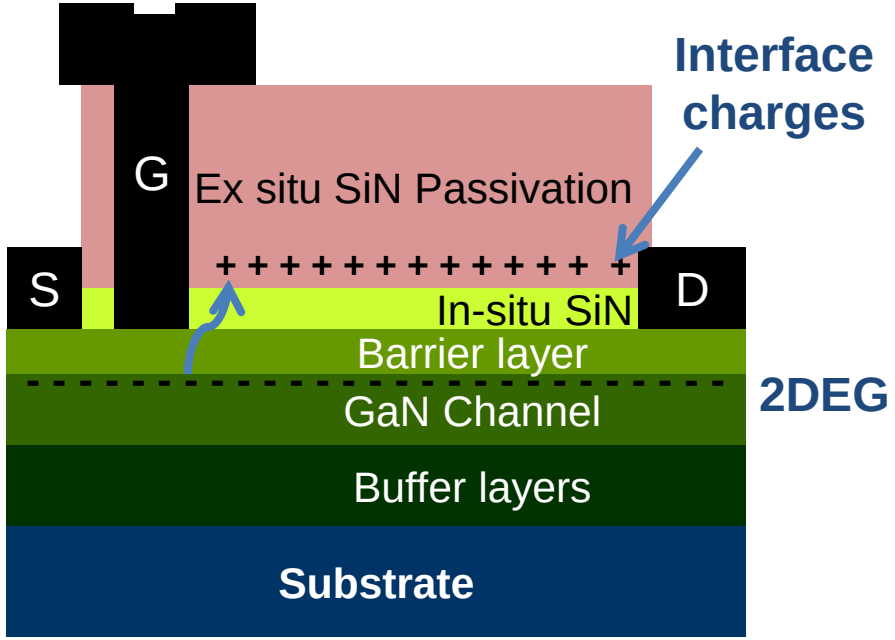




- after SiN PECVD passivation: Strong and systematic degradation of gate leakage and early breakdown when using thin SiN cap layer of couple of nm.
- Almost no degradation of gate leakage when using thicker SiN cap layer.

Proposed leakage current mechanism after full passivation

Electron injection at the MOCVD SiN / PECVD SiN interface under high electric field creating a conducting path at this location



A critical in-situ SiN cap layer thickness is needed to prevent the electron injection under high electric field

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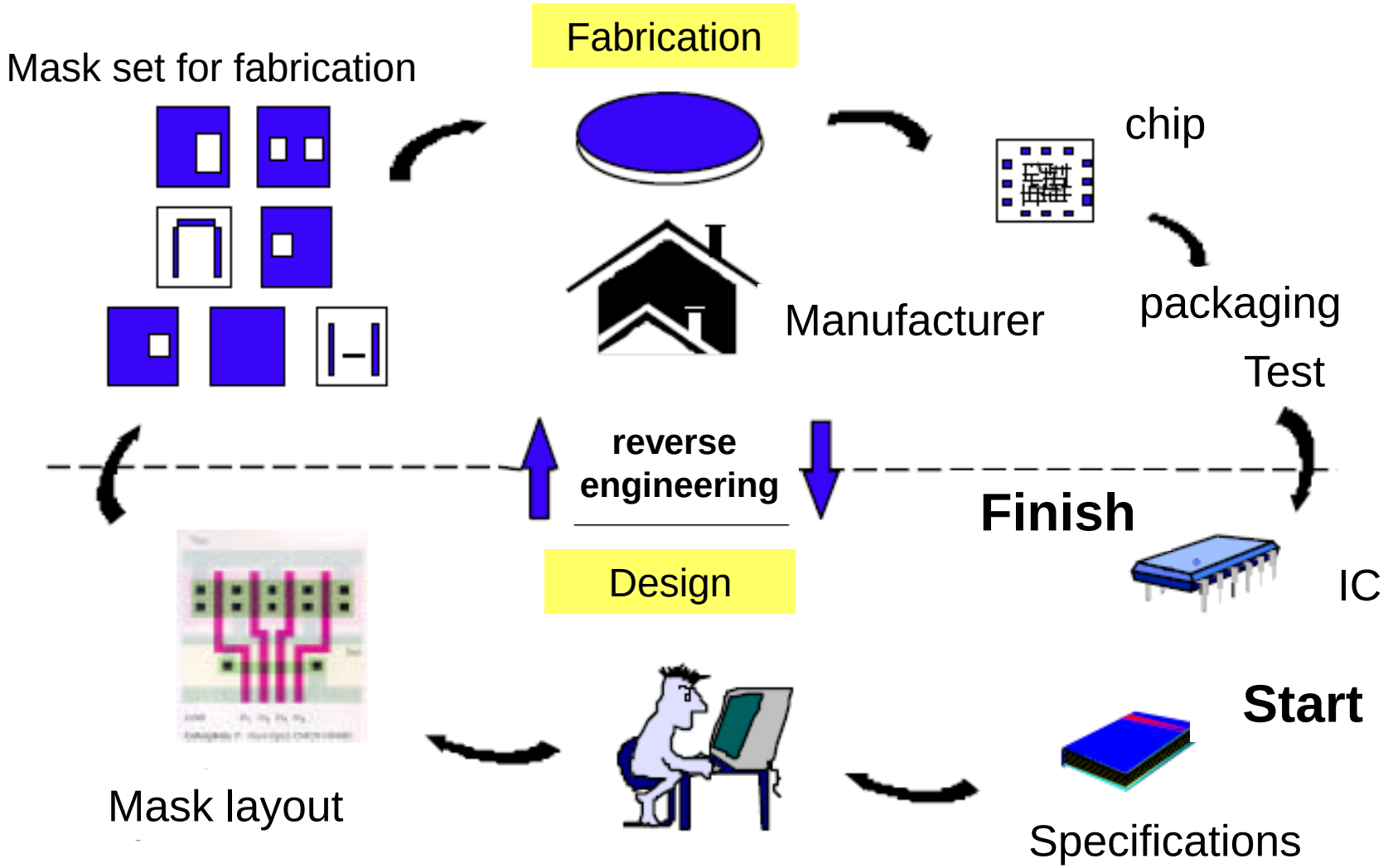
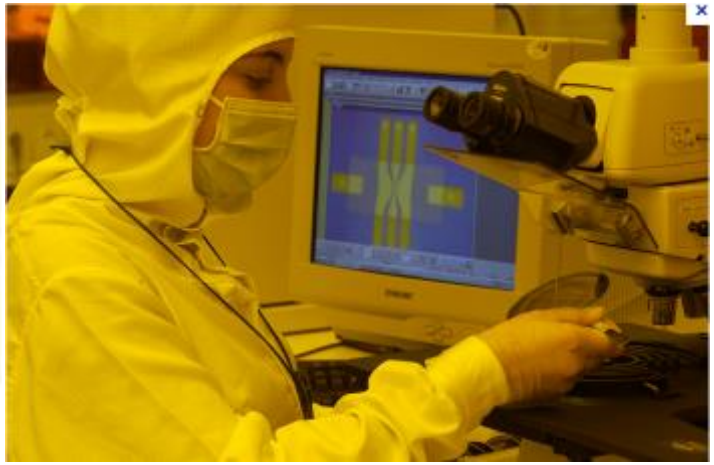
Design and fabrication of power devices



Cleanroom: fully controlled environment



- Controlled level of contamination, humidity, temperature, pressure, chemicals etc.
- 100 000 to 1 million times less particles than outside
- Personnel working in cleanrooms undergo extensive training in contamination. They enter and exit the cleanroom through airlocks, air showers. They must wear special clothing designed to trap contaminants that are naturally generated by skin and the body (boots, shoes, coveralls, face masks, gloves, hoods, and shoe covers)

Cleanroom: fully controlled environment

Cleanrooms are classified by how clean the air is

	particules /m³					
Classe	0,1 µm	0,2 µm	0,3 µm	0,5 µm	1 µm	5 µm
ISO 1	10	2	0	0	0	0
ISO 2	100	24	10	4	0	0
ISO 3	1 000	237	102	35	8	0
ISO 4	10 000	2 370	1 020	352	83	0
ISO 5	100 000	23 700	10 200	3 520	832	29
ISO 6	1 000 000	237 000	102 000	35 200	8 320	293
ISO 7	∞	∞	∞	352 000	83 200	2 930
ISO 8	∞	∞	∞	3 520 000	832 000	29 300
ISO 9	∞	∞	∞	35 200 000	8 320 000	293 000

Norme Iso146441

Classe ISO 3 = Classe 1
Classe ISO 4 = Classe 10
Classe ISO 5 = Classe 100
Classe ISO 6 = Classe 1000
Classe ISO 7 = Classe 10000
Classe ISO 8 = Classe 100000

EU standards

Foundry ONSEMI → No human presence ! Automation of all technological steps

IEMN → Manual operators Allows to achieve demonstrators / prototypes in small quantity

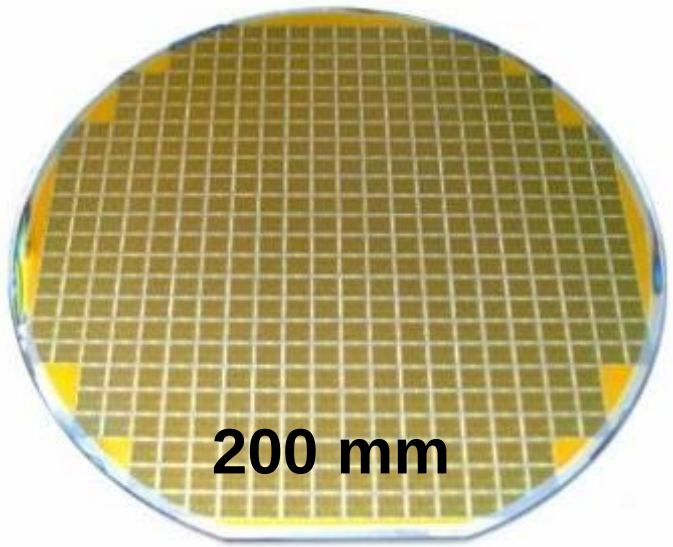
Cleanroom tour: Triquint (GaN RF manufacturer)

Device fabrication techniques

Today, GaN-on-Si power devices are fabricated on wafers up to 8-inch, which allows generating hundreds of devices simultaneously

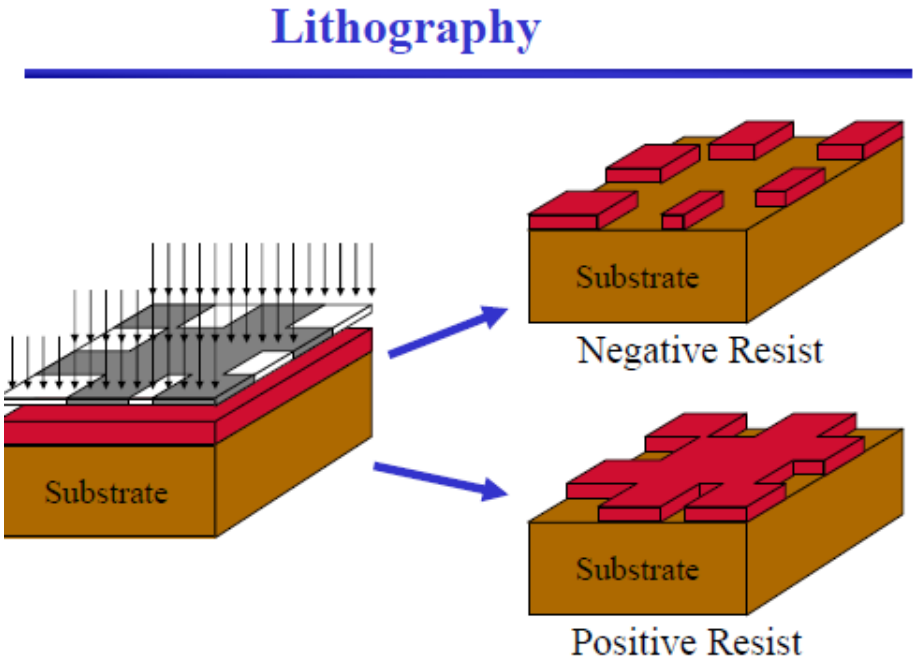
Basic processing steps:

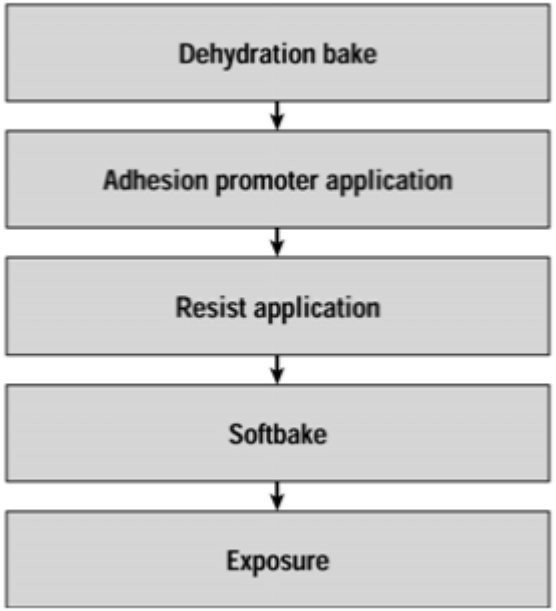
- Wet cleans
- Photolithography
- Metal deposition
- Thermal treatments
- Physical vapor deposition (PVD)
- Wet and dry etching
- Ion implantation
- Wafer back-grinding (thinning)
- Chemical-mechanical planarization
- Electroplating
- Wafer dicing and mounting
- Die bonding



Photolithography (optical)

- Enables to pattern parts of a thin film or the bulk of a substrate
- Uses light to transfer a geometric pattern from a photomask to a light-sensitive chemical "photoresist“ with a resolution of 0.5 to 1 µm
- Chemical treatments reveals the exposure pattern, or enables deposition of a new material in the desired pattern





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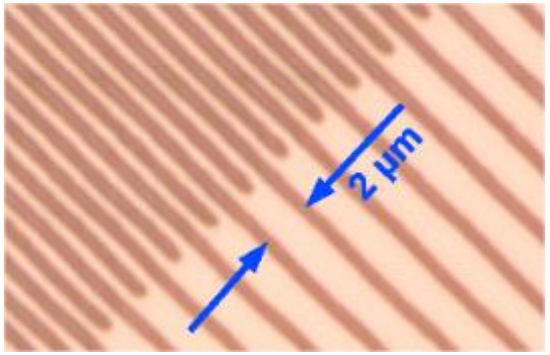
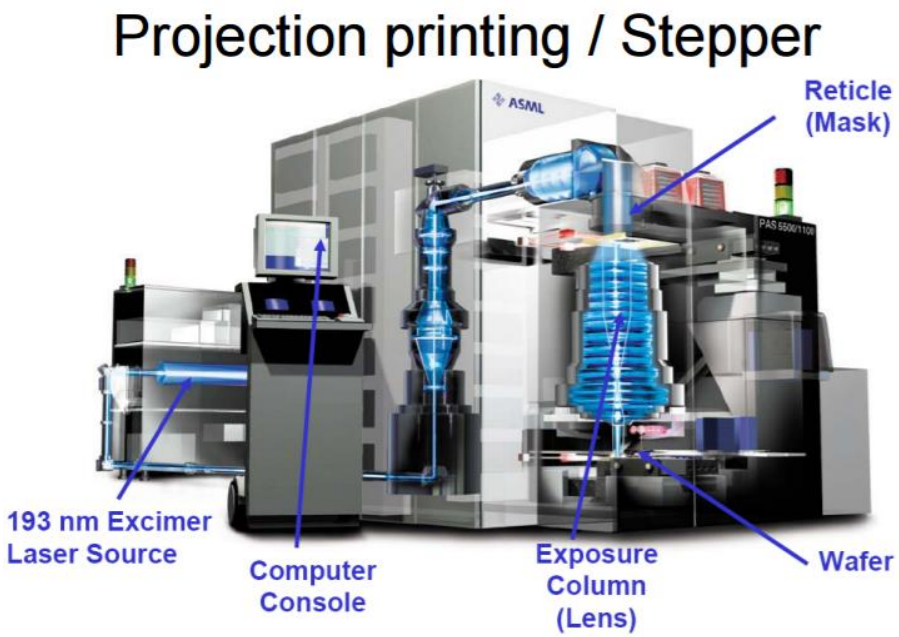


Photolithography (stepper)

step-and-repeat camera

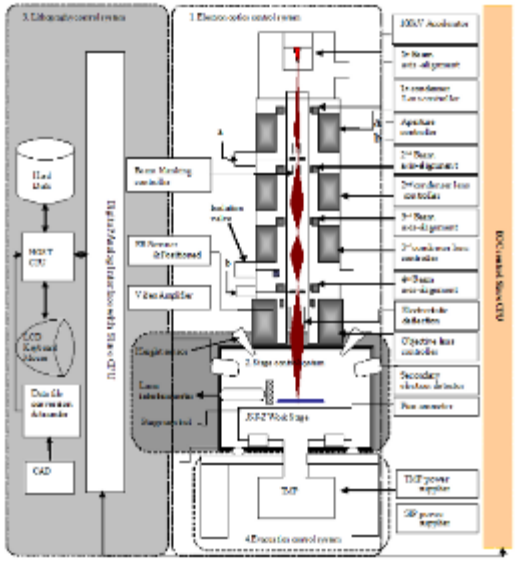
used in the manufacture of integrated circuits

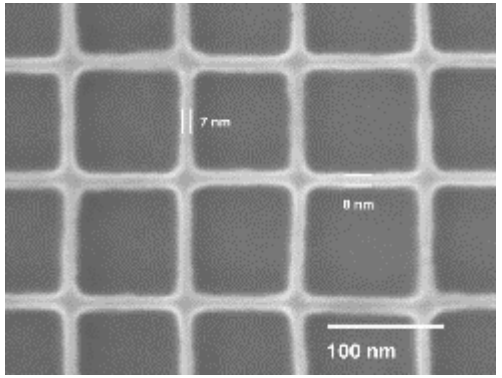
Use alignment marks to align each reticles with a resolution down to hundreds of nm

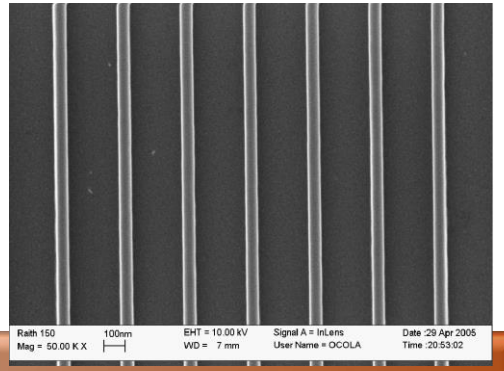


Electron-beam lithography

- Scanning a focused beam of electrons to draw custom shapes on a surface covered with an electron-sensitive film
- No mask required !
- The primary advantage of electron-beam lithography is that it can draw custom patterns (direct-write) with sub-10 nm resolution
- High resolution BUT low throughput limiting its usage to photomask fabrication, low-volume production of semiconductor devices, and research and development

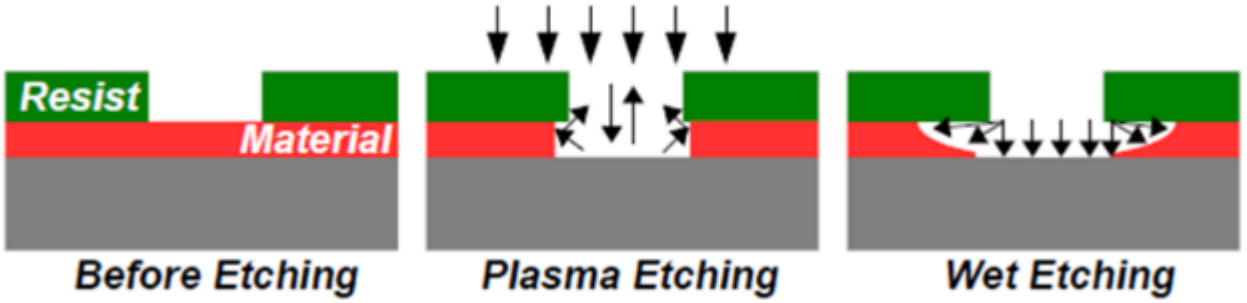






Etching

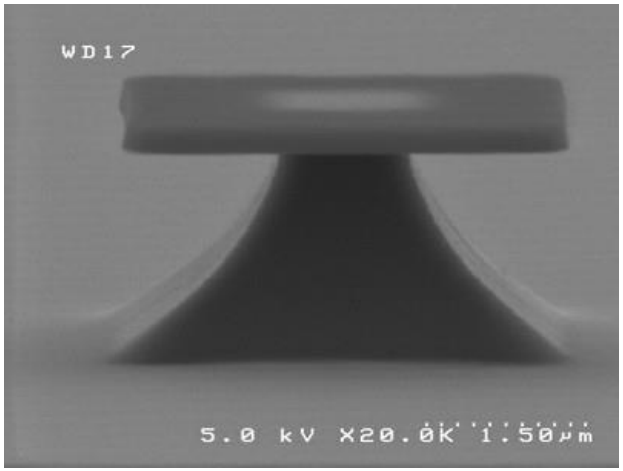
- Important factors:
  - Uniformity
  - Etch rate and control
  - Etch selectivity



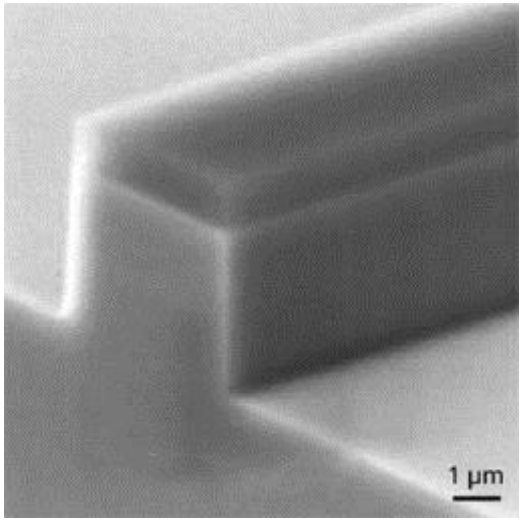
- Advantages and Disadvantages of Dry (plasma) and Wet etching
  - ✓ Wet etching provides low damage, high selectivity, simple equipment BUT generally isotropic (etching in all directions). No efficient wet etching solutions for GaN
  - ✓ Dry etching: lower cost, anisotropic (1 direction). However, plasma damages and re-deposition of no volatile compounds have to be overcome when used in the active parts of devices

Etching

Isotropic silicon wet etching



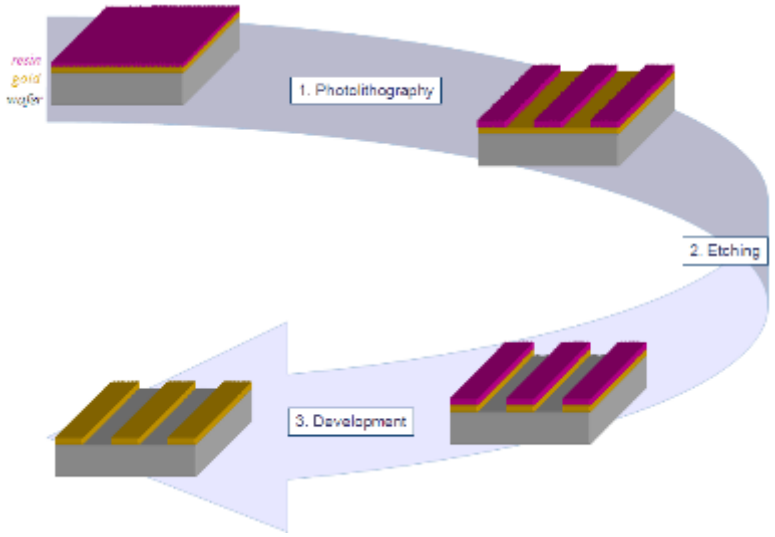
GaN Dry Etching Process



Metal deposition

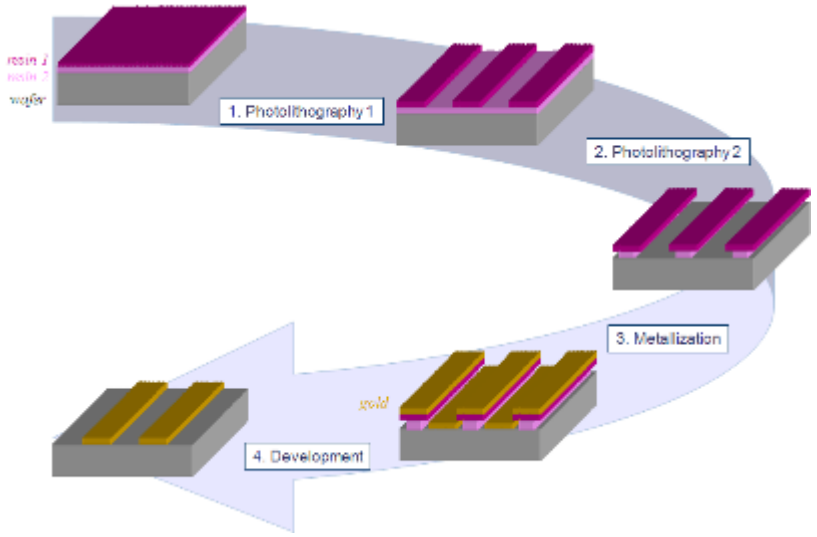
Two techniques to obtain the patterns by metallization :

Etching



1. Metallization of the substrate
2. Photolithography to define the patterns with a mask
3. Etching the metal in the open areas
4. Remove the resist with solvent

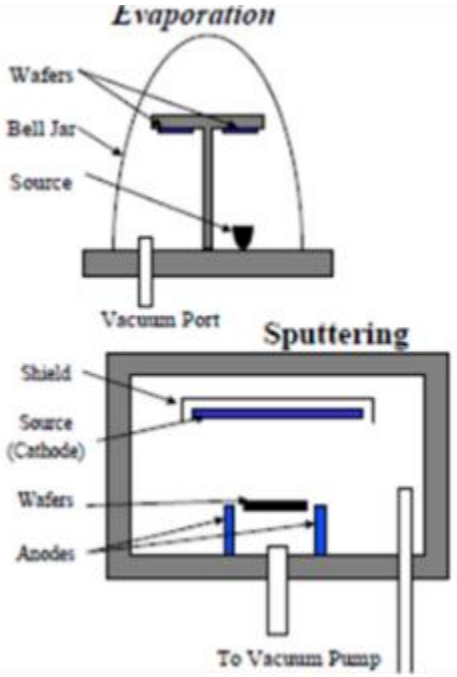
Lift-off



1. Bilayer resist
2. Photolithography to define the patterns with a mask
3. Exposure in order to open the areas and creation of an undercut due to difference in resist sensivity.
4. Metal deposition that will lift-off on top of the resists following removal with solvent

Metal deposition

- Primary Metal Deposition Techniques
  - Sputtering
  - Evaporation (E-beam)
  - Electroplating
- Commonly used metals
  - Adhesion layers: Cr and Ti
  - Aluminium
  - Gold
  - Copper
  - Nickel



Evaporation:

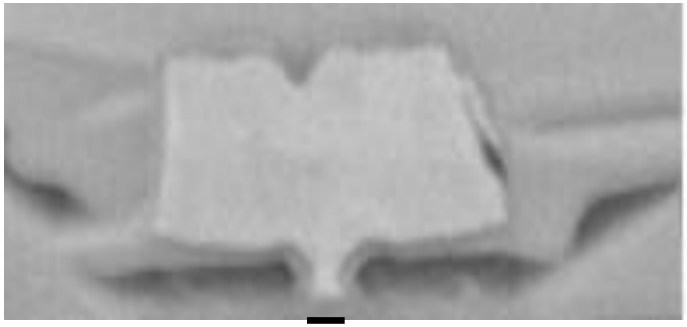
- Metal is melted in vacuum and evaporated to the sample through vacuum.
- Very common in III-V semiconductors, ideal for lift-off
- Deposition rate depends on pressure, temperature and atomic mass of species.

Sputter deposition:

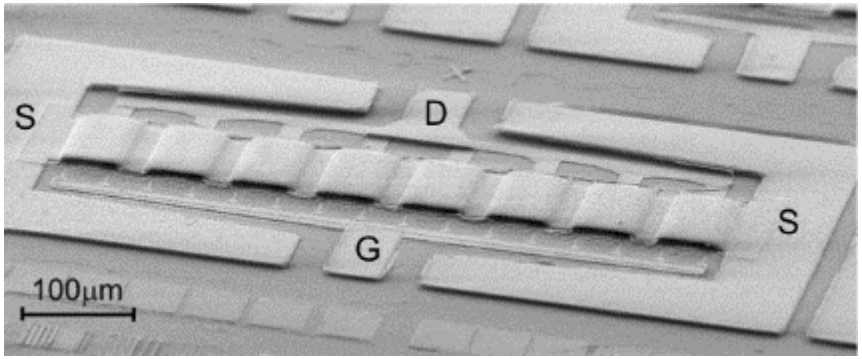
- Physical vapor deposition consisting in ejecting material from a "target" onto a "substrate“.
- The sputtering gas is often an inert gas such as argon.
- Better step coverage than evaporation

Metal deposition

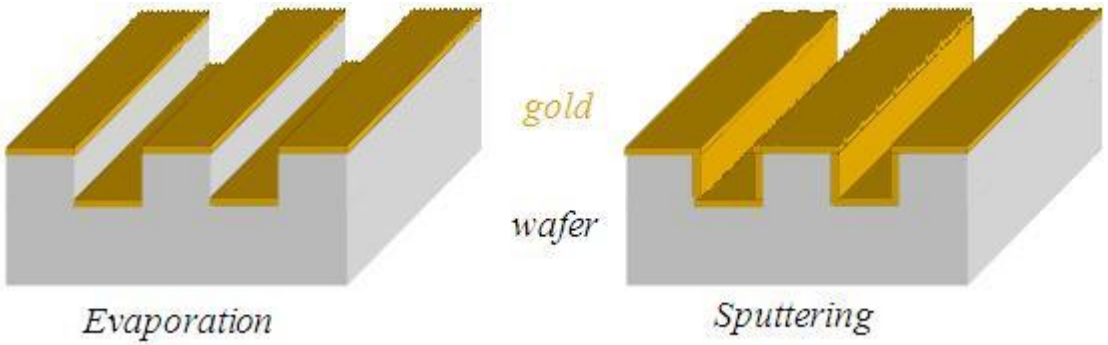
Evaporation tool



60 nm



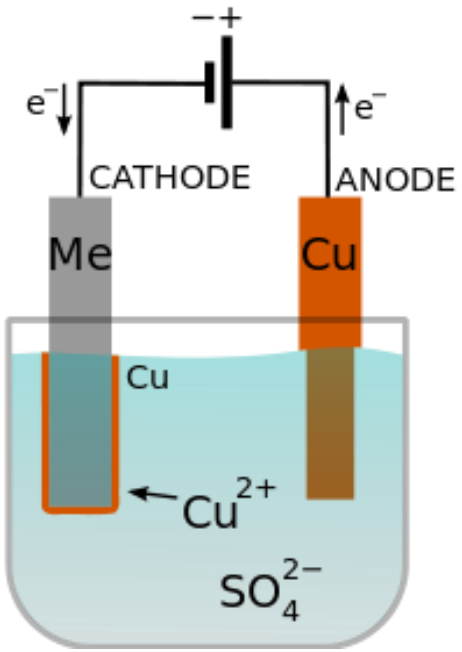
Sputtering tool



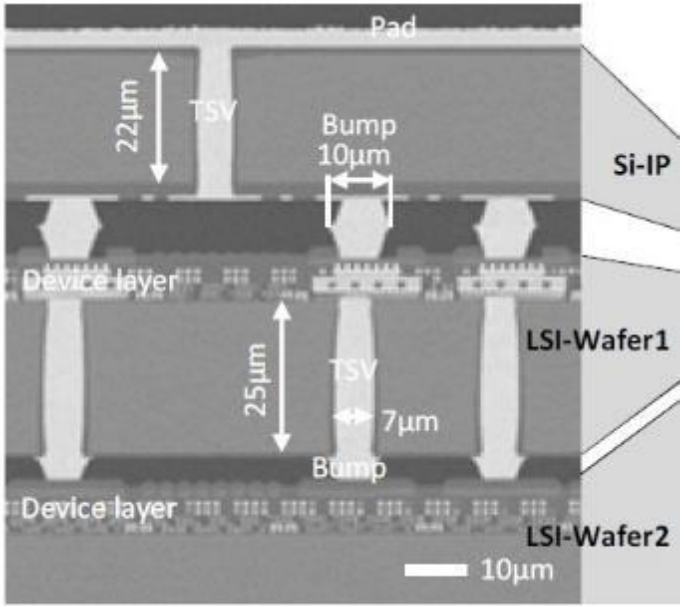
Metal deposition

Electro-plating:

- Used for thick metal deposition several µm to several tenths of µm
- Uses electric current to reduce dissolved metal cations so that they form a thin coherent metal coating on a conductive surface. Therefore, a seed layer (metal) is used on the area where plating is desired.

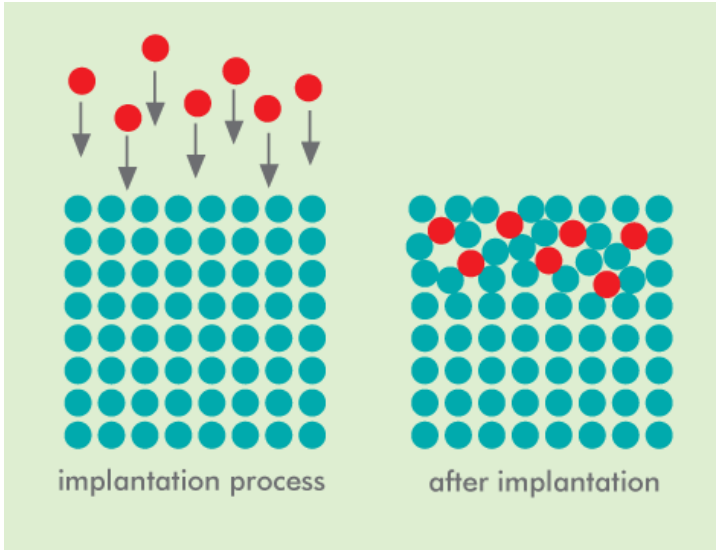


Cu interconnects
through via holes

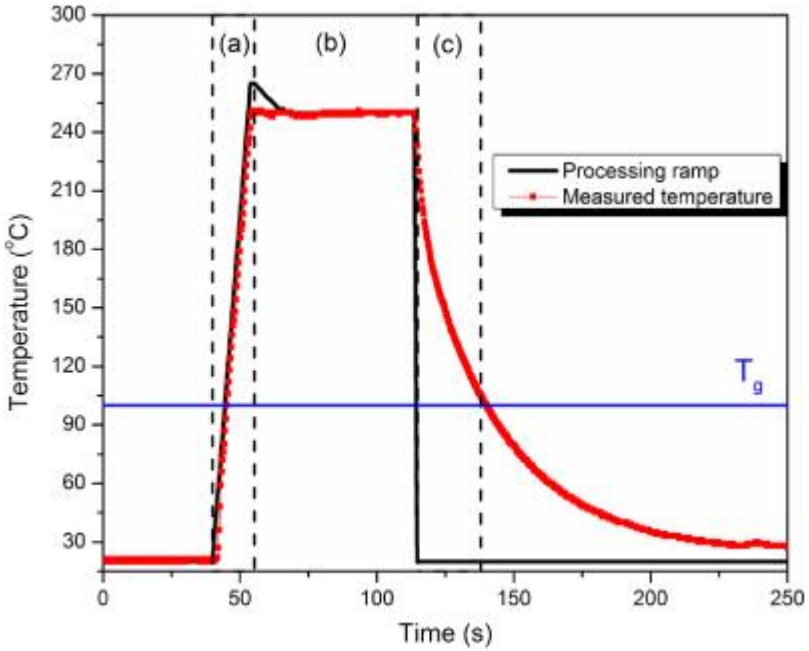


Ion implantation

- Ions of a material are accelerated in an electrical field and impacted into a solid.
- Process used to change the physical, chemical, or electrical properties of the solid.
- The energy of the ions (up to several hundreds keV), as well as the ion species and the composition of the target determine the depth of penetration of the ions in the solid
- Used for instance:
  - ✓ Preparing SOI substrate (high dose oxygen implant is converted to silicon oxide
  - ✓ Doping of semiconductors
  - ✓ Device isolation



Rapid Thermal Annealing



- Semiconductor manufacturing process which heats wafers to high temperatures (up to 1000° C) on a timescale of several seconds or less
- Used for formation of ohmic contacts

- Temperature range :
  - 140 à 1200° C
- High vacuum

PE and LP – CVD deposition

Plasma Enhanced – Low pressure Chemical vapor deposition

SiN and SiO_2 deposition highly in GaN device fabrication for passivation or as sacrificial layers

- Quality of deposition
  - Composition of the film
  - Contamination levels
  - Defect density
    - Pinholes, step coverage
  - Mechanical properties
    - Stress
  - Electrical properties
    - Conductivity
  - Optical properties
    - Reflectivity

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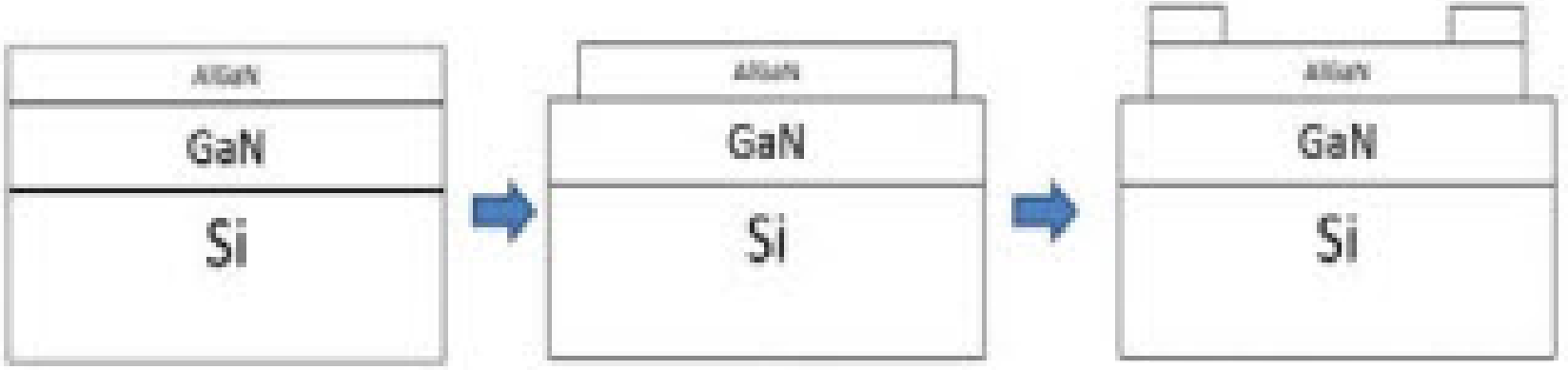
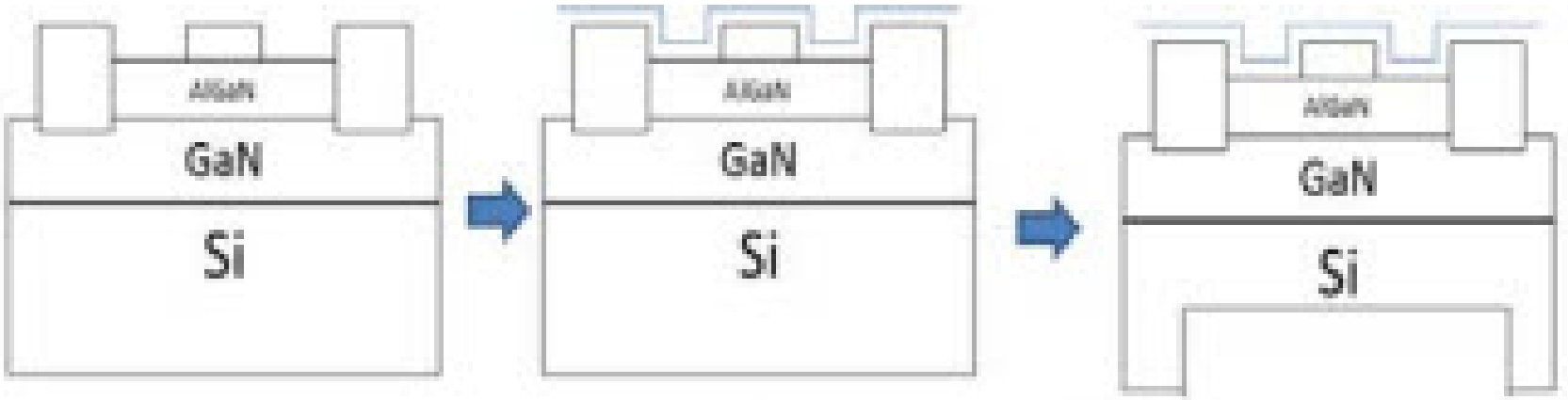
Basic process flow to fabricate the GaN devices

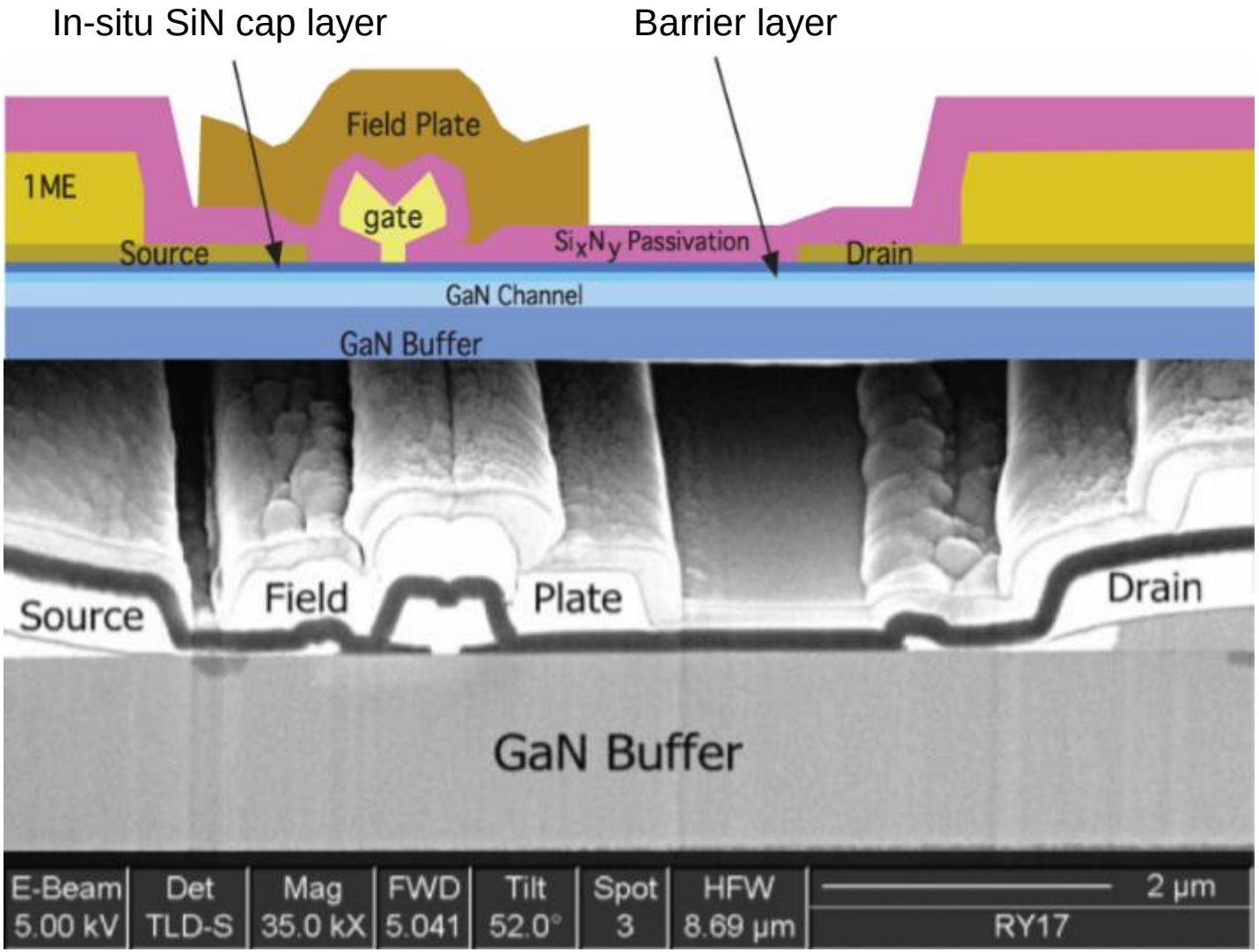


Starting wafer sample **Isolation** **Ohmic metal deposition and RTA**



Gate deposition **Passivation** **Backside pattern and etch**

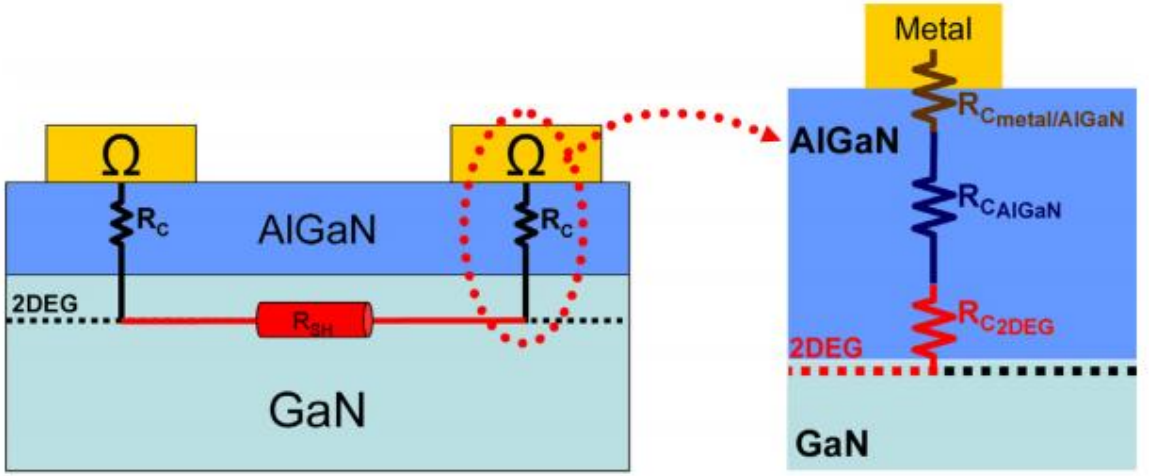
GaN device cross section



Ohmic contacts

Ohmic contacts are a fundamental building block of GaN power devices

The ohmic contact resistances must be as low as possible in order to minimize the device specific on-resistance (Ron) and, hence, the power losses of the system



Achieving good ohmic contacts in these materials is inherently difficult, due to the wide band gap (3.4 eV for GaN) which typically leads to Schottky barrier height values in the order of 1 eV on n-type and even of 2 eV on p-type material. Even more critical in AlxGa1-xN alloys with increased Al content

Ohmic contact formation

Lithography

↓

Surface treatment or etching

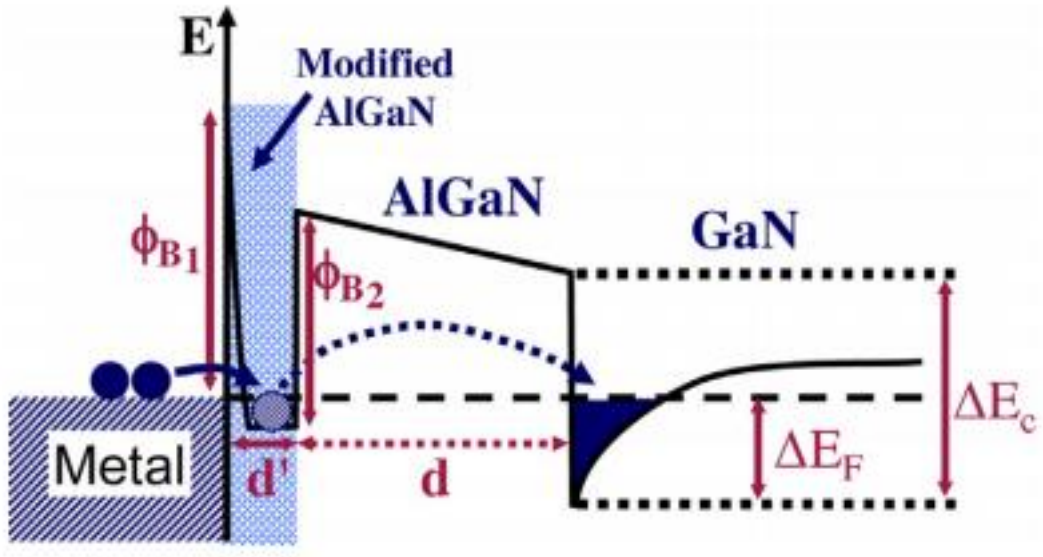
↓

Metal deposition (typically Ti/Al based for GaN heterostructures)

↓

Rapid flash annealing

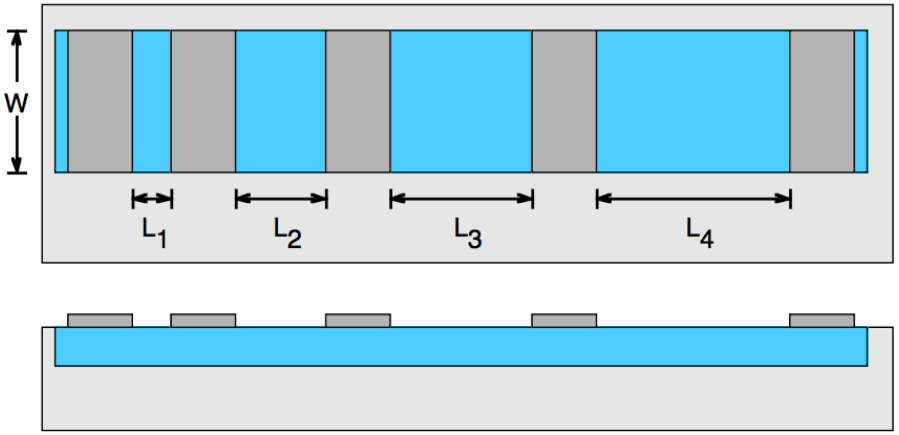
Schematic band diagram to describe the mechanism of current transport in ohmic contacts to AlGaN/GaN heterostructures



The model assumes the presence of the modified surface subsequent to the HT annealing. The electrons can easily tunnel through this very thin barrier. The second barrier is the one that the electrons injected in the AlGaN layer have to overcome in order to reach the 2DEG at the AlGaN/GaN interface.

How to measure the ohmic contact resistances ?

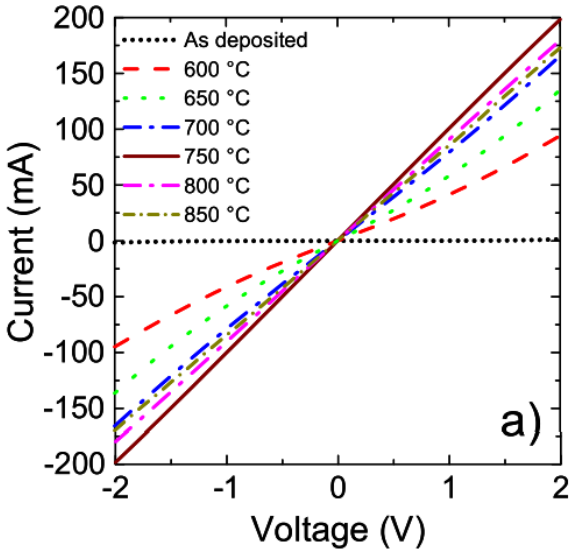
Transfer Length Measurement extraction

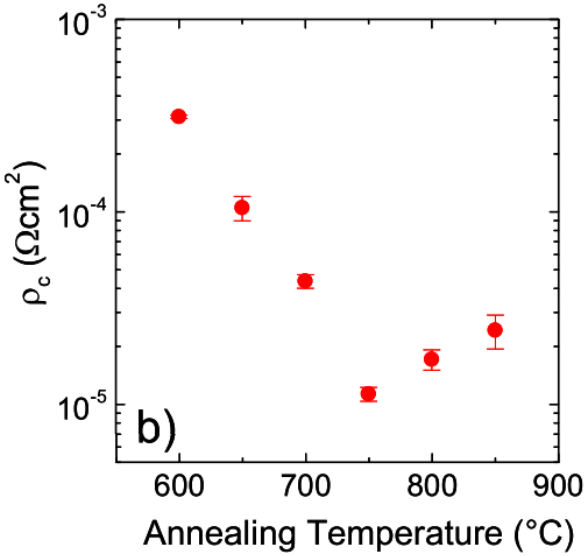


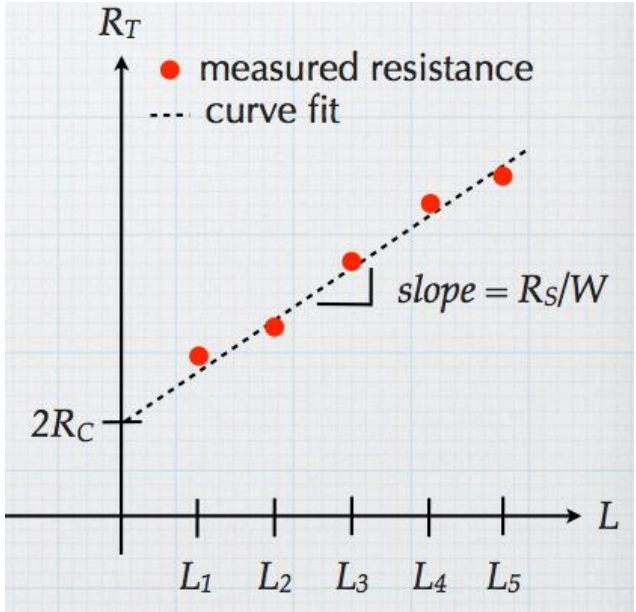
$$R_T = \cancel{2}R_m + 2R_C + R_{semi}$$

$$R_{semi} = R_S \frac{L}{W}$$

$$R_T = \frac{R_S}{W} L + 2R_C$$



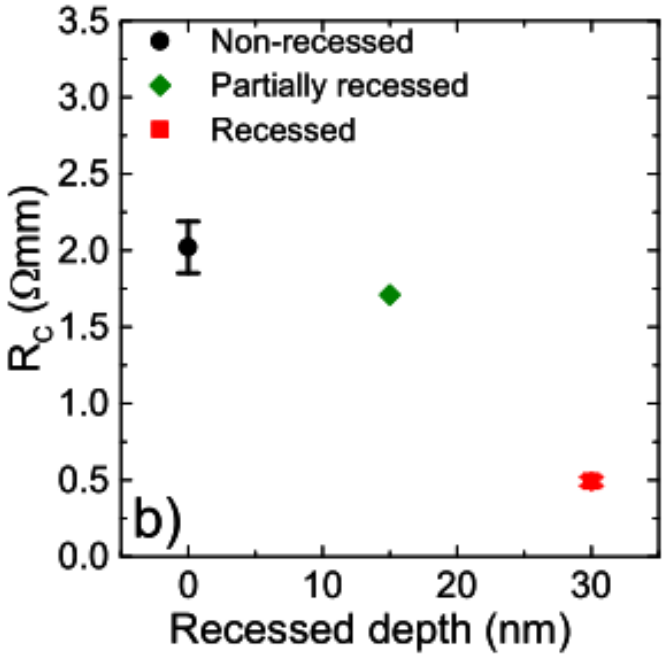




Au-free ohmic contacts

Most common solutions for ohmic contacts, both to GaN and AlGaN/GaN heterostructures, is based on annealed Ti/Al/X/Au multilayers providing R_C as low as 0.2 Ω.mm

Au cap layer enables to prevent surface oxidation and to improve the contact resistance by the formation of conductive phases inside the entire metal stack



However, GaN power devices must be low cost and fully compatible with Si CMOS technology. Therefore, to avoid "cross-contaminations" in Si devices industry and reduce the overall manufacture cost of the HEMT devices, Au cannot be used

"recessed" Ti/Al/W Ohmic contacts to AlGaN/GaN heterostructures

H.-S. Lee, et al, IEEE Electron Device Lett. 32 (2011) 623

Device isolation

2 approaches commonly used to isolate GaN devices

Mesa:

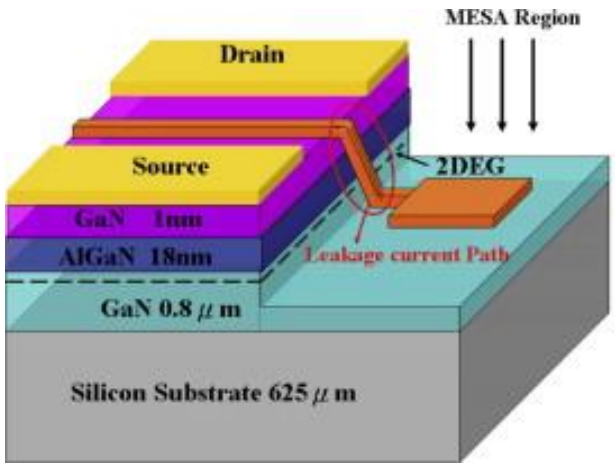
Dry etching in order to define device active regions

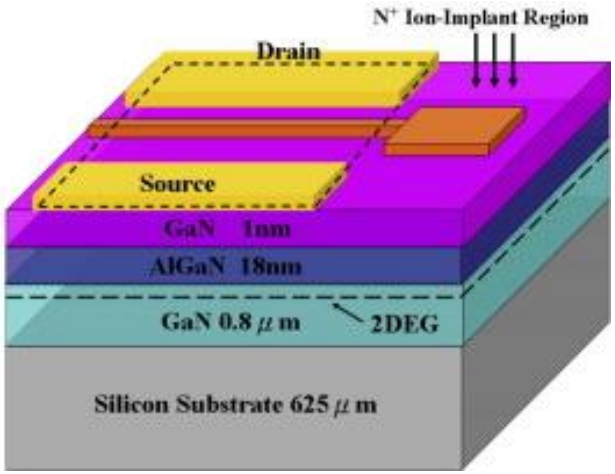
Mesa sidewalls can lead to increased gate leakage current and reduced breakdown voltage

Implantation:

Ion implantation in order to define device active regions

Planar surface, highly reproducible and stable

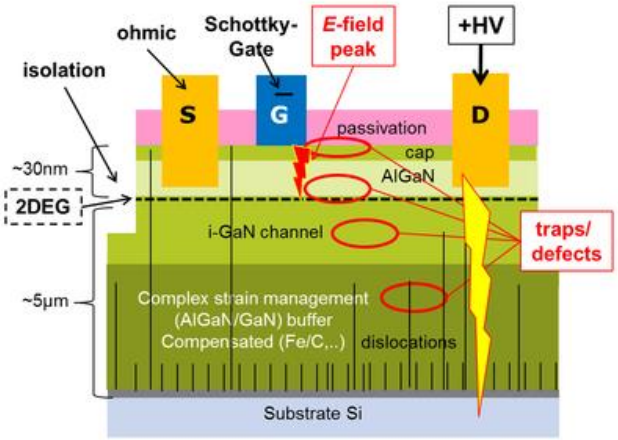




Gate module: various architectures

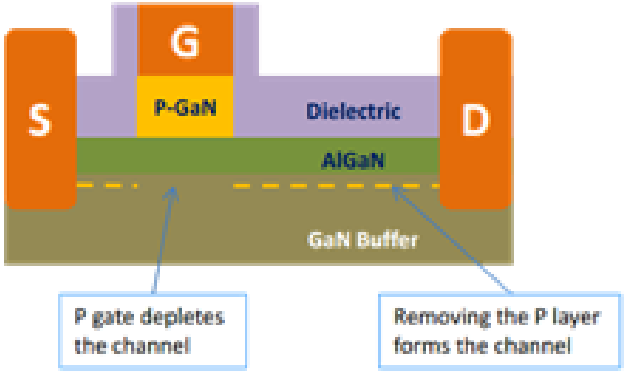
Normally-off desired for GaN power devices

Schottky contact



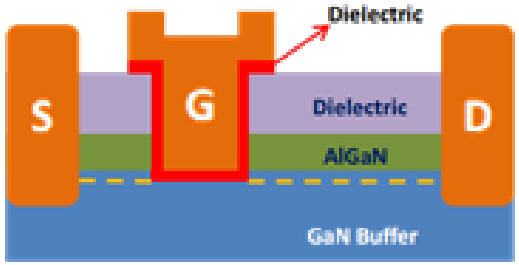
- High leakage current
- Reduced breakdown voltage
- Normally-on devices

Junction-gated HEMTs



- Low leakage current
- Single chip normally-off transistor
- Low threshold voltage

Channel etch-through MOSFET

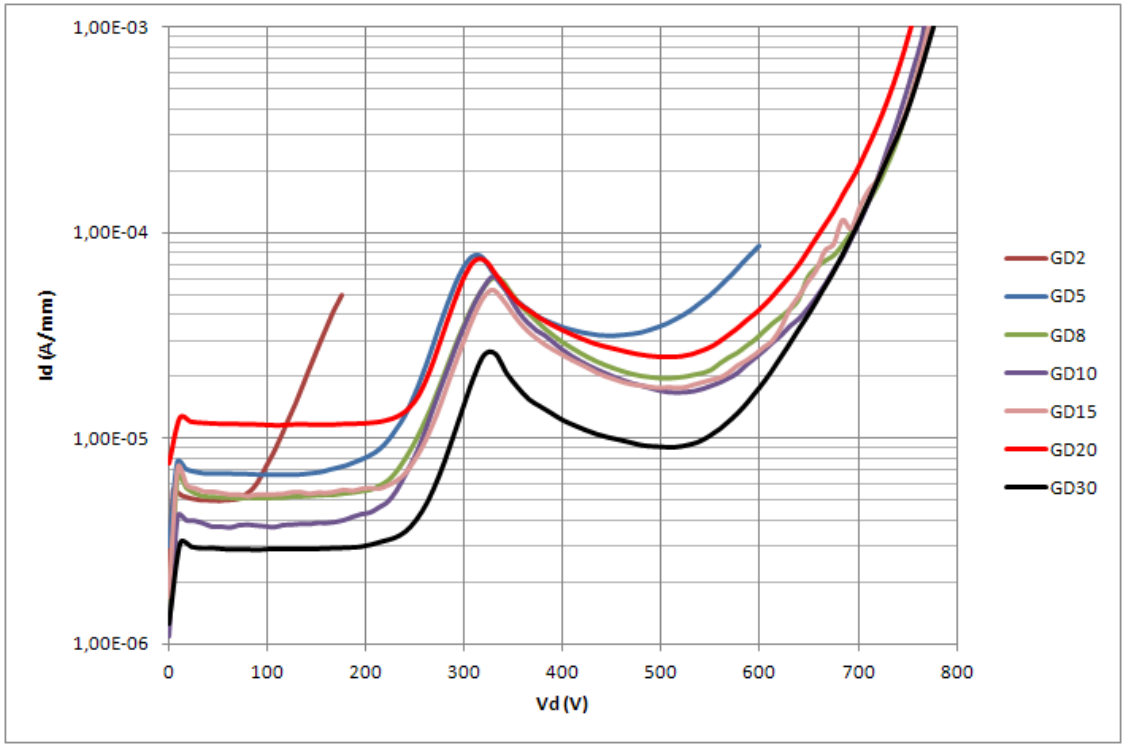


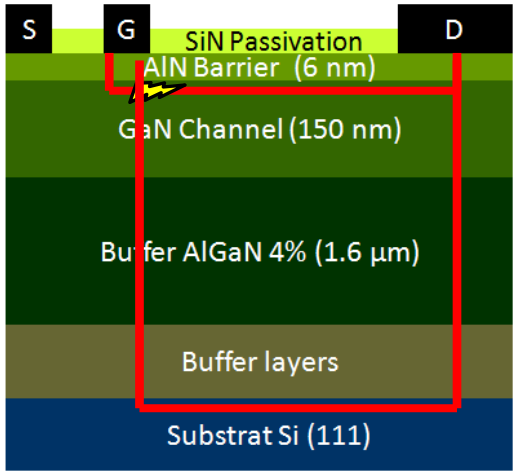
- Low leakage current
- Single chip normally-off transistor
- Device/dielectric not qualified

- Introduction
- Device design for high power devices
- Description of the device fabrication
  - Main processing techniques
  - Main technological bricks
- How to further push the breakdown limits of GaN-on-Si HEMTs
  - LSR approach developed within Inrel project
- Conclusion

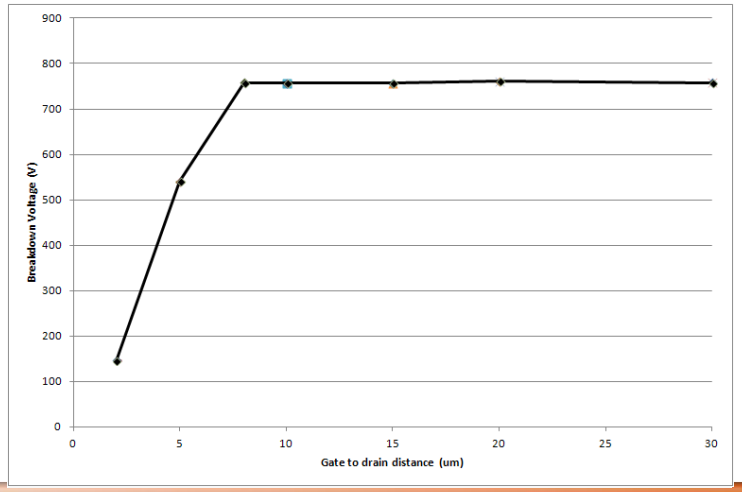
How to further push the limits of GaN power transistors by means of processing

Breakdown mechanism in GaN-on-silicon HEMTs

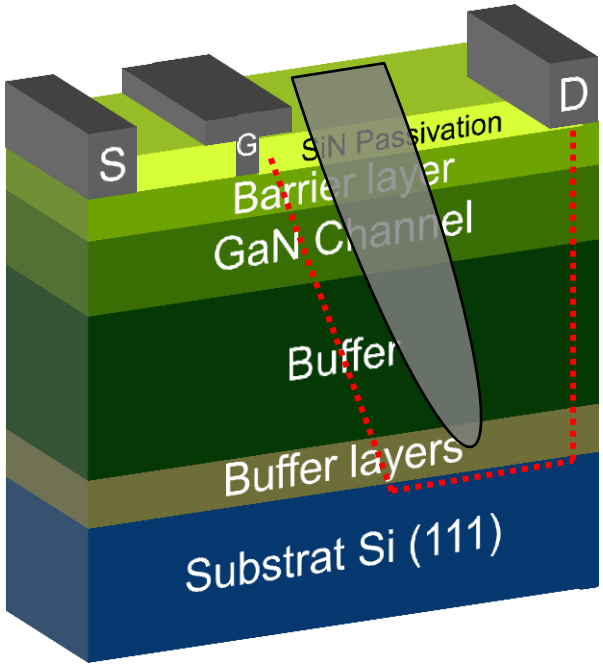




The breakdown saturation clearly shows that the silicon substrate is the limitation



How to further push the limits of GaN power transistors by means of processing



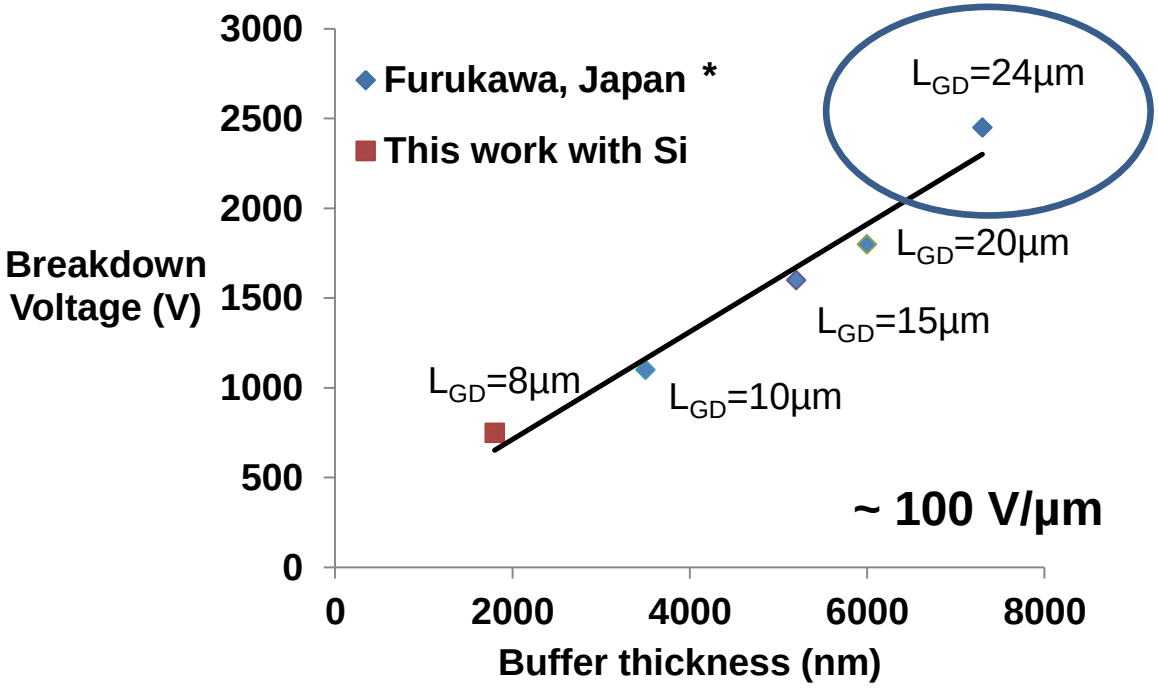
Thicker Buffer (> 6 µm)

Reliability issues

- **Higher defect density**
- **Higher strain**

Substrate removal

- Enable drastic increase of the BV
- No need of very thick buffer to achieve high BV



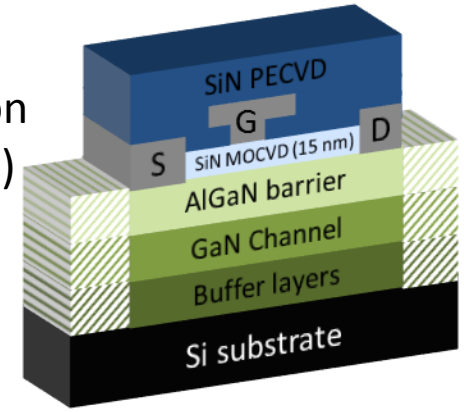
**N. Ikeda et al: in IEEE APEC 2010*

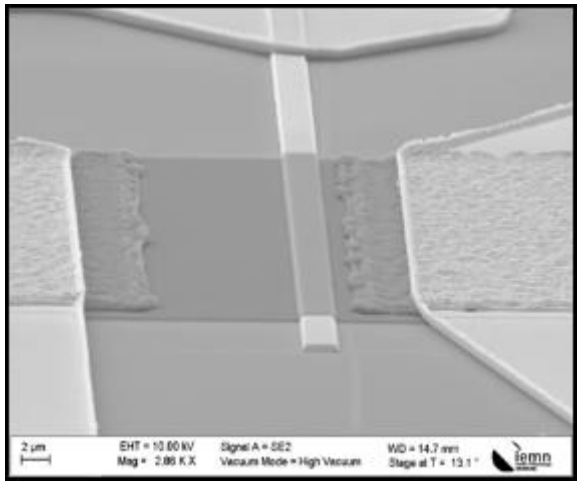
Device fabrication at IEMN within Inrel project

Process flow: front side

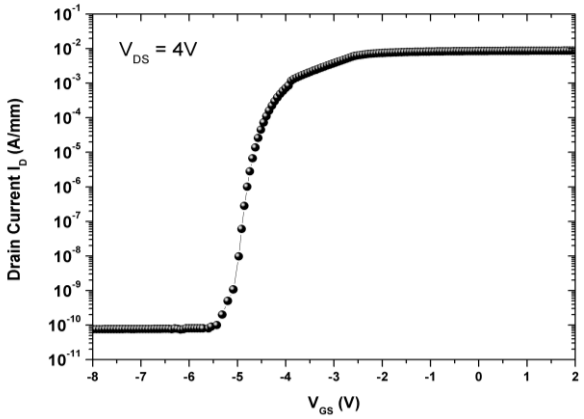
1. Ohmic contacts Ti/Al based

   R_C = 0.5 Ω.mm
2. Isolation by implantation
3. Gate module MIS configuration (MOCVD SiN as gate dielectric)
   - Lg: 2 µm, W = 50 µm
4. SiN PECVD Passivation
5. Interconnects

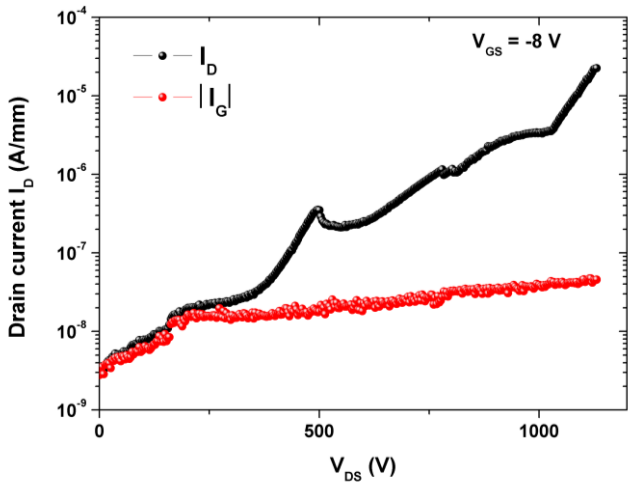




Front side SEM view of the GaN HEMT



Transfer characteristics I_D- V_G



Off-state characteristic of the GaN-on-Si HEMT with GD40

Typical blocking voltage about 1.2kV

Device fabrication at IEMN within Inrel project

Substrate removal on large area

Image of large membranes (about 2 cm)

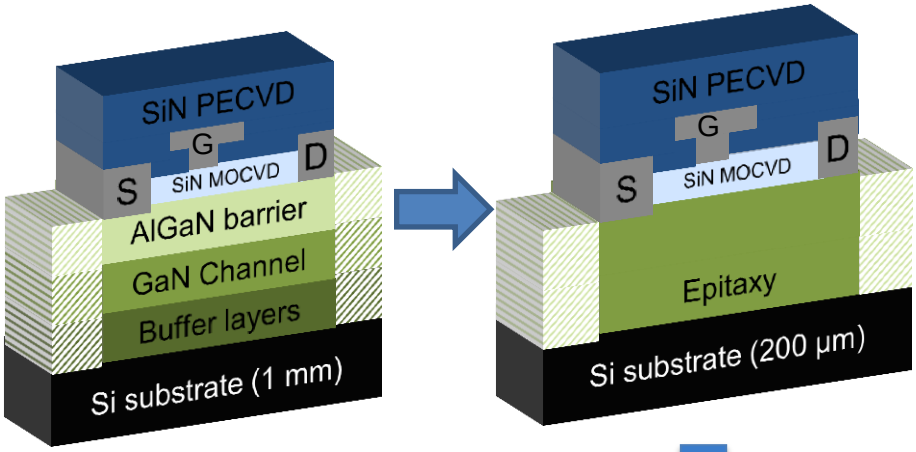
Complete breakage of the membrane due to significant strain

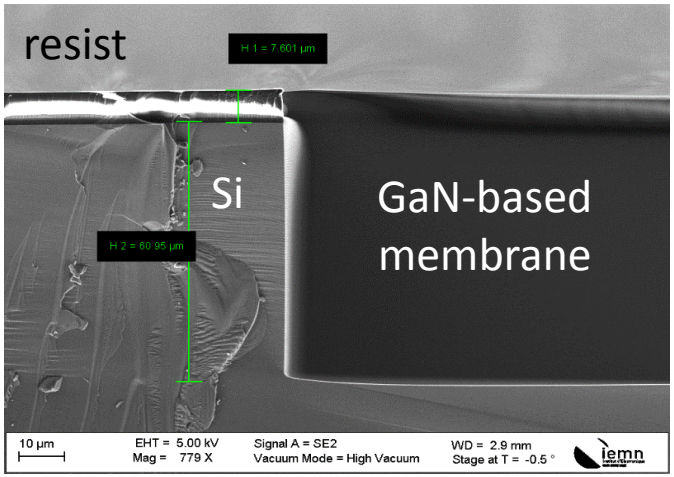
Substrate removal should be performed locally (mm^2)
as the strain issues will be significantly reduced

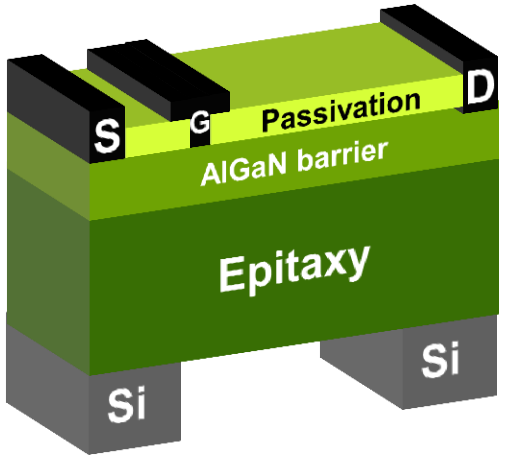
Device fabrication at IEMN within Inrel project

Process flow: backside

1. Wafer thinning and polishing down to 200 µm
2. Photolithography (laser writing)
3. Deep etching (Bosch process)
   - High selectivity with the AlN nucleation layer







Backside view after local Si removal

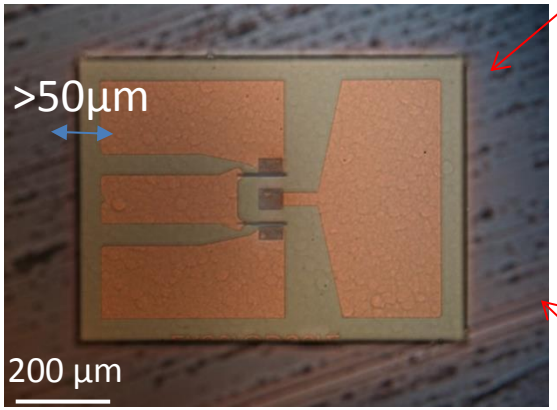
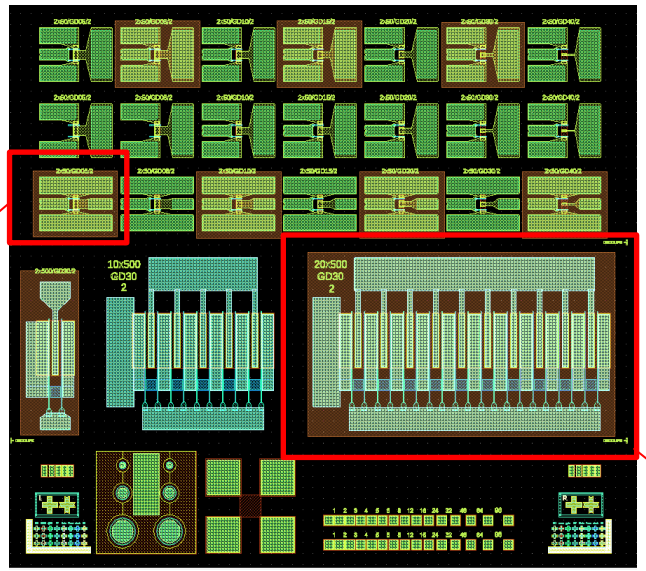
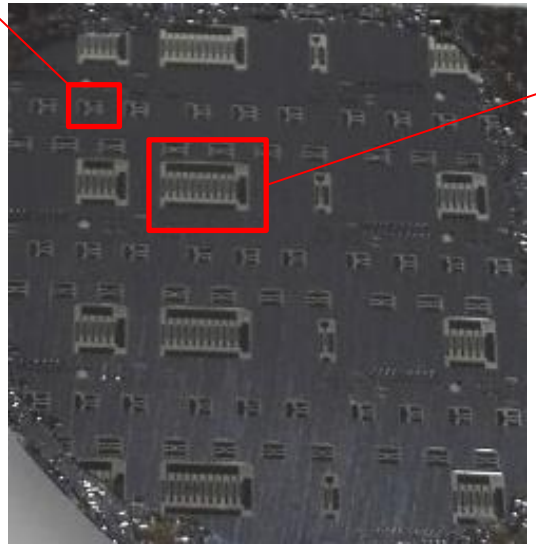


Image of a 2x50 transistor GD20 backside view





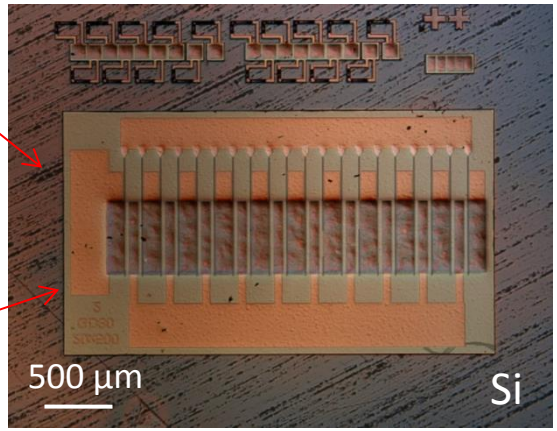
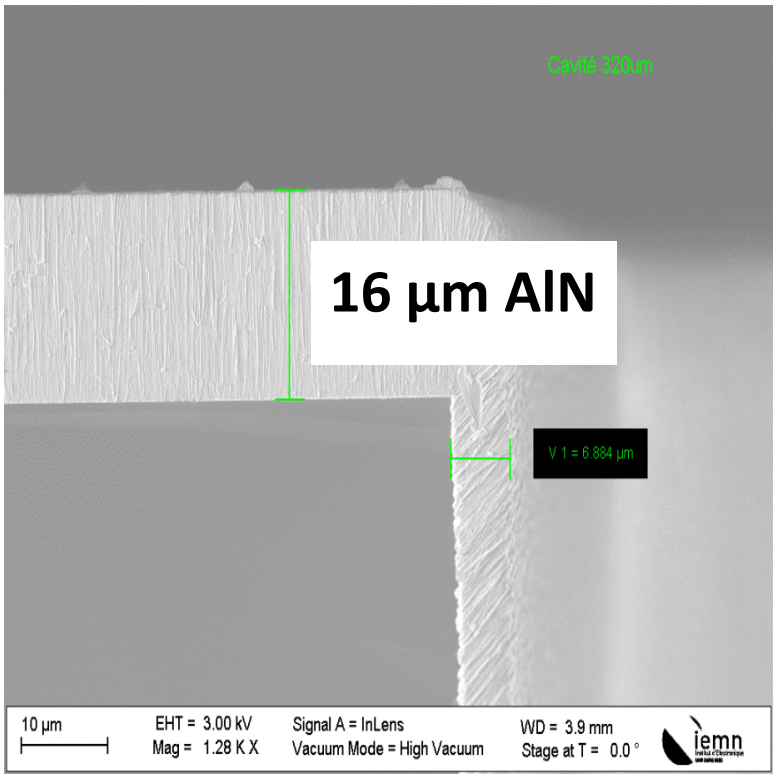
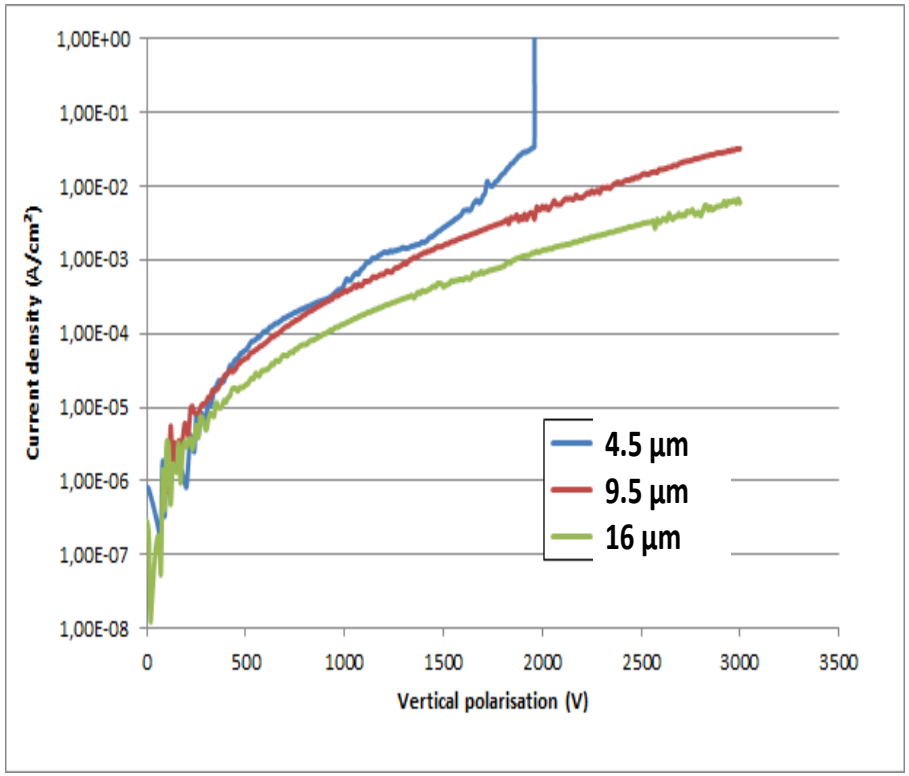


Image of a multifingers transistor GD20 backside view

UWBG such as AlN are a key to overcome vertical BV

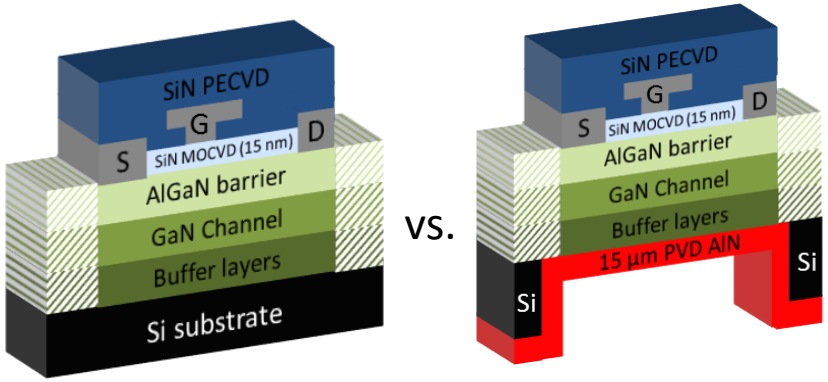




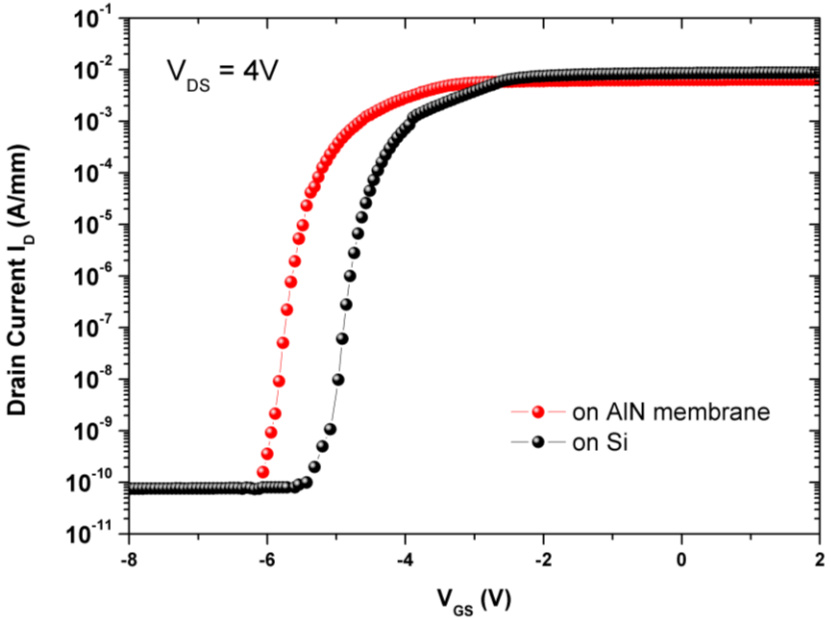
High dielectric quality with a breakdown field much higher than GaN (> 4 MV/cm) while using a temperature deposition < 350° C

Deposition by PVD can be achieved up to 12-inch: low cost

Comparison of electrical performances of GaN-on-Si vs. GaN-on-AlN

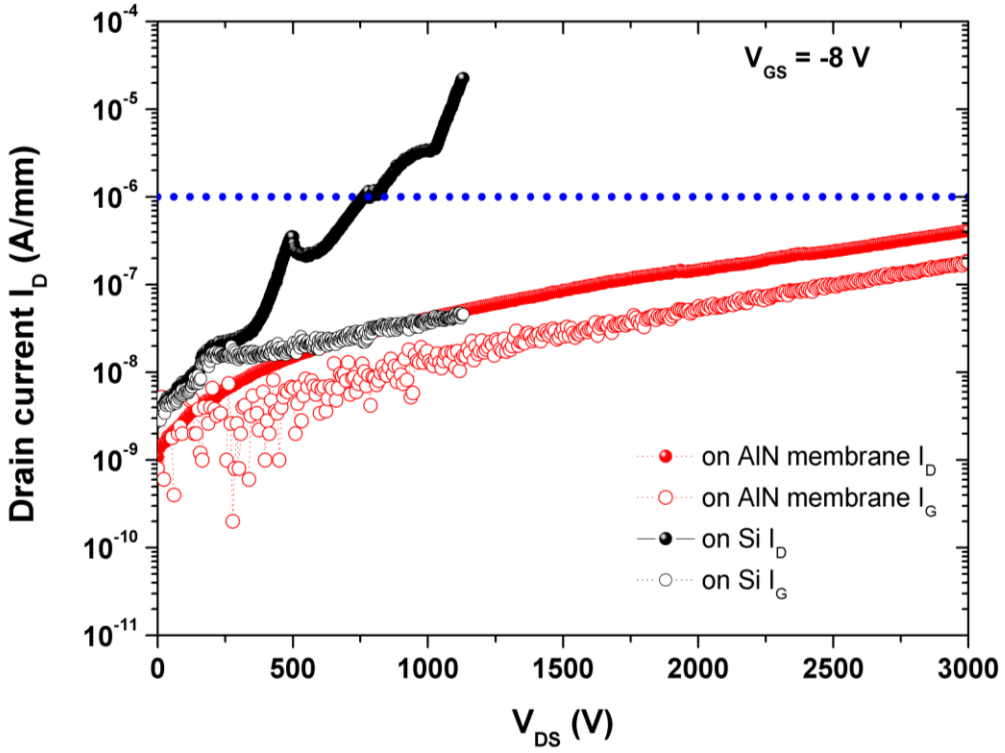


2x50 µm; GD: 40 µm; Lg : 2µm



I_D- V_G of transistors on Si and on PVD AlN

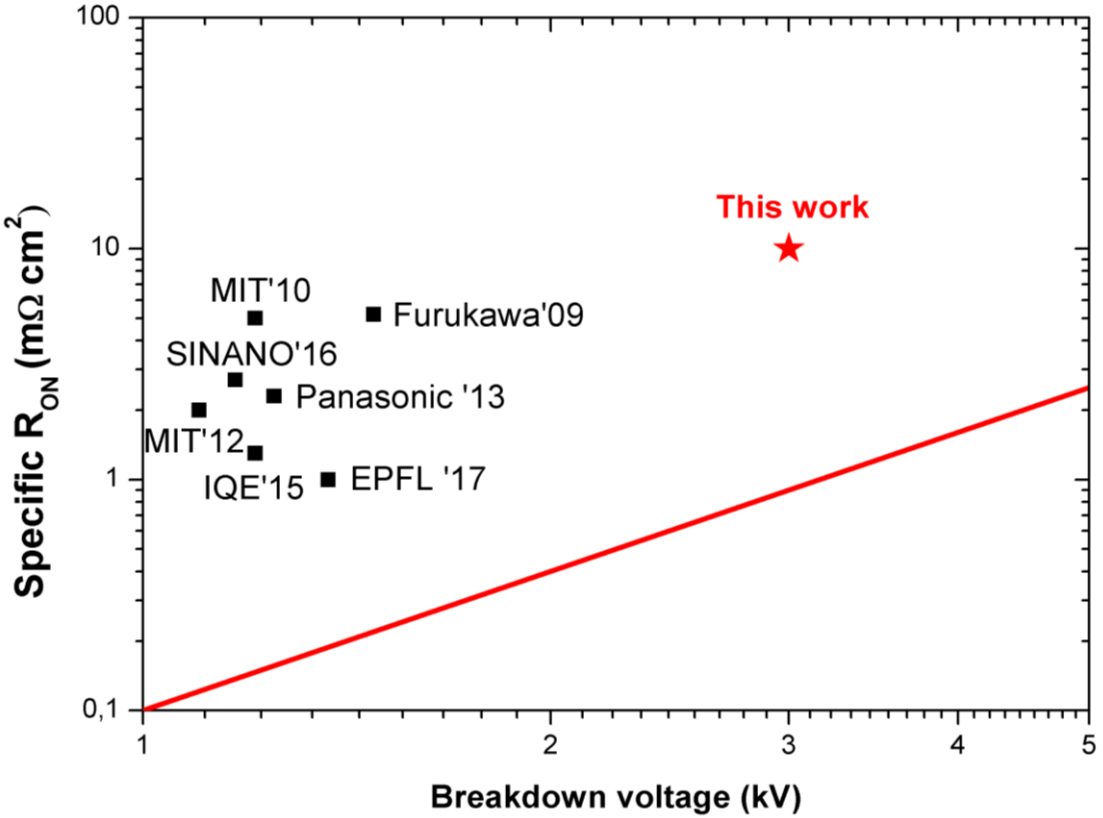
Off-state characteristics (floating substrate)



Very low leakage up to 3 kV (< 1 µA/mm)

Blocking voltage far beyond the state-of-the-art

Lateral Breakdown defined @ 1 µA/mm



Next step is to achieve these results on larger devices (> 10 mm)

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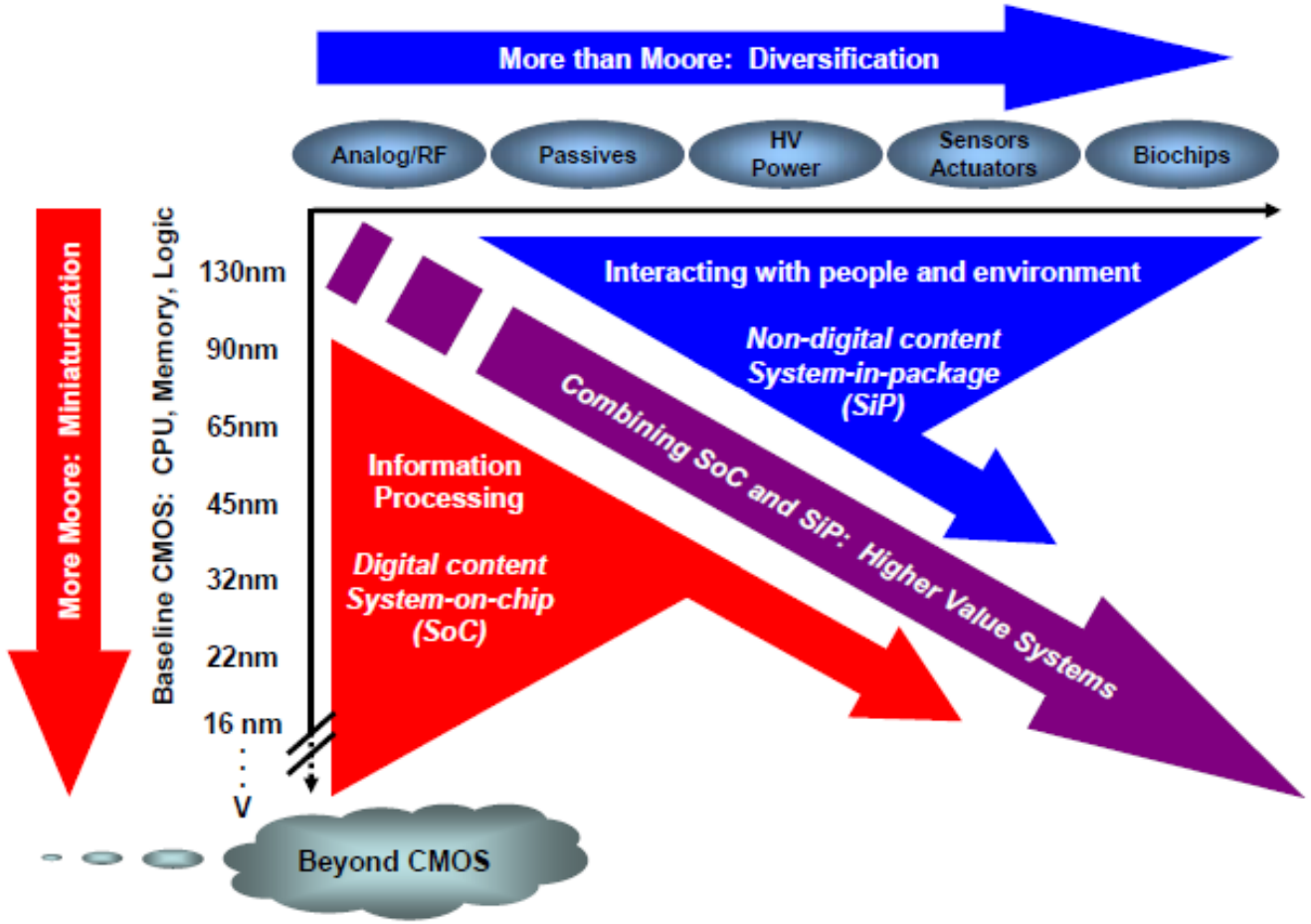
Future of microelectronics



End of silicon domination,
Introduction on the market of new materials such as high power GaN-on-Si for highly functional devices

Future of microelectronics

- Time for opportunities (new comers, young researcher or PhD students):
  - ➢ Transition towards new materials
- Multidisciplinary research teams will be required to overcome future challenges
- Unlike niche applications such as microwave and mmW, the cost will remain the main figure of merit for next generation of power devices