MODERN HIGH PERFORMANCE ASSEMBLY AND INTERCONNECTION TECHNOLOGIES FOR WBG POWER SEMICONDUCTOR POWER ELECTRONICS

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‘TECHNOLOGIES FOR ENERGY SUSTAINABILITY’
UNIVERSITY OF PADUA SUMMER SCHOOL IN INFORMATION ENGINEERING
IN CONJUNCTION WITH H2020 PUBLIC FUNDED RESEARCH PROJECT INREL-NPOWER
BRESSANONE/BRIXEN, JULY 5TH 2017

Università degli Studi di Padova

Dipartimento di Ingegneria dell'Informazione

InRel NPower

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Modern High Performance AIT for WBG PSC PE
Content

- Introduction and system definitions
- Assembly and interconnection technologies
  - Materials' basics
  - Specific technologies: Ag-Sintering, diffusion soldering, Cu-bonding
- Components to join
  - Power semiconductor
  - Substrates and circuit carriers
- Examples of modern wide-band-gap power module concepts
- Reliability assessment
  - Principle aspects: Loads on power electronics and examples of failure mechanisms
  - Power cycle test premises and life-time curves
  - 'Robustness Validation' methodology
- Summary

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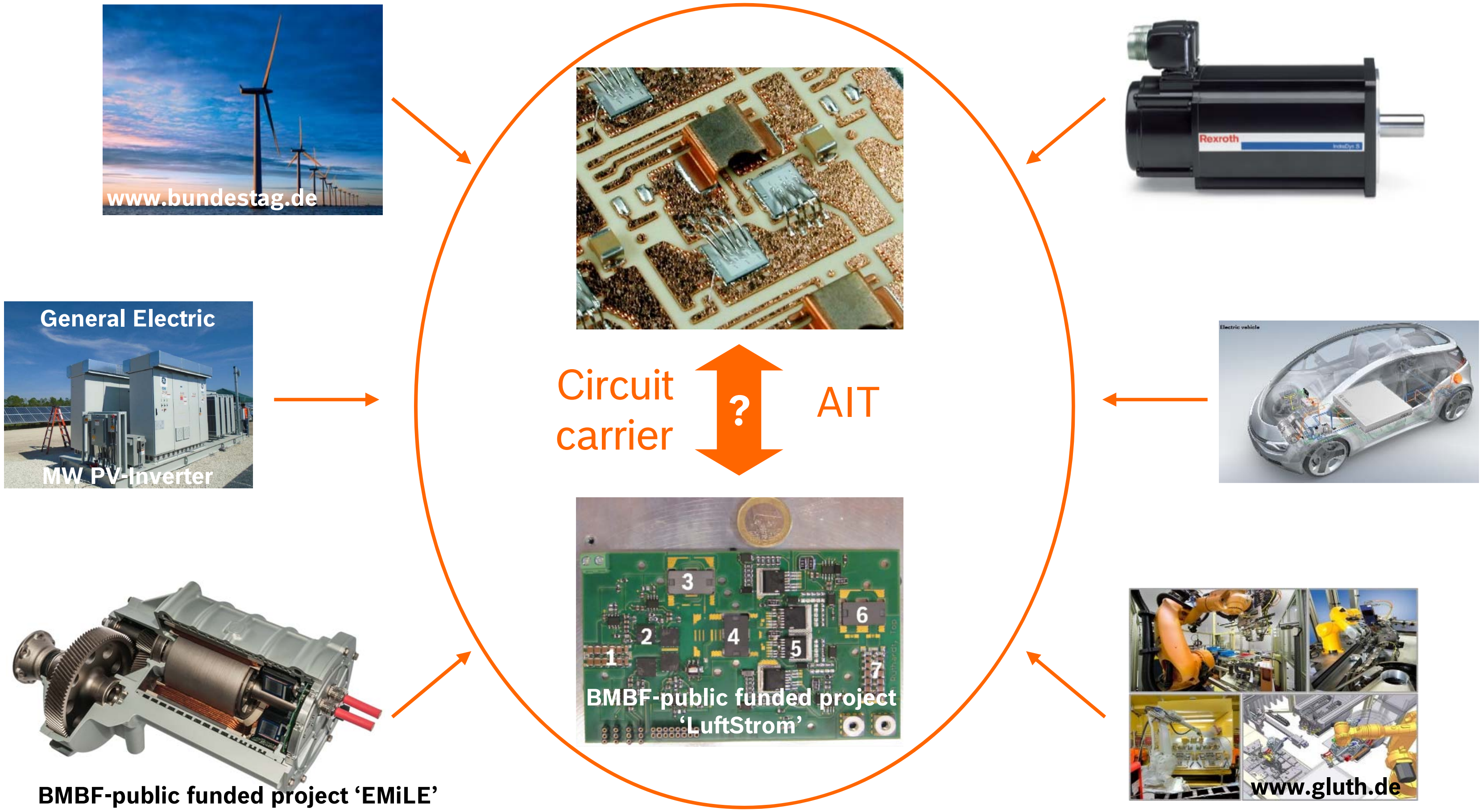
System Definition I: Power Electronics Application



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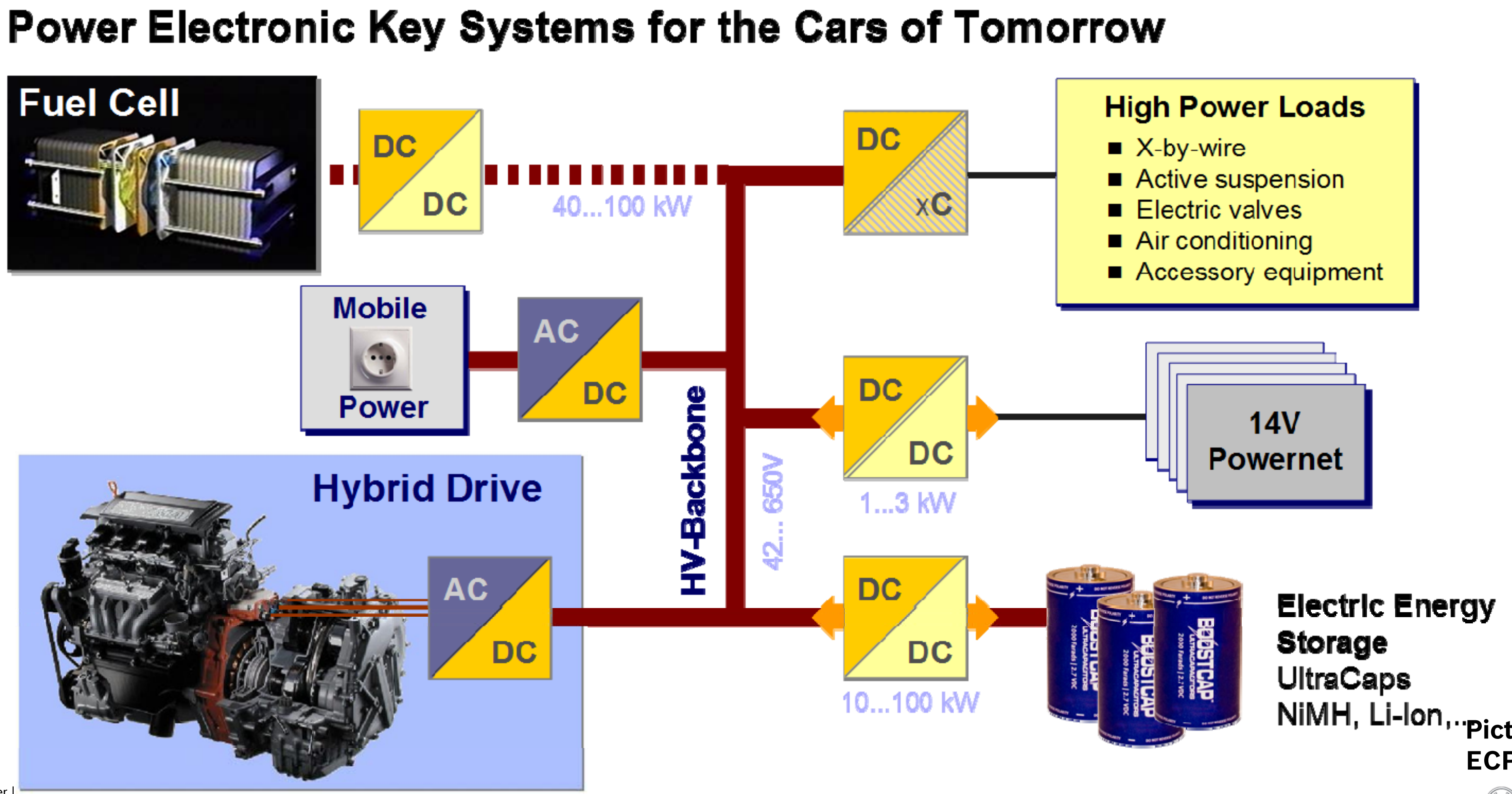
System Definition II: Automotive Electrified Powertrain System



Picture Source: ECPE

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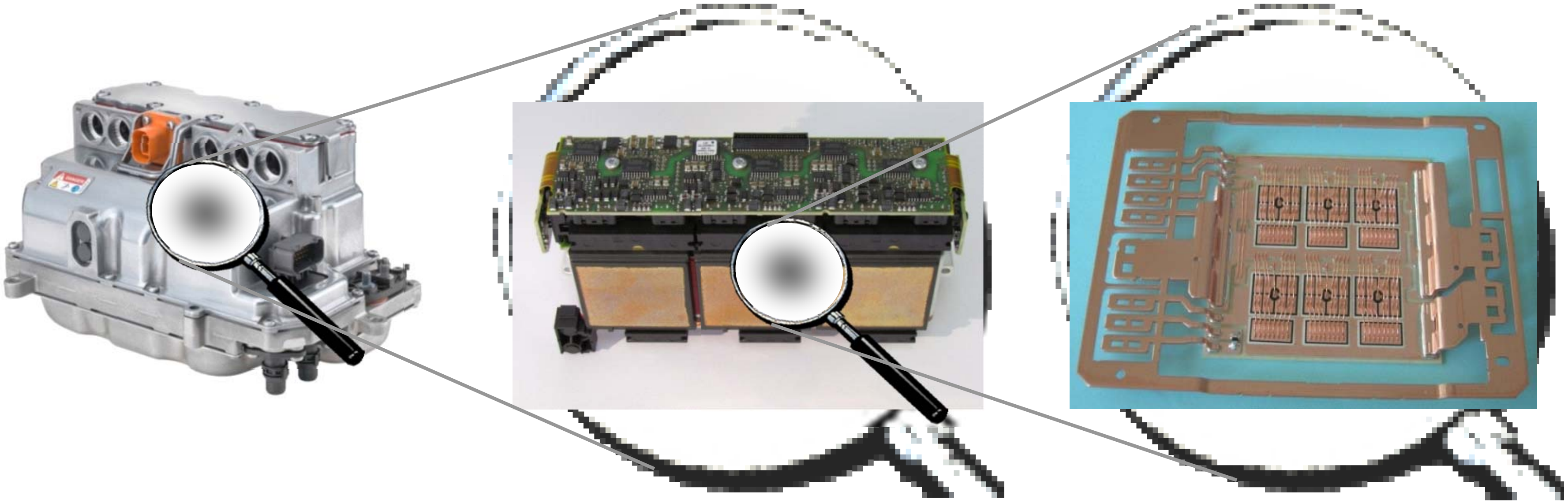
System Definition III: Built-up Levels (Example Drive Inverter)

Aggregate/System **Electronics Assembly** **Power Module**



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System Definition IV: Level of Electronics Packaging

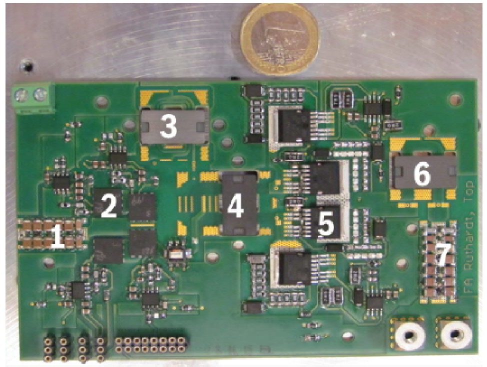
First Level Packaging (FLP)

- Bare-dies on a substrate w/ 'housing'
  - Discrete's packaging
  - Power module
- AITs of bare die
  - Die-attach
  - Bonding
  - …

Cross section of a typical power module

Second Level Packaging (SLP)

- Complex mixture of components on a substrate
  - Discrete actives
  - Diverse passives
  - Diverse sensors
  - Plugs and connectors
  - …
- AITs on pcb
  - SMD reflow soldering
  - SMD adhesives
  - THD selective soldering
  - THD press fitting
  - THD screwing
  - …



SLP of a DC/DC-converter BMBF-public funded project 'LuftStrom'

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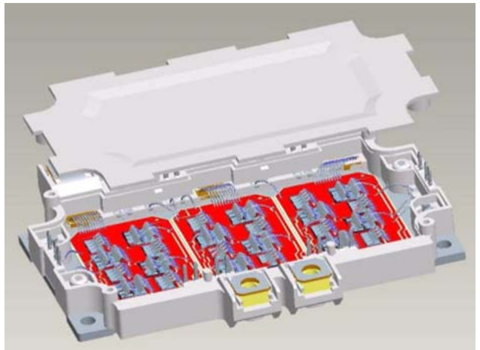
System Definition Va: Power Module Technologies

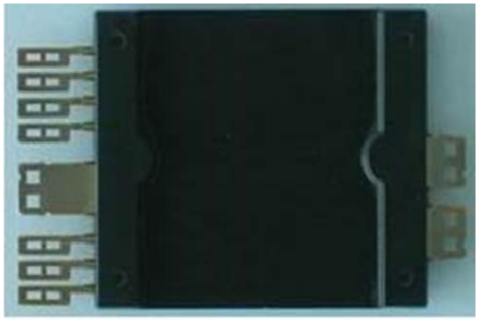
Module base technologies

- Open construction module



Picture Source: M. Thoben, Infineon, within BMBF Public funded project 'ProPower'

- Molded module



Picture Source: F. Osterwald, Danfoss, within BMBF Public funded project 'ProPower'

Diversified module technologies

- Circuit carrier
  - Ceramics (DCB, AMB)
  - Lead-frame, ...
- Die-attach power semiconductor
  - Solder
  - Ag-sintering, diffusion-soldering
- Top-side contact Chip
  - Al-bonding
  - Cu-bonding
- Semiconductor metallization
  - AlSiCu, Ni/Au, Cu, ...
- Chip-mounting und therm. management
  - Single-sided joining and contacting
  - Double-sided joining
- Module-mounting on cooler
  - Polymeric thermal interface material
  - Soldering
  - Ag-sintering

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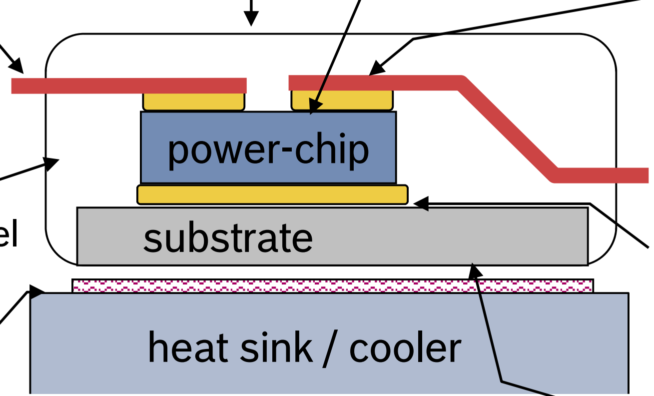
System Definition Vb: Power Module AIT Design Elements

Smart Power Integration
- multi-chip system-in package (driver IC, discrete, passive)

Peripheral Contacts
- US-Bonding
- Welding
- Soldering
- Press fitting

Power Packaging
- Frame module w/ gel
- Molded module
- PCB embedded power-dies

Thermal Interface Material (TIM)
- Thermal adhesive or foil
- Epoxy / soldering / Ag-sintering



Power Semiconductors
- Si
- SiC, GaN
- Chip-metallization

Top-Electrode
- Al-bond material
- Cu-bond material
- Cu-clip soldered
- Cu-clip Ag-sintered

Die-Attach
- Soldering
- Diffusion soldering
- Ag-sintering, sinter adhesive

Circuit carrier
- DCB, DAB, AMB: Al_2O_3, Si_3N_4 or AlN ceramics
- Cu-lead frame / Insulated Metal Substrate

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Content

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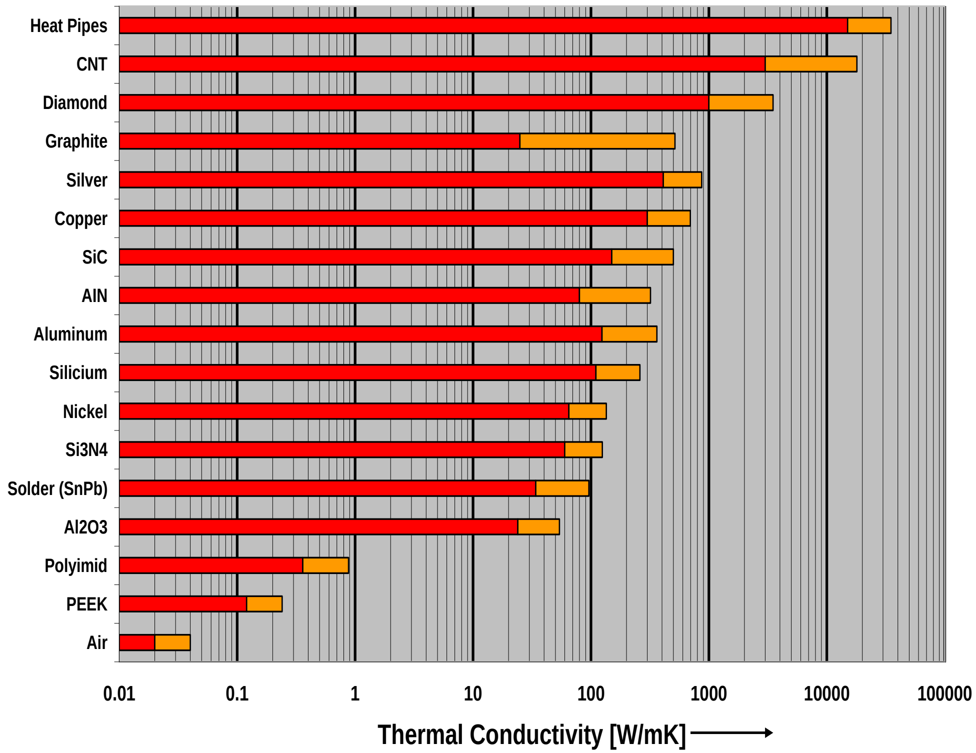
Functions of Assembly and Interconnection Technologies

- **Mechanical**
  - Young's modulus *E*
  - Shear modulus *G*
  - Plastic deformation
  - Stress-strain-characteristics $\sigma - \varepsilon$
  - Bending strength
- **Thermal**
  - Coefficient of thermal expansion α
  - Specific conductivity λ_{th}
  - Absolute resistance R_{th} bzw. Z_{th}
- **Electrical**
  - Specific conductivity λ_{el}
  - Absolute resistance R_{Ohm}



Picture Source: Prof. Martin März, FhG IISB

Modern High Performance AIT for WBG PSC PE
(Solder) Material Characteristics

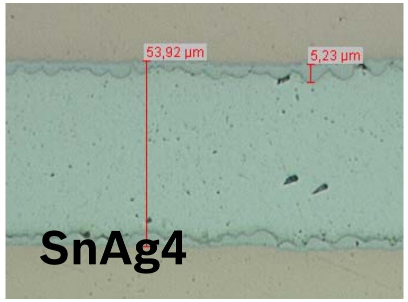
- **Metallurgical alloy:** (non-)eutectic binary (e.g. SnPb, BiAg, AuSn, ...), ternary (e.g. SnAgCu), ... (e.g. 'InnoLot-alloy' SnAgCuSbBiNi), further 'dopants' (e.g. precipitation hardening, ...)

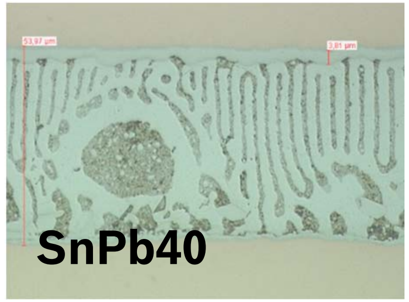
- **Microstructure:** morphology (e. g. grains), diffusion (e. g. intermetallic compound – IMC), grain coarsening, sliding of grain boundaries, ...

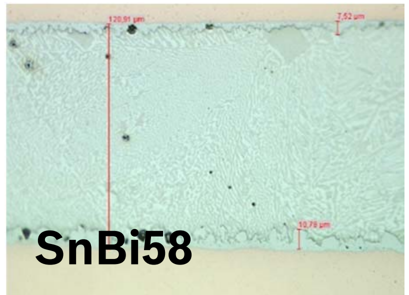
- **Physical Properties:** Young's modulus, stress-strain-properties (e.g. elastic, plastic, visco-plastic, creep, ...)

- **Fatigue:** crack initiation and crack progress, physics-of-failure, statistical distributions, ...

Never forget: (Solder) Material systems are quit complex systems







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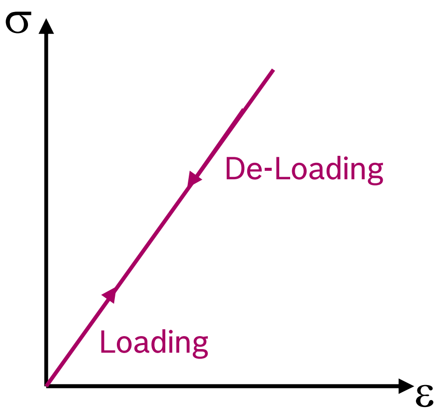
Basics on Stress-Strain-Relationships

Tensile sample tester

Picture source: www.zwick.de

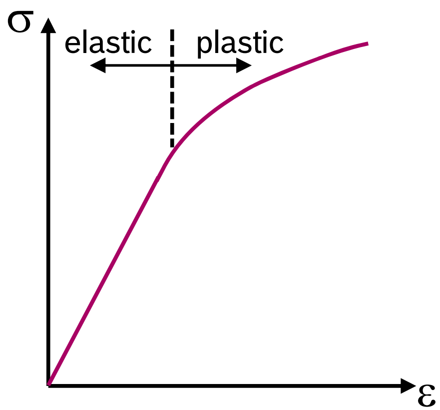
Linear elastic

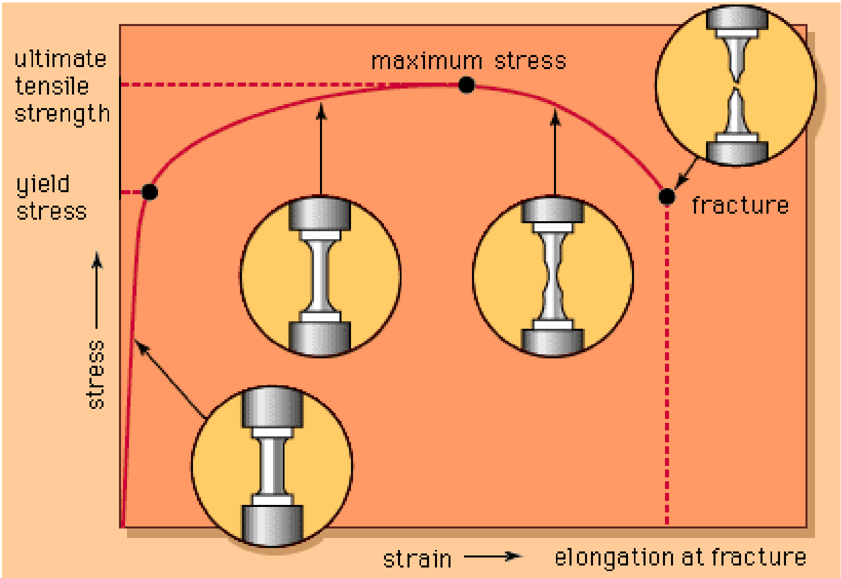


$\sigma = E \times \varepsilon$

'Hook's Law'

Plasticity





Picture source: www.totalmaterial.com

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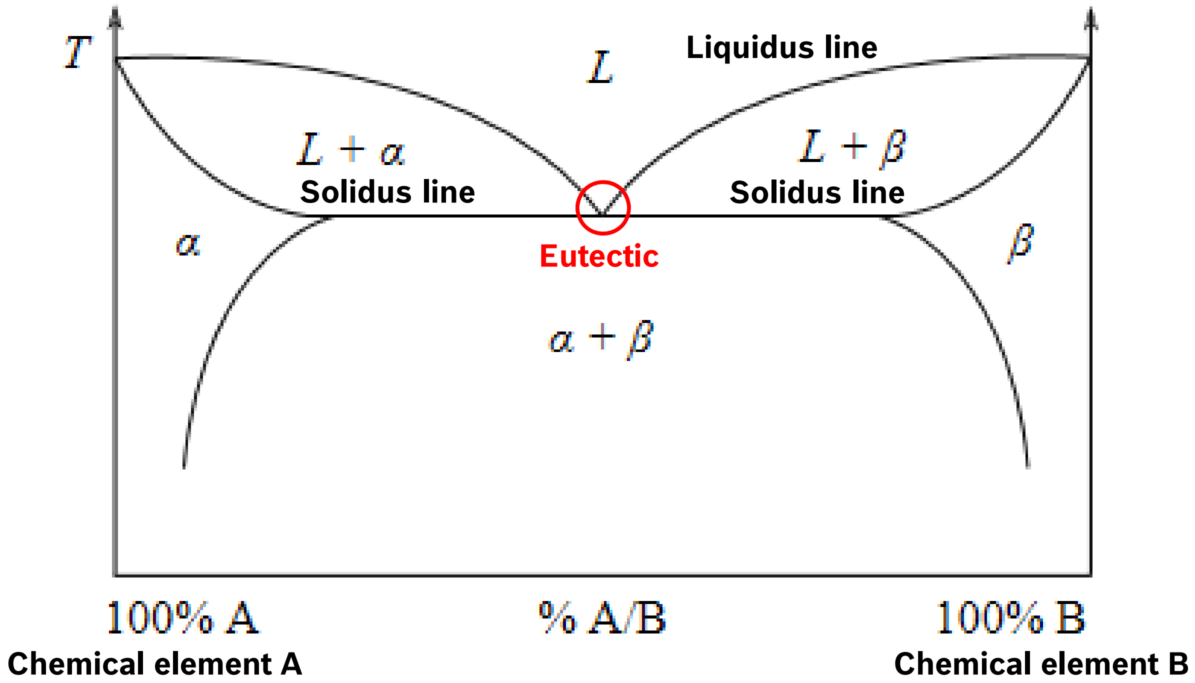
Binary Phase Diagram Liquid-Solid



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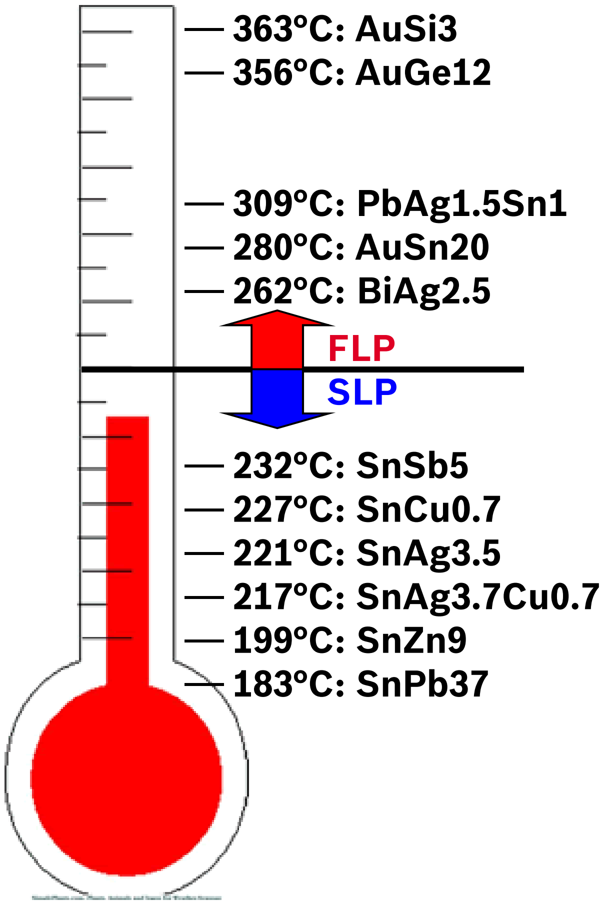
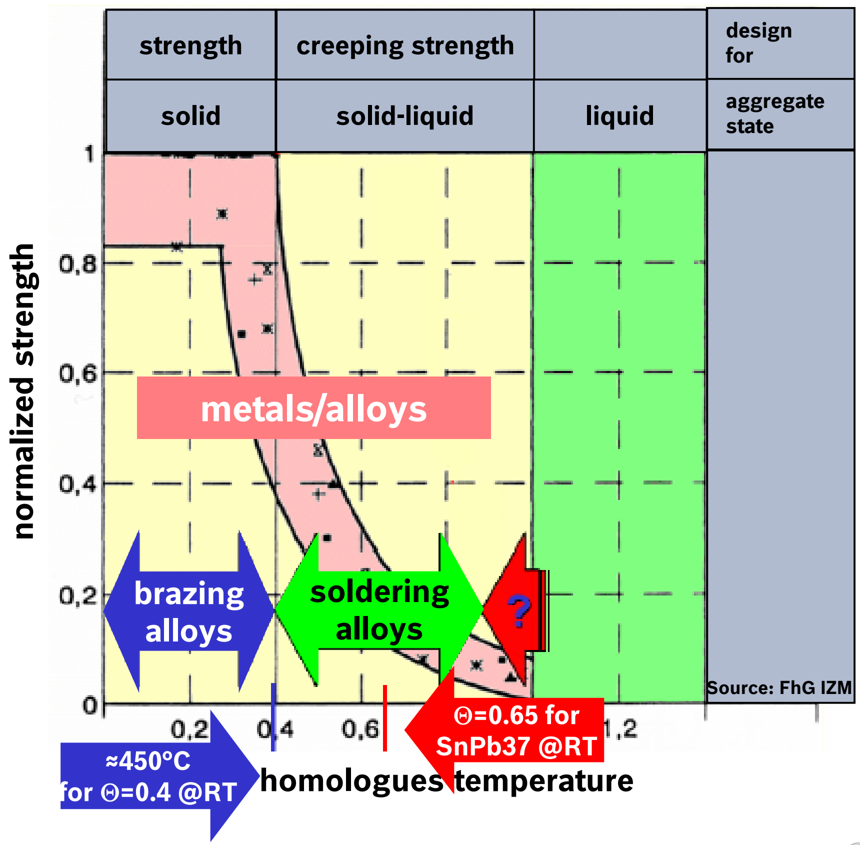
Melting Temperatures of Solders and Homologues Temperature



Homologues Temperature $\Theta = T_{use}$ [K] / T_{melt} [K]



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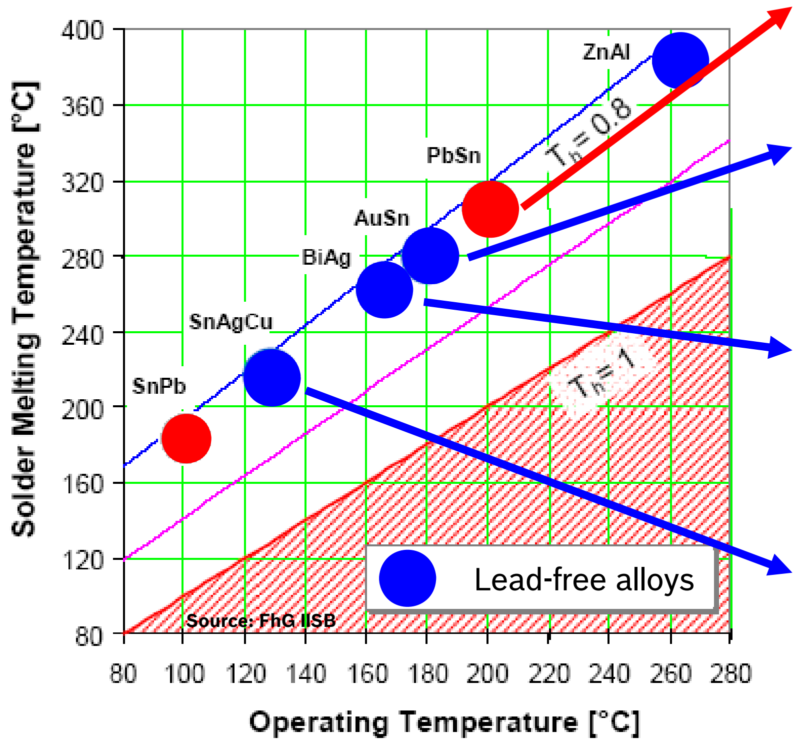
High Melting Solder Alloys



- Pb95Sn5
  - High ductility
  - Process and reliability reference
- Au80Sn20
  - High cost alternative
  - Little brittleness
  - Excellent wetting
- Bi97.5Ag2.5
  - Low cost alternative
  - High brittleness
  - Bi same chemical group as Pb
- Sn96.5Ag3.0Cu0.5
  - Preferred substitute for Sn63Pb37
  - Robust processes
  - Reliable alloy up to 125°C

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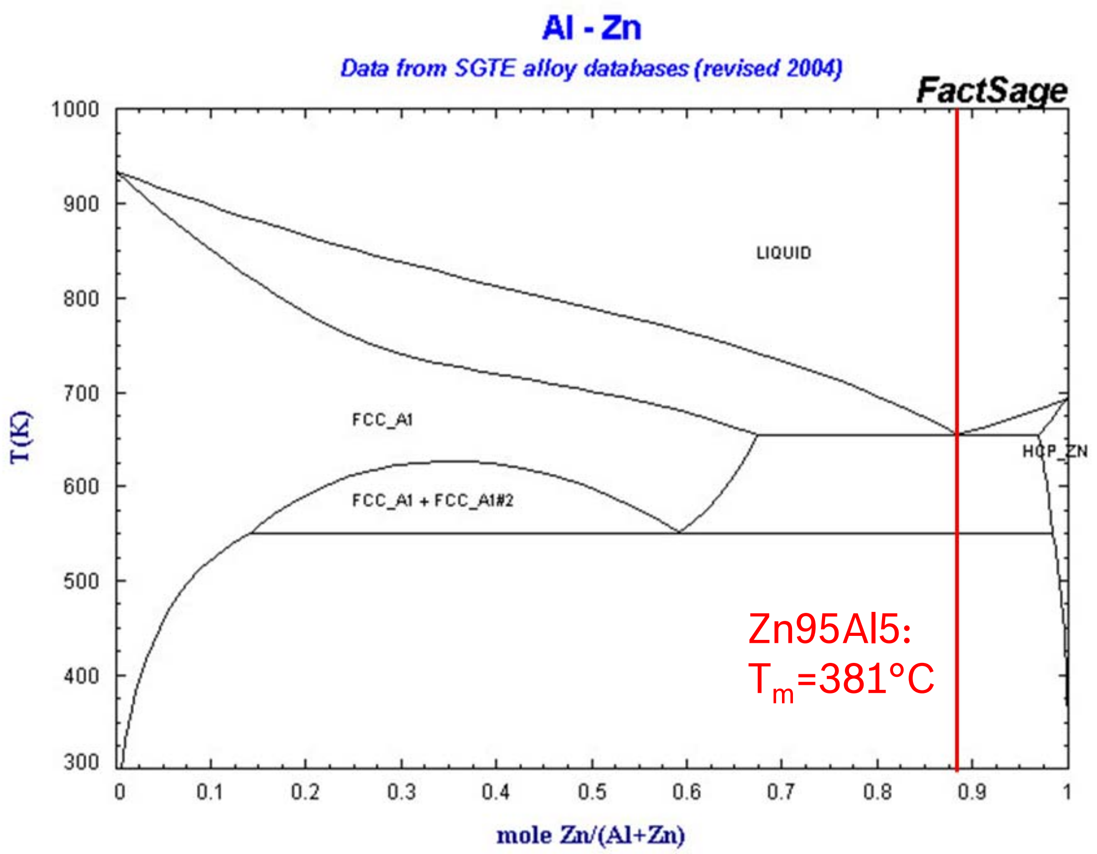
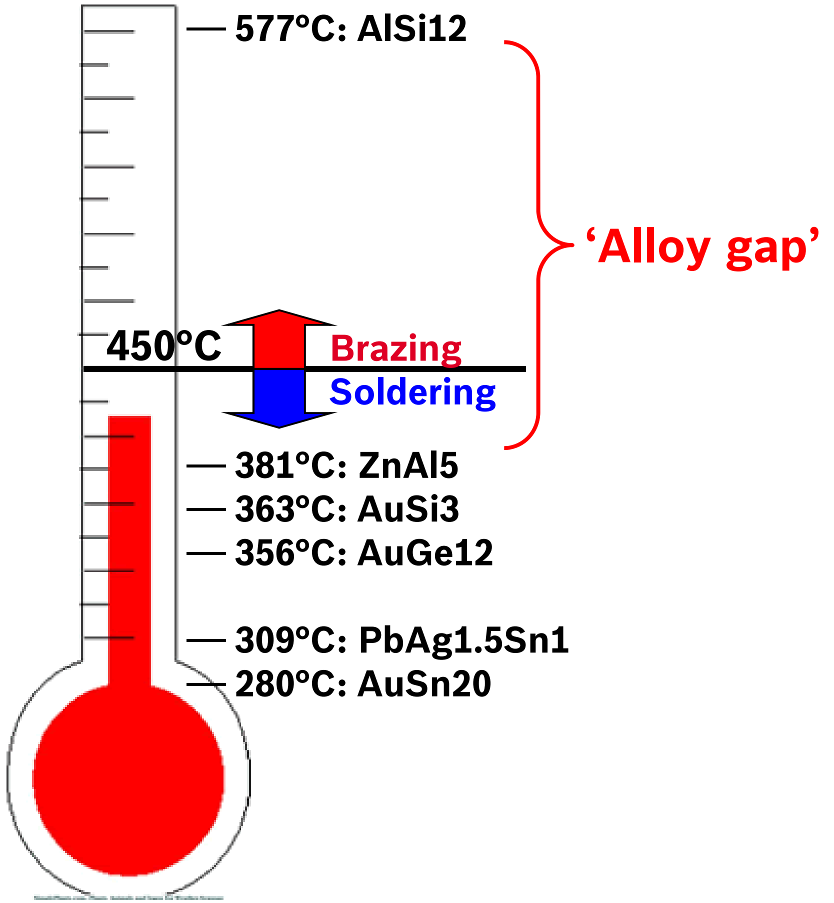
Solders at their limit?





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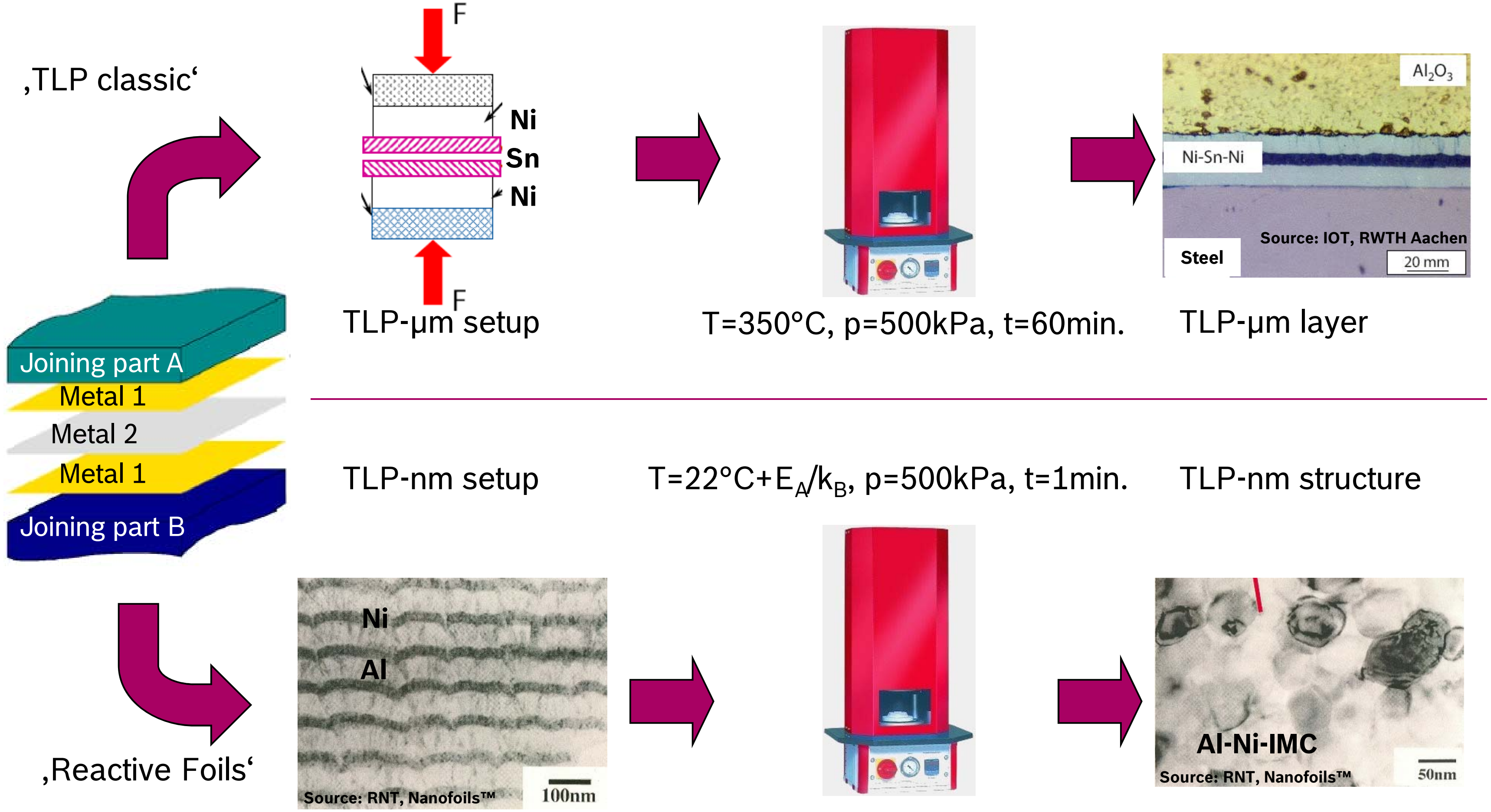
Transient Liquid Phase Diffusion Soldering (1)



Modern High Performance AIT for WBG PSC PE
Transient Liquid Phase Diffusion Soldering (2)

TLP classic:

- High melting metals:
  - Au, Ag, Cu, Ni, …
- Low melting metals:
  - Sn, Ge, In, …
- Established die-attach systems
  - Au-Sn or (Si-)Au-Sn with few µm of Au as die-attach (e. g for opto-electronic devices)
- High temperature capability due to primary IMC microstructure
- Open technology questions
  - Reliability in power cycle tests?
  - Cost-level for power semiconductors?

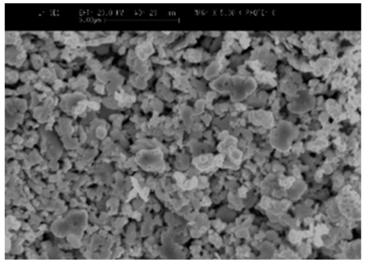
Reactive Foils:

- Commercially available:
  - e.g. RNT Nanofoils™
- Interfacial characteristics:
  - soldered-like
  - brazed-like
- Due to sputter processes for the nm-scale: costly
- But further research activities ongoing, especially to raise layers on (sub)µm-scale thicknesses w/o losses in processability

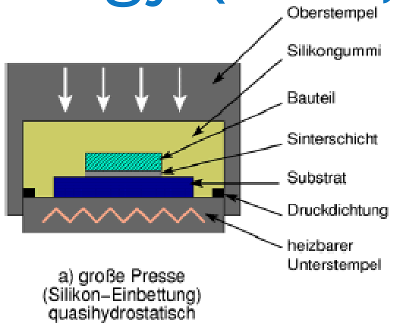
Modern High Performance AIT for WBG PSC PE

Low Temperature Joining Technology (LTJT, Ag-Sintering) (1)

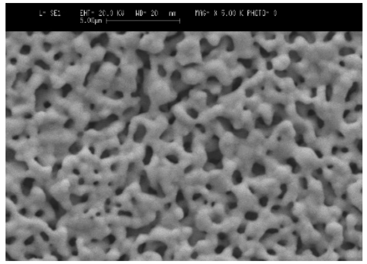
‚Classic process‘



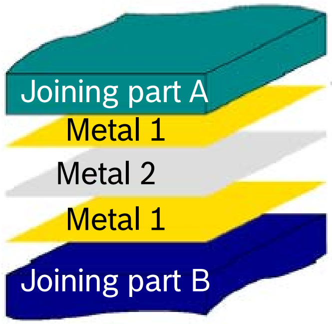
Ag-LTJT-µm paste



T=240°C, p=40MPa, t=2min.



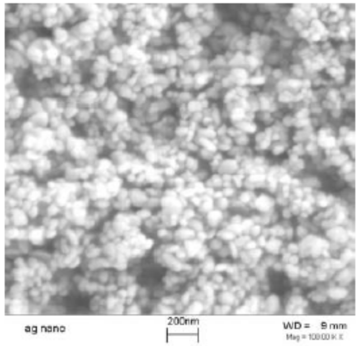
Ag-LTJT-µm layer

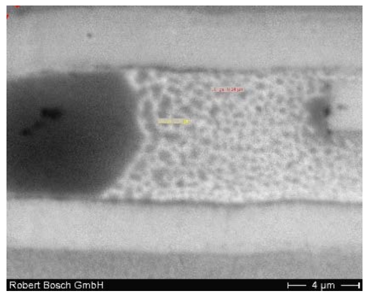


Ag-LTJT-nm paste

T=300°C, p=100kPa, t=60min.

Ag-LTJT-µm layer





‘Nanoparticle Process’

Modern High Performance AIT for WBG PSC PE
Low Temperature Joining Technology (LTJT, Ag-Sintering) (2)

LTJT classic process:

- Pastes are commercially available
- Functionalizes surfaces of joining partners
  - Ag, Ni/Au (e.g. ENIG), Cu-blank (under development)
- Characteristics of joint
  - Dense, low porous joint with good connection to joined partner surfaces ⇒ maximal reliability
- Industrialized for single-sided power modules
- Open technology questions
  - Process transfer to double-sided systems?
  - Integration of further components in power module while applying just one process step?

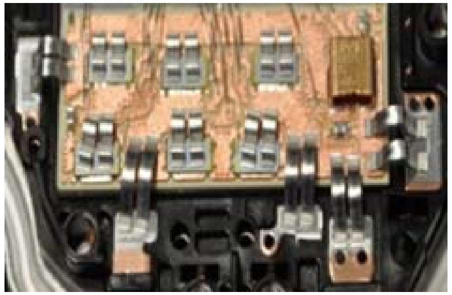
LTJT nanoparticle process:

- Pastes are commercially available
- Functionalizes surfaces of joining partners
  - Ag, Ni/Au (e.g. ENIG), Cu-blank (under development)
- Characteristics of joint
  - Porous joint with reduced connection to joined partner surfaces ⇒ reduced reliability
- Industrialized for LED-applications
- Open technology questions
  - Process transfer to molded power modules w/o losses in reliability?
  - Easier integration ability of further components?

Modern High Performance AIT for WBG PSC PE
US-Bonding Technology on Power Semiconductors

Standard Aluminium US-Bonding

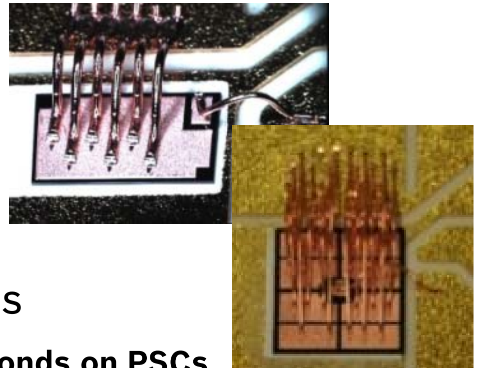
- Well established process on PSC
  - Heavy wire
  - Ribbon bond
- Chip metallization AlSi,AlCu, AlSiCu (≈3 µm) is typically designed for this process landscape
- Limitations
  - Electrical conductivity
  - Thermal conductivity
  - Power cycle Robustness



Al-ribbon bonds on Si-MOSFET

New Copper US-Bonding

- Processes under development
  - Heavy wire
  - Ribbon bond
- New chip metallization is needed
  - Damage in active S/C-structure w/ standard metallization under bond
  - Change to thicker Cu-metallization (≈40 µm)
  - Wafer-bowing
- Improvements
  - Electrical conductivity
  - Thermal conductivity
  - Power cycle robustness



Cu-bonds on PSCs

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Content

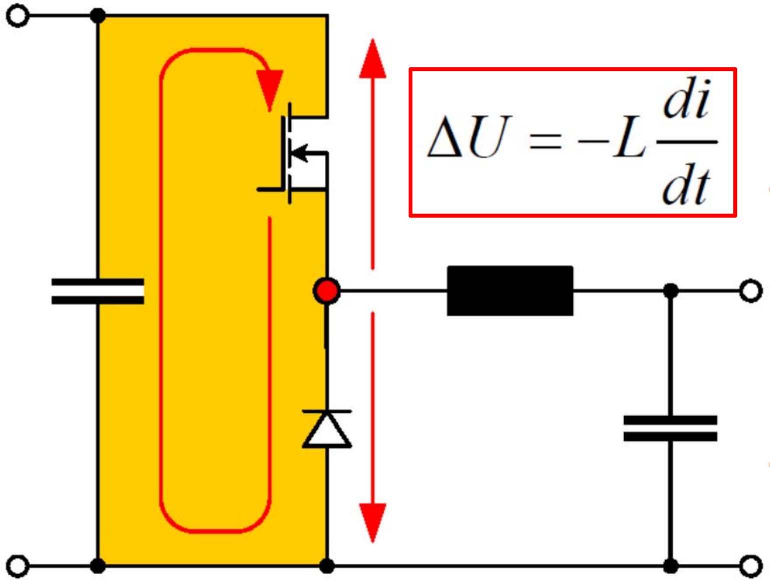
Modern High Performance AIT for WBG PSC PE
Power Semiconductor: General Requirements

Technological requirement	Typical state of the art values Si IGBT	Foreseeable values SiC MOSFET	Foreseeable values GaN HEMT
Maximum operating chip temperature	$T_{junction,max.}$ = 150°C (175°C)	175°C ≤ $T_{junction,max.}$ ≤ 250°C	175°C ≤ $T_{junction,max.}$ ≤ 250°C
Current density	2 A/mm²	3 A/mm²	≥3 A/mm²
ΔT with at least 10^6 power cycles	60 K	100 K	100 K
Power dissipation density	0,4 W/cm³	0,6 W/cm³	≥ 0,6 W/cm³
Module $R_{th,j\text{-}c}$	≈ 1 K/W	≈ 0,1 K/W	≈ 0,1 K/W
Switching Frequencies and Switching Gradients	9 kHz ≤ f_{sw} ≤ 11 dI/dt ≈ 10 kA/µs ⇒ 15 nH ≤ L_{stray} *) ≤ 20 nH	24 kHz ≤ f_{sw} ≤ 48 kHz (hard switching) dI/dt ≈ 20 kA/µs ⇒ L_{stray} *) ≤ 6 nH	24 kHz ≤ f_{sw} ≤ 1 MHz (hard → soft switching)
Integration of passives in module	Not assigned	Capacitors Resistors	Capacitors Resistors
Integration of actives in module	Not assigned	Gate-driver or µ-controller	Gate-driver or µ-controller (already on chip-design-level)

*) including peripheral module contacts

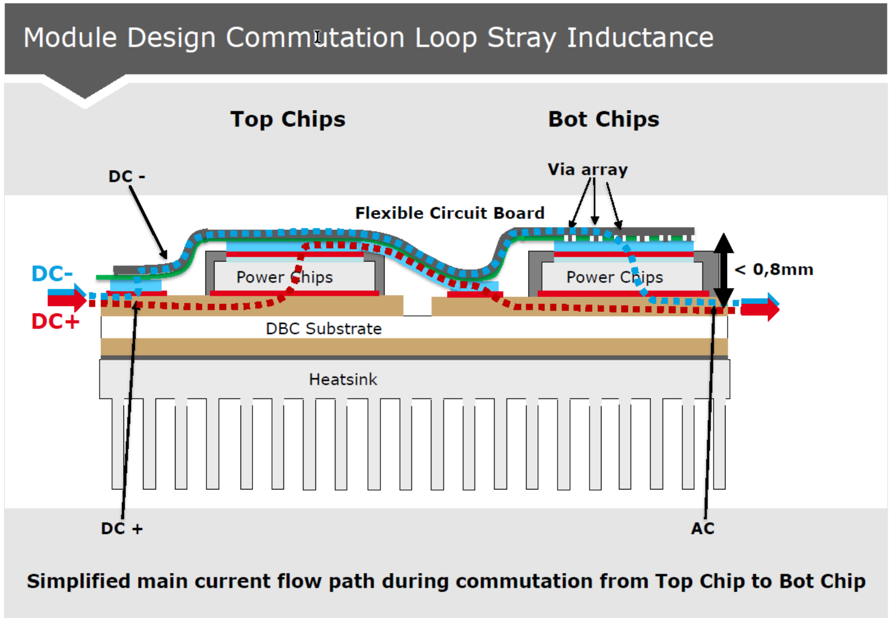
Modern High Performance AIT for WBG PSC PE

Power Semiconductor: Fast Switching and Parasitic Inductance



$$\Delta U = -L\frac{di}{dt}$$

Transfer from topology, circuitry and functional design in hardware and technology choice



Picture Source: Ch. Göbl, SemiKron

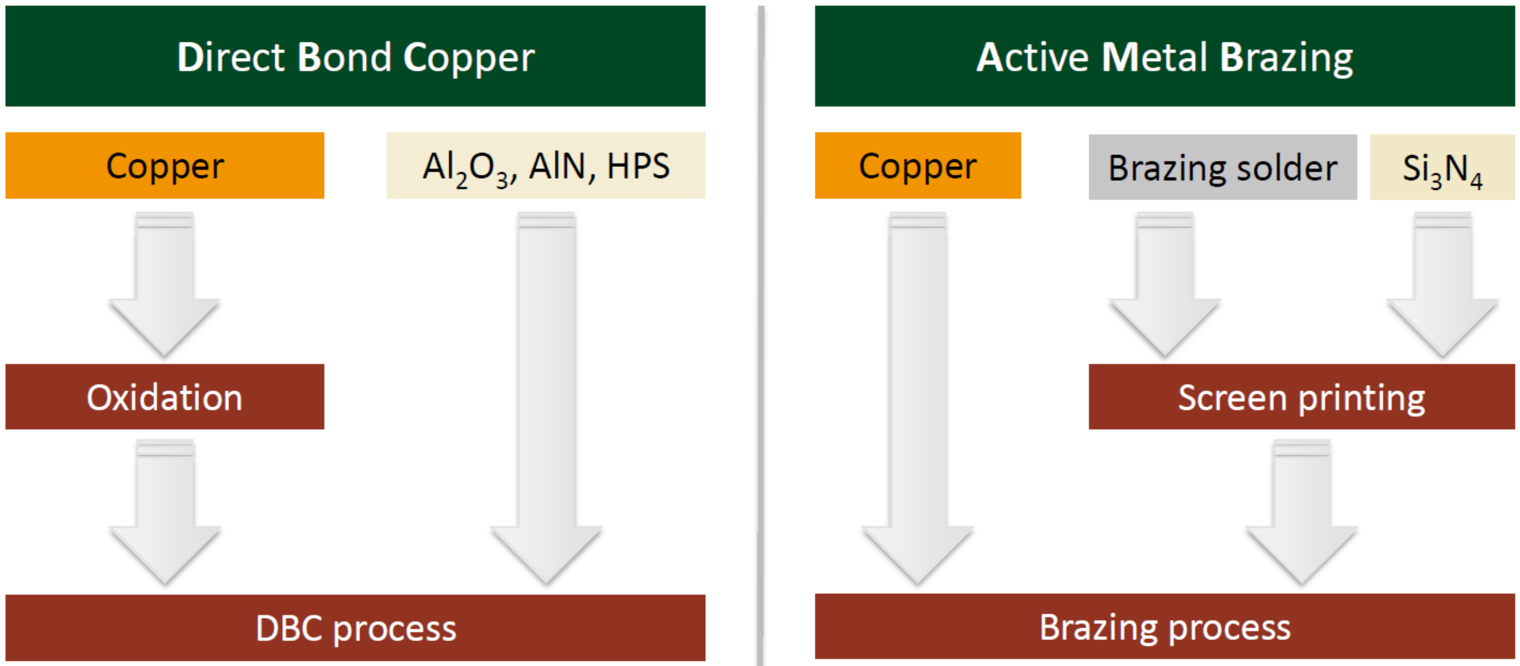
Modern High Performance AIT for WBG PSC PE
Overview of Substrate Technologies

‘Inorganic circuit carriers’	Special systems	‘Organic circuit carriers’
Power substrates: - Direct Copper Bonded - Direct Aluminum Bonded - Active Metal Brazing	‘Hybrids’: - Insulated Metal Substrate - PCB on ceramics	Rigid systems: - FR4-/FR5-pcb - High-Tg-pcb - High-current-pcb
Logic substrate: - Thick film ceramics - Low Temp. Co-fired Cer. - High Temp. Co-fired Cer.	‘Exotic’: - Cold-Gas-Spraying - Metal-Matrix-Composites	Flexible systems: - Polyimide flex foil

Integration capability (increase in functionality and added value)
Logic-power-integration (especially w/ respect of active components, ...)
Integration of passive components (e.g. C, I-Sensor, T-Sensor, ...)
Increased integration depth of thermal management
Mechatronic integration (aggregate level)

Modern High Performance AIT for WBG PSC PE

DCB- and AMB-Substrates I: Process Technologies



Direct Bond Copper

- Process temperature approx. 1065° C
- Eutectic melt reaction between ceramic and copper

Active Metal Brazing

- Process temperature approx. 800° C
- High temperature brazed joint between ceramic and copper

Picture Source: K. Schmidt, Rogers Corp.

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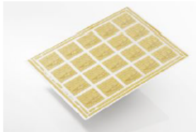
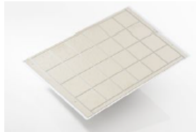
DCB- and AMB-Substrates II: Characteristics

	curamik® Power	curamik® Power Plus	curamik® Thermal	curamik® Performance
* Values are for bare ceramics ** curamik internal tests				
Ceramic Type	Al_2O_3	HPS (Zr doped Al_2O_3)	AlN	Si_3N_4
Thermal Conductivity [W/mK]@20°C *	24	26	170	90
CTE [ppm/K] 20-300°C *	6.8	7.1	4.7	2.5
Bending Strength [N/mm²] *	450	600	350	700
Fracture Toughness $[MPa/\sqrt{m}]$ *	4.2	5.0	3.4	6.0
Peeling strength **	≥ 4 N/mm			≥ 10 N/mm
Dielectric Strength (DC) [kV/mm] *	20			
Master Card size	138 mm x 190.5 mm (usable area: 127 mm x 178 mm)			

Picture Source: K. Schmidt, Rogers Corp.

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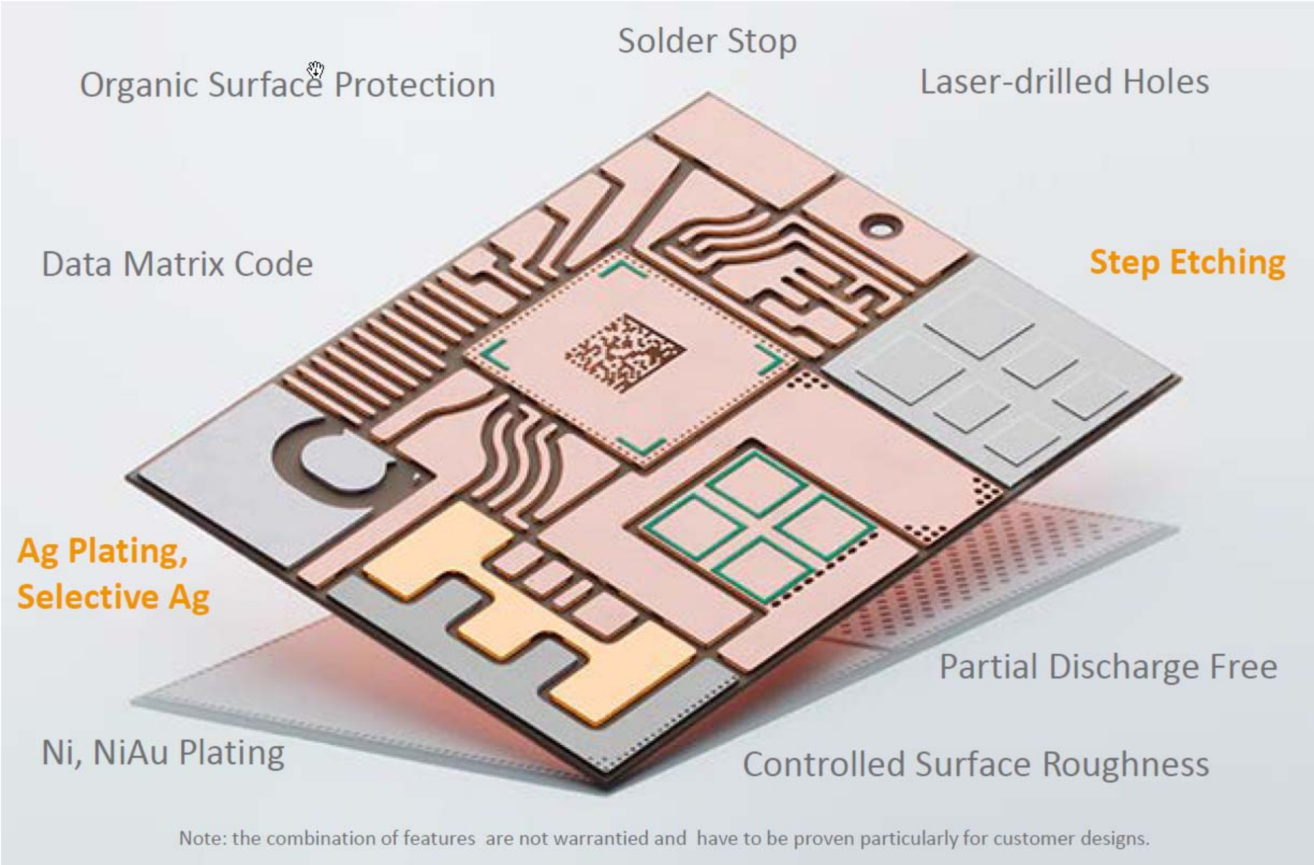
DCB- and AMB-Substrates III: Customization



Picture Source: K. Schmidt, Rogers Corp.

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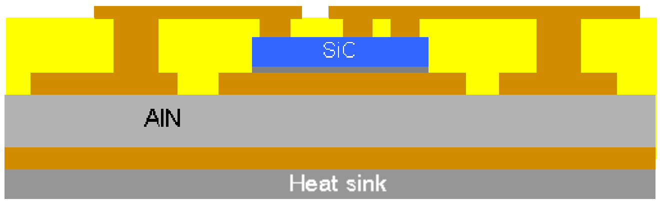
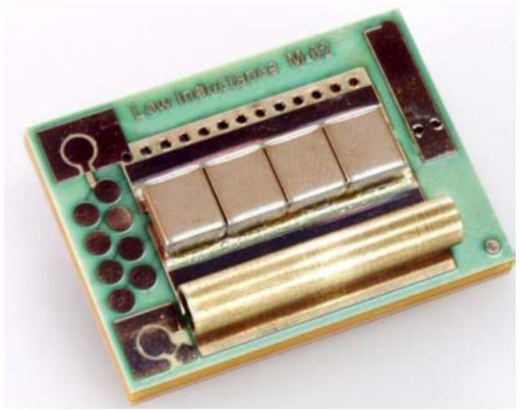
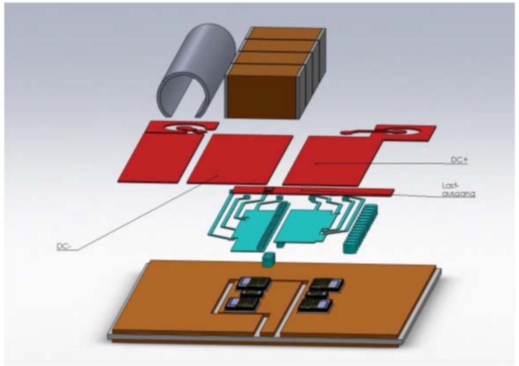
Content

Modern High Performance AIT for WBG PSC PE
Low-inductance fast switching SiC-module w/ lowest EMI (1)

- Half-bridge-module, single phase
- Power class 5 kW
- 'Extreme' design optimization of commutation cell to a level of lowest possible parasitic inductance
- DBC-substrate with a high voltage blocking SiC-JFET laminated in one prepreg layer
- DC-link-inductance: 0,6 nH
- Technology selection on 'academic level'



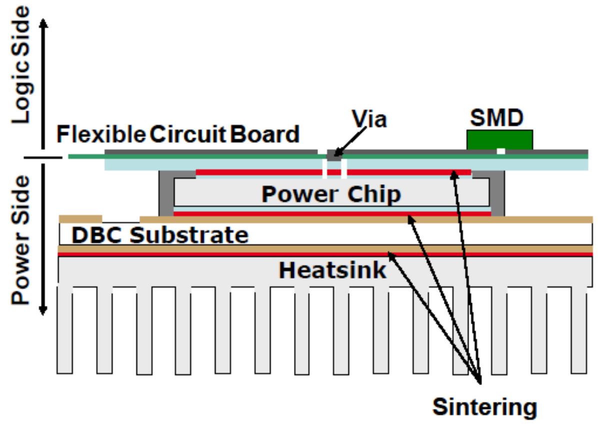


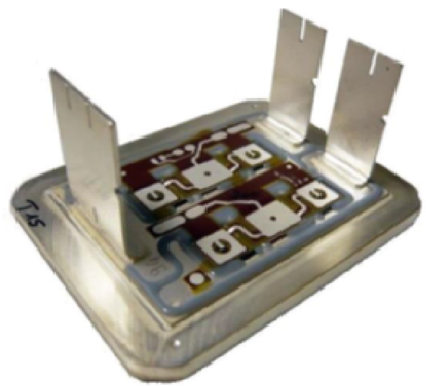


Picture Source: Prof. Eckart Hoene, FhG IZM

Modern High Performance AIT for WBG PSC PE
Low-inductance fast switching SiC-module w/ lowest EMI (2)

- Half-bridge-module, single phase
- Power class 400 kW
- Good design optimization of commutation cell to a very low level of parasitic inductance
- DBC-substrate with a high voltage blocking SiC-MOSFET laminated in flex-foil-substrate
- DC-link-inductance: ≃1 nH
- Technology close to industrialization

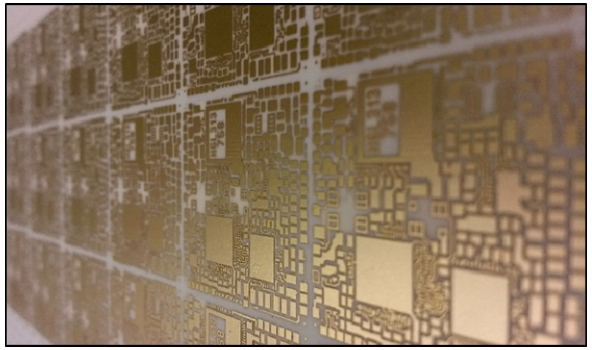


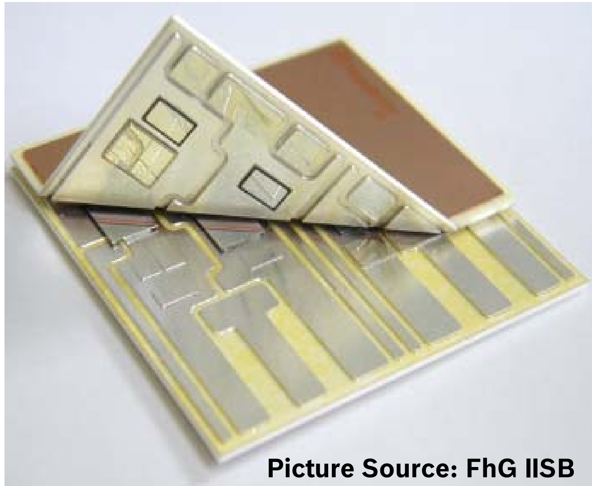


Picture Source: Ch. Göbl, SemiKron

Modern High Performance AIT for WBG PSC PE
InRel-Npower: Low-inductance fast switching GaN-module

- Full-bridge-module, three phase
- Power class 20 kW – 30 kW
- Under research investigation in the InRel-NPower project:
  - Si3N4-AMB-substrate with a high voltage blocking GaN-HEMT and with a second ‘counter substrate’ as a LTCC multilayer ceramics
  - Boundaries of design optimization of commutation cell?
  - Reachable DC-link-inductance down to 1 nH?
  - Technology boundaries on the way to the industrialization of this hardware design concept?





Picture Source: FhG IISB

Modern High Performance AIT for WBG PSC PE
Content

- Introduction and system definitions
- Assembly and interconnection technologies
  - Materials' basics
  - Specific technologies: Ag-Sintering, diffusion soldering, Cu-bonding
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  - Power semiconductor
  - Substrates and circuit carriers
- Examples of modern wide-band-gap power module concepts
- Reliability assessment
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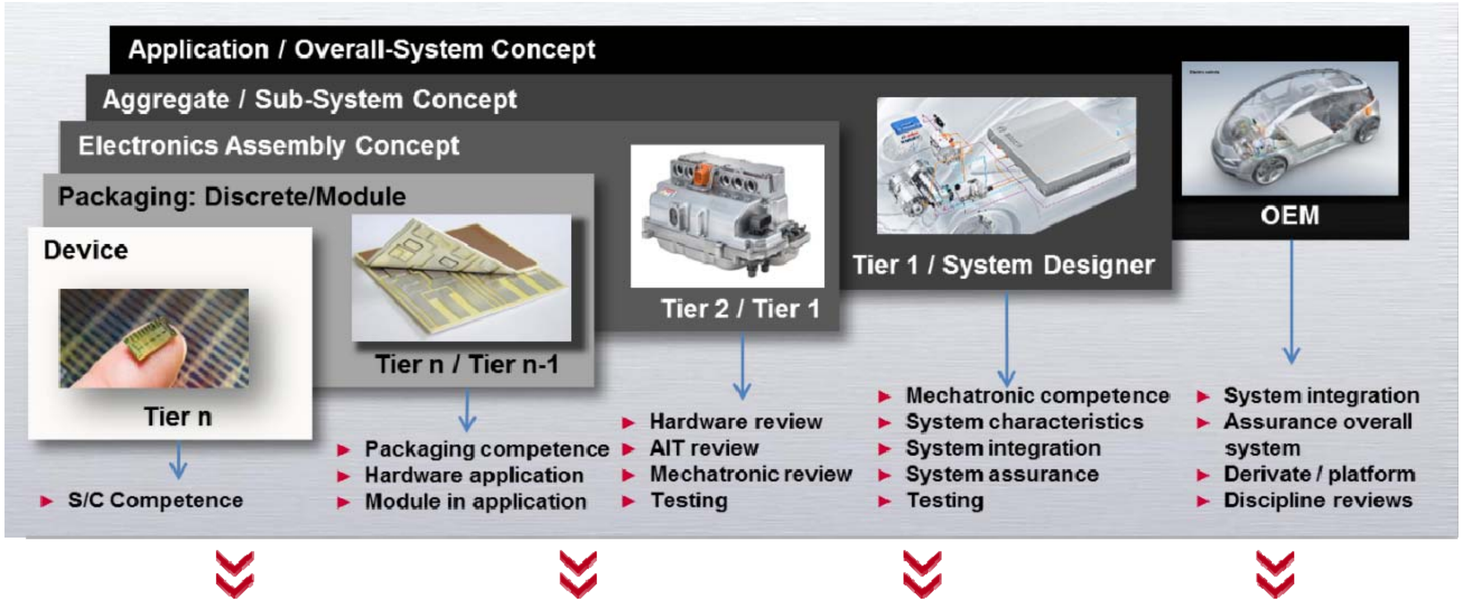
  - Power cycle test premises and life-time curves
  - 'Robustness Validation' methodology
- Summary

Modern High Performance AIT for WBG PSC PE

‘Front-Loading’ of Function and Robustness in Automotive Elec.

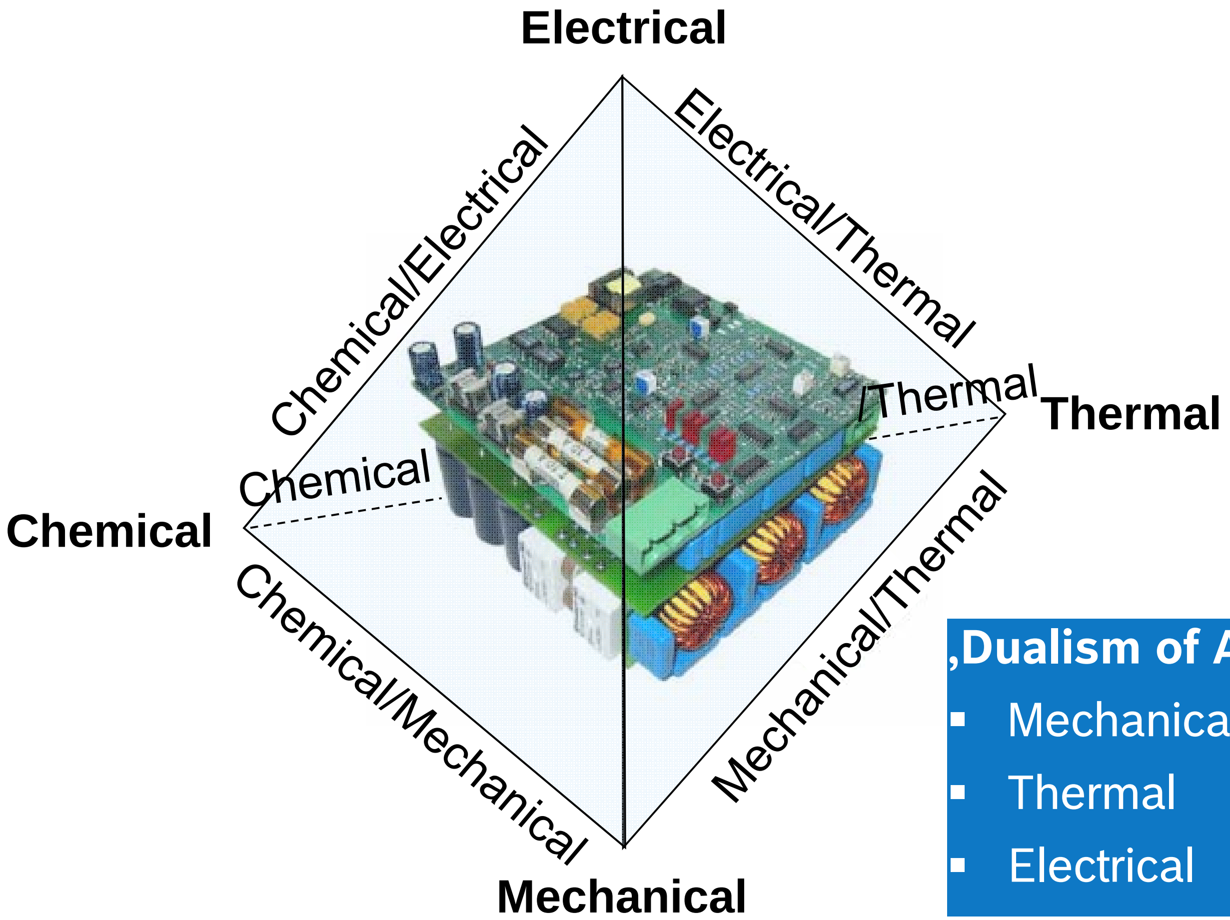


Functionality and Robustness Validation on Electronics Design upon all chain links

- **Design starts already upon device** (design, testing, screening / usage in application / life-time)
- **OEM competence mission down to Tier n**
  - Discussion about application and mission profile with S/C-manufacturer / hardware assembler
  - Expert’s dialog along supply chain (Tier n… Tier 1)
- **Competence development at Tier n … Tier 1**

Picture Source:
B. Hellenthal, Audi AG, within the BMBF public funded project ‘ProPower’

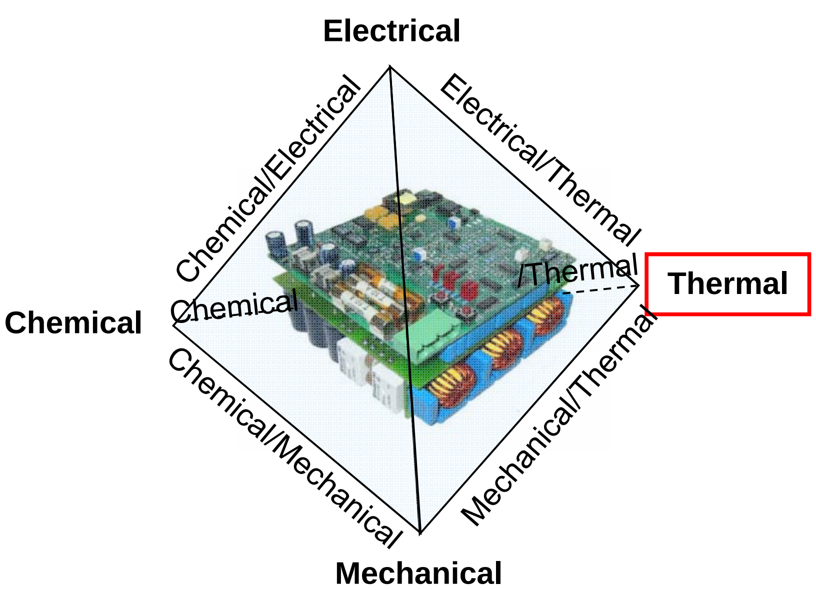
Modern High Performance AIT for WBG PSC PE
Spectra of Loads

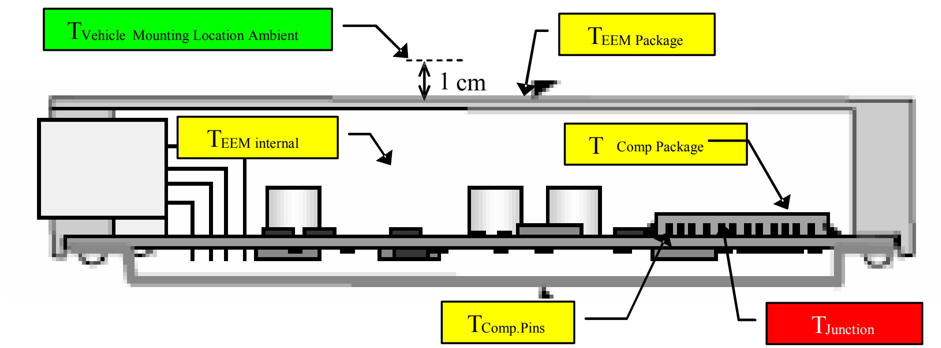


‚Dualism of AIT': Loads reflect functions

- Mechanical
- Thermal
- Electrical

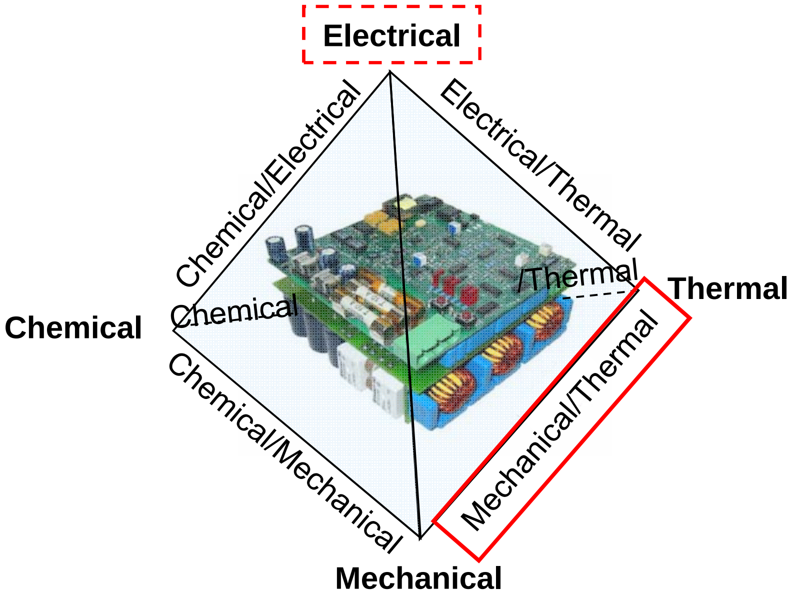
Modern High Performance AIT for WBG PSC PE
Loads on Power Electronics: Temperature





- Definitions of temperatures must be clear
  - junction, component, substrate, ambient, ...
- Consideration of temperature over time
- Maximum Operating Temperatures?
  - Depends on chosen technology base and components
  - Circuit carrier, especially pcb
  - Discrete mold package
  - ...

Modern High Performance AIT for WBG PSC PE
Loads on Power Electronics: Temperature Cycles



Passive Cycle Testing (ambient condition) (Temperature Cycle Test, TCT)

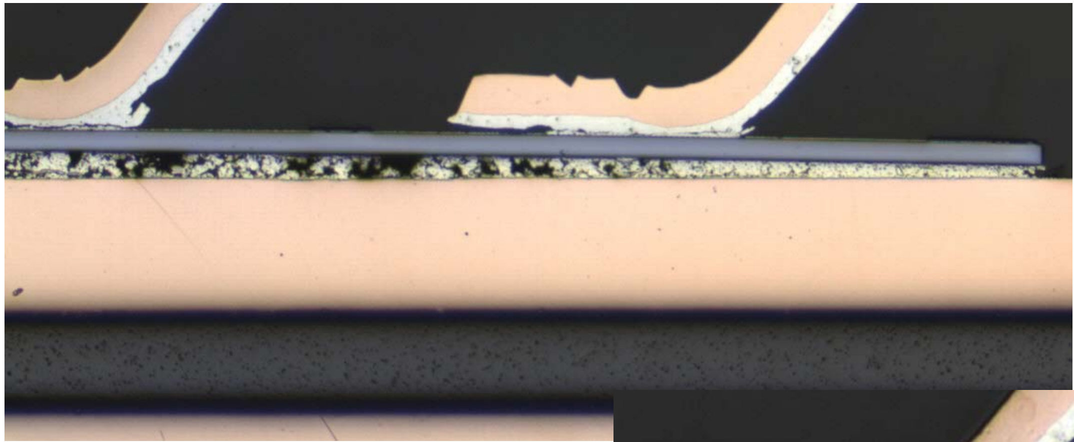
- Embossment by ambient: homogenous through heating and cooling
- shock condition in a two chamber funeral system
- ramped condition in a single chamber funeral system
- -40°C/+125°C, -40°C/+150°C swings are typically
- 30'/30' minutes dwell time is typically

Power Cycle Testing (active condition) (PCT)

- Embossment by current: temperature gradients
- Short-term period (≈1s) for near-chip bond-technology
- Long-term period (≈30s) for near chip die-attach-technology

Modern High Performance AIT for WBG PSC PE

Examples of Failure Mechanisms



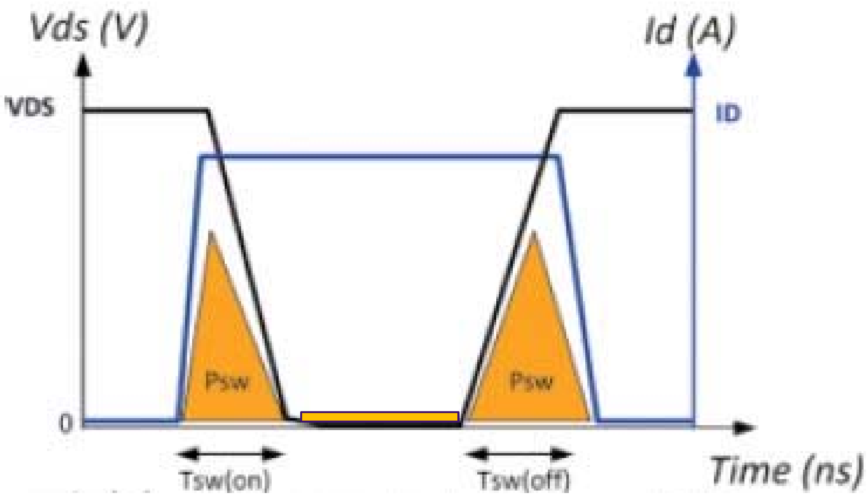
PCT-result in a soldered die-attach system:
Bond contacts and die-attach show typically a mixed failure mode

PCT-Result in a Ag-sintered die-attach system:
Typically just bond contacts show failure mode
But for pure Cu-bonding this effect is not valid any longer

Modern High Performance AIT for WBG PSC PE
Switching Losses in Power Electronics

Hard switching:

- Voltage and current change at same time
- DC-AC-drive inverter-type w/ f_{sw} ≈ 20 kHz
- Each switching event 'counts down life-time'
- Immediate PCT-scenario



$$P_{losses\ total} = Ps_{tat} + Pd_{yn}$$

$$P_{losses\ total} = \int V_{ds}(t) \times I_d(t)dt$$

Soft switching (ZVS):

- Voltage and current change phase shifted
- DC-DC-converter-type w/ f_{sw} ≥ 100 kHz up to 1 MHz
- Switching events average to elevated mid-term temperature level
- More similarity to TCT-scenario

$$P_{losses\ total} = [V_{ds} \times Id]_{steady\ state} + \int_{sw\ on} V_{ds}(t) \times I_d(t)dt + \int_{sw\ off} V_{ds}(t) \times I_d(t)dt$$

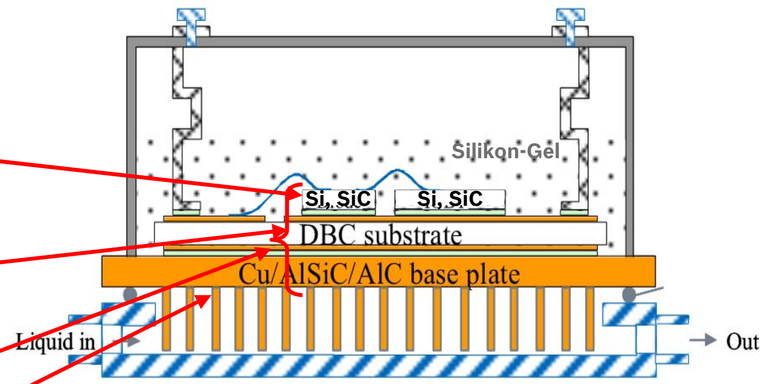
CR/APJ3-Rittner | 02/07/2017

Modern High Performance AIT for WBG PSC PE
Power Cycle Test Premises

Università degli Studi di Padova
Dipartimento di Ingegneria dell'Informazione
InRel NPower

Premises of Power Cycle Test

- Power semiconductor defines maximum $T_{junction}$
- Semiconductor, AIT und circuitry causes power losses P_{loss}
- Module design and AIT-materials' stack generate therm. resistance $R_{th,jc}$
- Thermal management defines T_{case}
- Temperature swings ΔT causes thermo-mechanical stress at different CTEs between devices and substrate



Sketch of a power module with liquid cooling

$$\Delta T = T_{junction} - T_{case} = P_{loss} \bullet R_{th,jc}$$

$$P^{1)}_{loss} = R^{2)}_{on} \bullet I^2$$

$$I = \sqrt{\frac{\Delta T}{R_{th,jc} \bullet R_{on}}}$$

1) Disregarding dynamic losses
2) Semiconductor and peripherals

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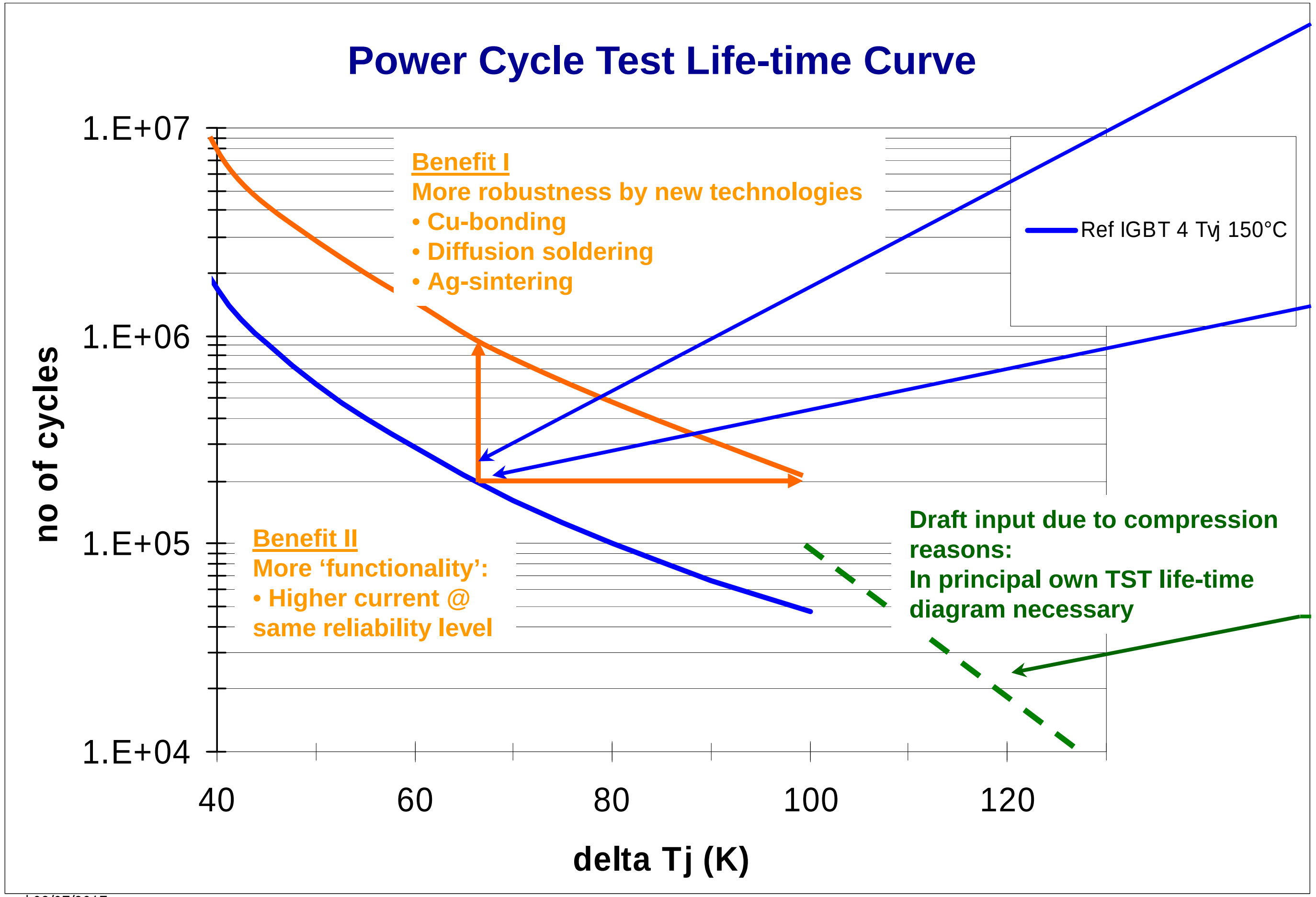
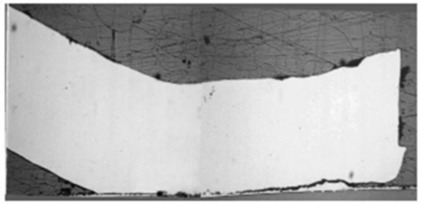
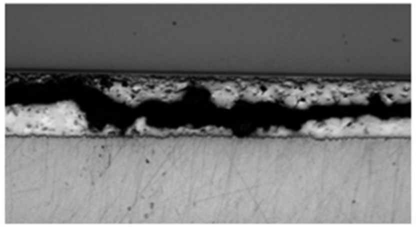
Modern High Performance AIT for WBG PSC PE
PCT Life-Time Curves



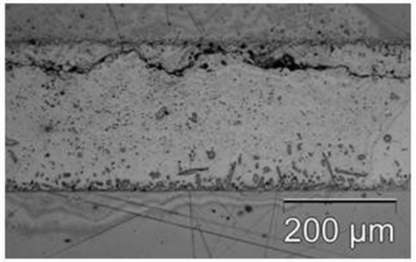
- Bond wire lift-off



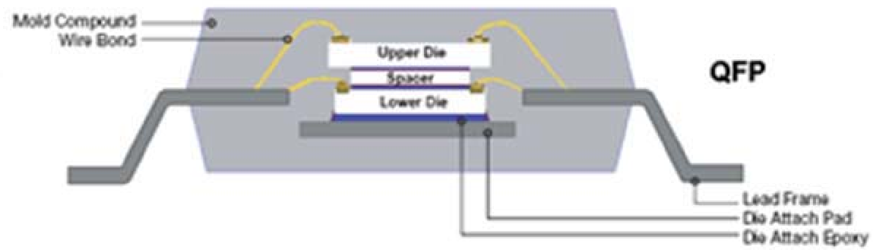
- Chip-to-substrate joint



- Substrate-to-baseplate



Modern High Performance AIT for WBG PSC PE
Semiconductor & AEC-Q100/-Q101



Typical design mold package for discrete device

- Semiconductor Packages
  - Discrete for logic/ASIC
  - Discrete for power
  - Bare-die
    - Typical for power modules
- Qualification referred to AEC-Q100/-Q101
  - Determined by descriptions of stress tests
  - Pre-defined stress tests with pre-defined load conditions
  - Sample lot sizes typical 45 ... 77 pieces within 1 ... 3 lots
  - Passed/not passed criteria
  - Objective in its origin: approval of samples for customer provision
  - Utilization meanwhile as ‘product and field-approval qualification’
  - Maximum applying remains yet on the level of ‘fit for test’

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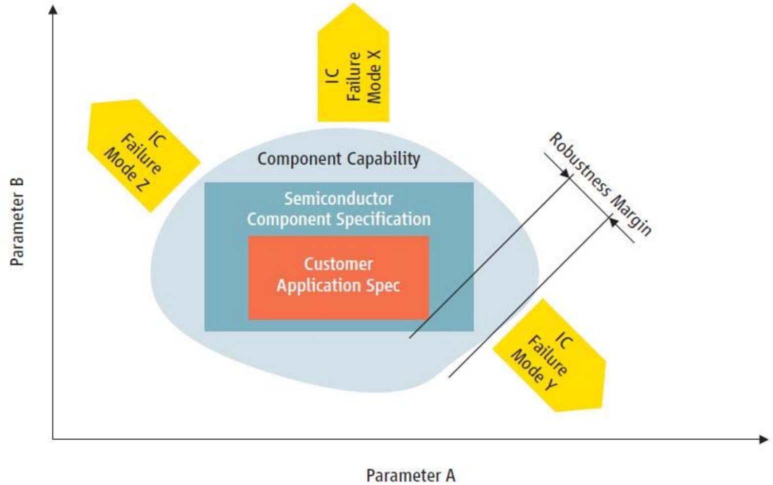
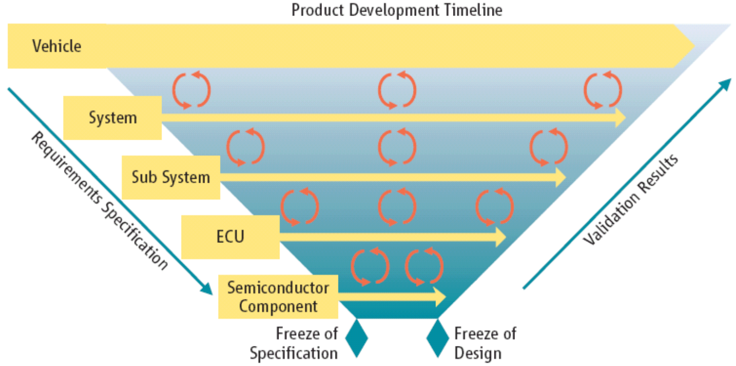
Modern High Performance AIT for WBG PSC PE
Robustness Validation

- Semiconductor
  - Removal of lack in AEC-Q100/-Q101
  - Change towards ‘fit for application’
  - Design for reliability/robustness
  - Description of the Mission Profile as core column
  - Derivation and performing of valid loading- and life-time tests
  - ‘Knowledge based qualification’
- ECUs
  - Systematic expansion of RV-methodology on the ECU level
  - Mission Profile (incl. manufact,/assembly)
  - Failure mechanisms and failure modes
  - Accelerating models for failure mechanisms
  - Field relevant accelerated testing





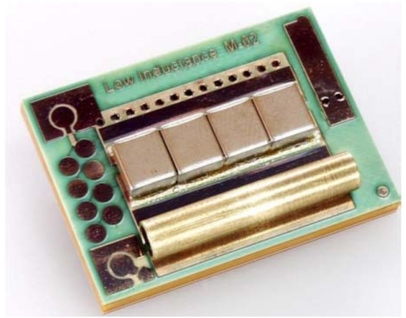
Picture Sources: Robustness Validation Handbooks, ZVEI

Modern High Performance AIT for WBG PSC PE
Wide-Band-Gap Power Modules

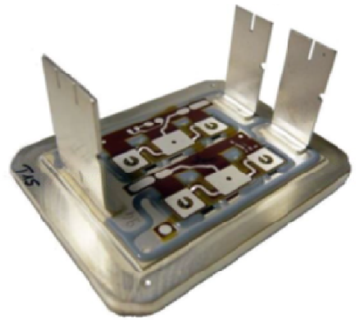
WBG-basing power modules changes something in comparison to ‘state of the art power module qualification (German OEM-Tier1-LV324)’

- Intensified trend towards SiC-MOSFET-basing power modules, in industrial applications and as well in automotive drive inverters, is foreseeable
- Data points in technology life-time curve, that reflect highly accelerated conditions at high ΔT ($\geq$ 100 K) for current Si-IGBT-based modules, will be data points for typical field loads in future SiC-MOSFET-basing modules
- SiC-MOSFET-performance – higher switching frequencies and steeper switching gradients – leads to distinct higher module complexity in design and chosen AIT
  - Low-inductive ‘planar-design’
  - Spatial close mounting of DC-link capacitor and integrated passive/active components

$\Rightarrow$ Effects on testability plus failure mechanisms/modes and root-cause analysis after loading are probably



Low-inductive SiC-MOSFET basing Power Module Picture Source: E. Hoene, FhG IZM, CIPS-conference 2014



Low-inductive SiC-MOSFET basing Power Module Picture Source: P. Beckedahl, SemiKron, CIPS-conference 2016

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Modern High Performance AIT for WBG PSC PE
Summary

- Power electronics assembly and interconnection technology is a complex ‘cross-disciplinary science’ between the science disciplines materials’ science, physics, chemistry, electronics engineering, mechanical engineering, ...
- Modern high performance AIT for WBG power semiconductor power electronics considers
  - Low-inductive power electronics design for fast switching and steep voltage and current gradients
  - New technology variations or even completely new technologies ‘beyond state of the art’
  - High temperature capability due to higher in application usable $T_{junctions}$
  - Thermal cycle robustness in TCT and PCT
  - Qualification routines: general ones and new upcoming specific ones
- WBG power semiconductors are ‘precious’ devices: AIT has to support their outperformance

Never forget: each power electronics design has to be ‘physical incarnated’ as hardware

⇒ Assembly and interconnection technology has to be mastered

⇒ Wide-band-gap power electronics demands new design boundaries